SAMSUNG Challenge the Limits

KS85F40113

High Performance 8-bit MCU for Portable Audio Application

The KS85F40113 single-chip CMOS microcontroller has been designed for high performance using Samsung's newest 8-bit CPU core, CalmRISC.

With features such as Multiple CODEC decoder capability, 8-channel A/D converter, full speed USB, DSP Architecture (24 x 24-bit MAC), and watch timer, the KS85F40113 offers an excellent and variety design solutions for portable digital audio systems.

Features

■ CPU
- 8-bit CalmRISC Core
- DSP Architecture (24 x 24-bit MAC)

■ Memory
- Code Memory : 128-K Bytes(64-KWord) Full Flash type memory(User PGM mode)
- Data Memory : 36-K Bytes SRAM.

■ I/O Pins
- I/O: 59pins, 8 input only pin.

■ ROM CODE OPTIONS
- Maximum Watchdog timer clock source select
- Basic timer counter clock source selecting reset value and CPU stop release bit select

■ 8-Bit Basic Timer & Watch-dog timer
- Programmable basic timer 8-bit counter + WDT 3-bit counter
- 8 kinds of clock source
- Overflow signal of 8-bit counter makes a basic timer interrupt. And control the oscillation warm-up time
- Overflow signal of 3-bit counter makes a system reset.

■ Two 8-Bit Timer/Counters
- Two programable timer/counters
- Interval, capture or match & overflow mode

■ 8-Bit Serial I/O Interface
- 8-bit transmit/receive or 8-bit receive mode.
- LSB first or MSB first transmission selectable.
- Internal and external clock source.

■ IIC, IIS Interface
- One-Ch Multi- Master IIC controller
- Two-Ch Sony/Phillips IIS controller

■ UART Interface - One Full-duplex UART controller

■ SSFDC Interface Logic

■ Random Number Generator

■ USB Specification Compliance(Ver1.0, Ver1.1)
- Built in Full Speed Transceiver
- Support 1 device address and 4 endpoints.
- One control endpoint and 3 data endpoints
- one 16 bytes endpoint, one 32 bytes end point, two 64 bytes endpoints.
- each data endpoint can be configurable as interrupt, bulk and isochronous.

■ Parallel Port Interface Controller
- Interrupt-based operation
- Support IEEE Standard 1284 communication mode(compatibility, nibble, byte and ECP mode).
- Supports ECP protocol with or without run-length encoding
- Automatic handshaking mode for any forward or reverse protocol with software enable/disable.

■ External Interrupt
- 10 source (Edge triggered 8 + Level triggered 2)

■ ADC - Six 8-bit resolution channels and normal input

■ Two Power-down Modes
- Idle mode : only CPU clock stop.
- Stop mode : system clock and CPU clock stop.

■ OSCILLATION SOURCES
- Clock Synthesizer(Phase Locked Loop) based on 32.768KHz.
- CPU clock divider circuit(Div by 1, 2, 4, 8, 16, 32, 64, 128)

■ INSTRUCTION EXECUTION TIMES
- 33.3ns at Fxx=30MHz when 1 cycle instruction
- 66.6ns at Fxx=30MHz when 2 cycle instruction

■ OPERATING TEMPERATURE
- - 40 ˚C to 85 ˚C

■ OPERATING VOLTAGE RANGE
- 3.0V to 3.6V at 30MHz

■ Package Types : 80-QFP, 80-TQFP

Strong Point

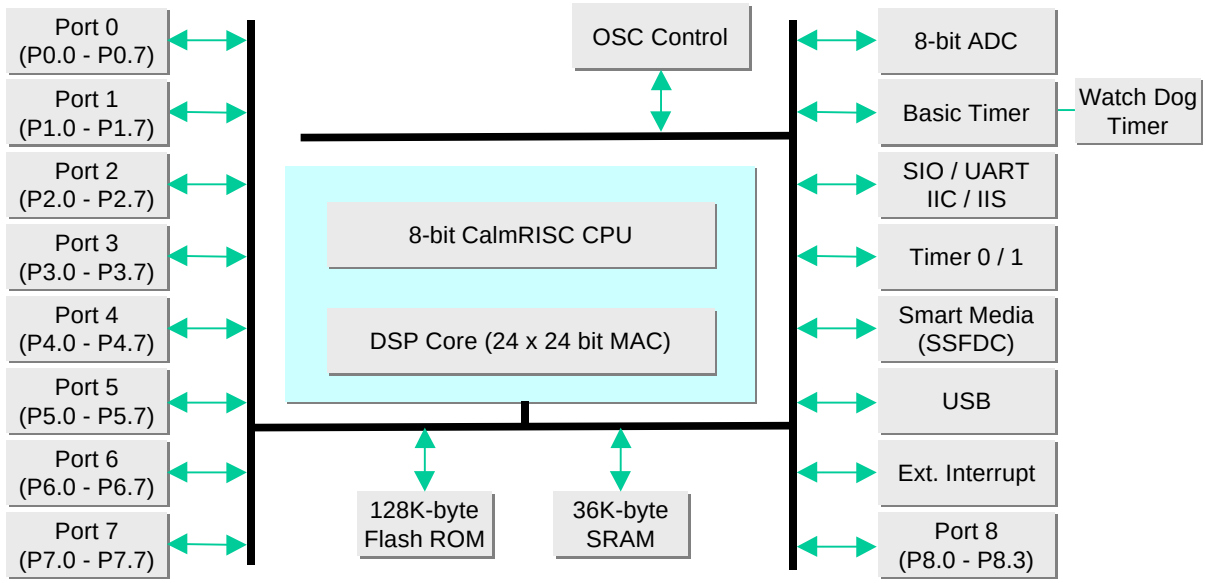
- Provide the Flash version of the device which is totally compatible with the standard mask ROM product
- Real time engineering support
- Competitive Price

Target Application

- Portable Digital Audio Application
  . MP3 (MPEG-1 Audio, Layer 3)
  . MS Audio 4.0
  . AAC
  . RealAudio (G2)
  . G.729, G.726

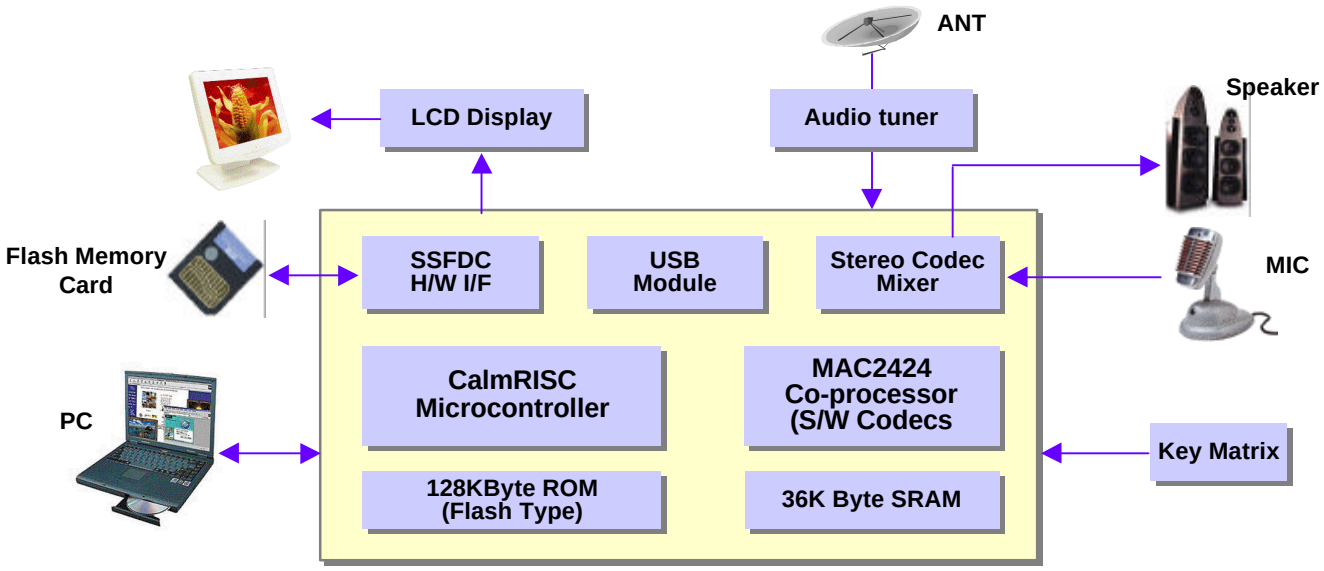
KS85F40113

Block Diagram



System Block Diagram

C-PAD (*C*almRISC for *P*ortable *A*udio *D*evice) Block Diagram (MP3 Application, KS85F40113)



Hardware Release Schedule

- E/S : End of Nov. `99
- M/P : '00. 3
- User's manual : End of Dec. `99
- Target Board : End of Dec. `99

Software Development Schedule

- MP3 Decoder : End of Dec. `99
- MS Audio 4.0 : End of Dec. `99
- A-CELP.live : End of Dec. `99

Contact Point

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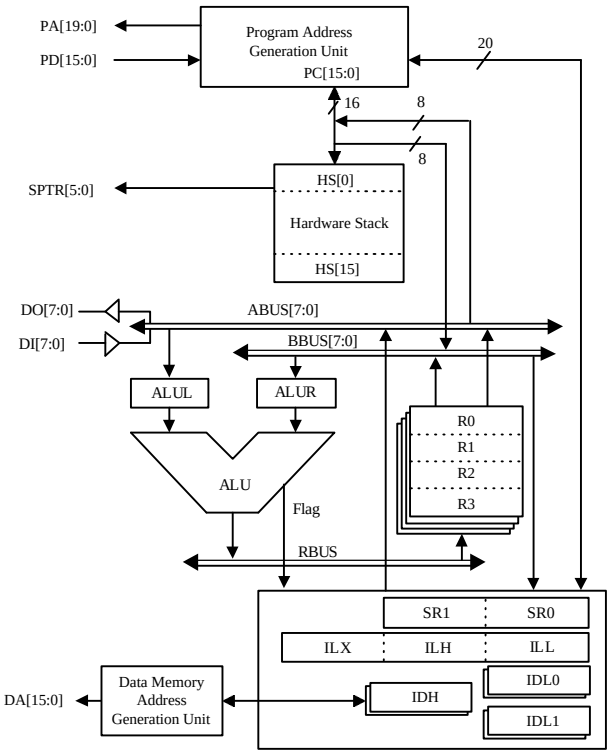
CalmRISC Core

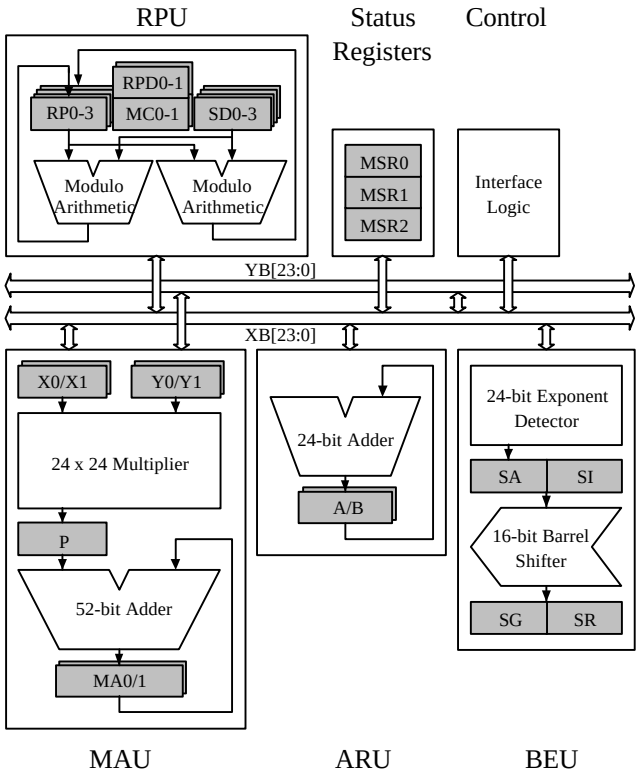
- 8-Bit Harvard RISC Core
  - Up to 1MWord Program Memory Space
  - Up to 64KByte Data Memory Space
- Register-Memory Instruction Set Architecture
- 3 Stage Pipeline
- 16 General Purpose Registers, 11 Special Purpose Register
- Efficient Coprocessor Interface (Fig. 3)
- 46 Instruction Classes including Coprocessor Instructions
- All Instructions 1 Word Long Except Long Branches (2 Words Long)
- Ultra Low Power and High Performance
  - 70¥ ìA/MIPS
  - 35 MIPS at 3.0V with 0.5¥ ìm 3-Metal CMOS Process



(Fig. 1)

MAC2424 Coprocessor

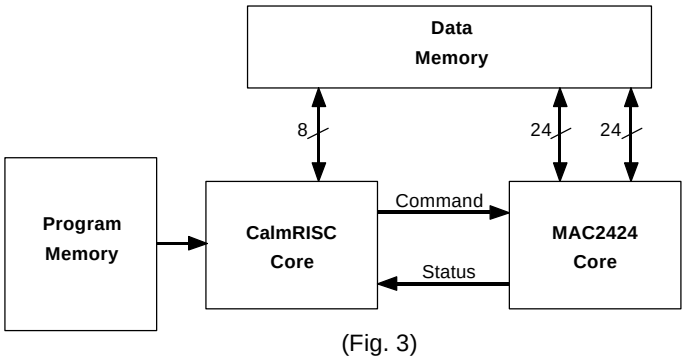
- 24-Bit MAC Engine
  - 24 by 24 Multiplier
  - 52 Bit Adder/Subtracter
- 2 MAC Accumulators (MA0, MA1)
- 32KWord X-Memory and Y-Memory Address Space (1Word = 3 Bytes)
- 2 Accumulators (A, B)
- 6 RAM Pointers(RP0/1/2/3, RPD0/1)
- Exponent Detector
- Barrel Shifter
- Ultra Low Power and High Performance
  - 300¥ ìA/MIPS
  - 35 MIPS at 3.0V with 0.5¥ ìm 3-Metal CMOS Process



(Fig. 2)

Coprocessor Interface

- Passive Coprocessor (Only CalmRISC Fetches Instructions)
  - 24 by 24 Multiplier
  - 52 Bit Adder/Subtracter
- Pipeline Synchronization between CalmRISC and MAC2424
  - No Resource Conflict
  - No Feadlock 32KWord X-Memory and Y-Memory Address Space (1Word = 3 Bytes)
- Real Time Status Flagging from a Coprocessor to CalmRISC
- Single MDS (Microprocessor Development System)



(Fig. 3)