

K7N163609A
K7N163209A
K7N161809A

Preliminary
512Kx36/32 & 1Mx18 Pipelined NtRAM™

Document Title

512Kx36/32 & 1Mx18-Bit Pipelined NtRAM™

Revision History

<u>Rev. No.</u>	<u>History</u>	<u>Draft</u>	<u>Date</u>	<u>Remark</u>
0.0	1. Initial document.		April. 18. 2001	Preliminary
0.1	1. Add JTAG Scan Order		May. 10. 2001	Preliminary
0.2	1. Add x32 org and industrial temperature . 2. Add 165FBGA package		Aug. 30. 2001	Preliminary

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16Mb NtRAM(Flow Through / Pipelined) / Sigma x72 Ordering Information

Org.	Part Number	Mode	VDD	Speed FT ; Access Time(ns) Pipelined ; Cycle Time(MHz)	PKG	Temp
1Mx18	K7M161825A-Q(H/F)C(I)65/75/85	FlowThrough	3.3	6.5/7.5/8.5ns	Q : 100TQFP H : 119BGA F: 165FBGA	C (Commercial Temperature Range) I (Industrial Temperature Range)
	K7N161801A-Q(H/F)C(I)16/13	Pipelined	3.3	167/133MHz		
	K7N161809A-Q(H/F)C(I)25/22/20	Pipelined	3.3	250/225/200MHz		
	K7N161845A-Q(H/F)C(I)16/13	Pipelined	2.5	167/133MHz		
	K7N161849A-Q(H/F)C(I)25/22/20	Pipelined	2.5	250/225/200MHz		
512Kx32	K7M163225A-QC(I)65/75/85	FlowThrough	3.3	6.5/7.5/8.5ns		
	K7N163201A-QC(I)16/13	Pipelined	3.3	167/133MHz		
	K7N163209A-QC(I)25/22/20	Pipelined	3.3	250/225/200MHz		
	K7N163245A-QC(I)16/13	Pipelined	2.5	167/133MHz		
	K7N163249A-QC(I)25/22/20	Pipelined	2.5	250/225/200MHz		
512Kx36	K7M163625A-Q(H/F)C(I)65/75/85	FlowThrough	3.3	6.5/7.5/8.5ns		
	K7N163601A-Q(H/F)C(I)16/13	Pipelined	3.3	167/133MHz		
	K7N163609A-Q(H/F)C(I)25/22/20	Pipelined	3.3	250/225/200MHz		
	K7N163645A-Q(H/F)C(I)16/13	Pipelined	2.5	167/133MHz		
	K7N163649A-Q(H/F)C(I)25/22/20	Pipelined	2.5	250/225/200MHz		
256Kx72	K7N167245A-HC16/13	Pipelined (Normal Type)	2.5	167/133MHz	H : 209BGA	
	K7N167249A-HC25/22/20	Pipelined (Normal Type)	2.5	250/225/200MHz		
	K7Z167285A-HC30/27/25	Pipelined (Sigma Type)	1.8	300/275/250MHz		

512Kx36/32 & 1Mx18-Bit Pipelined NtRAM™

FEATURES

- 3.3V+0.165V/-0.165V Power Supply.
- I/O Supply Voltage 3.3V+0.165V/-0.165V for 3.3V I/O or 2.5V+0.4V/-0.125V for 2.5V I/O.
- Byte Writable Function.
- Enable clock and suspend operation.
- Single READ/WRITE control pin.
- Self-Timed Write Cycle.
- Three Chip Enable for simple depth expansion with no data-contention.
- A interleaved burst or a linear burst mode.
- Asynchronous output enable control.
- Power Down mode.
- 100-TQFP-1420A /119BGA(7x17 Ball Grid Array Package).
- 165FBGA(11x15 ball array) with body size of 13mmx15mm.
- Operating in commercial and industrial temperature range.

FAST ACCESS TIMES

PARAMETER	Symbol	-25	-22	-20	Unit
Cycle Time	tCYC	4.0	4.4	5.0	ns
Clock Access Time	tCD	2.6	2.8	3.2	ns
Output Enable Access Time	tOE	2.6	2.8	3.2	ns

GENERAL DESCRIPTION

The K7N163609A, K7N163209A and K7N161809A are 18,874,368-bits Synchronous Static SRAMs.

The NtRAM™, or No Turnaround Random Access Memory utilizes all the bandwidth in any combination of operating cycles. Address, data inputs, and all control signals except output enable and linear burst order are synchronized to input clock. Burst order control must be tied "High or Low".

Asynchronous inputs include the sleep mode enable(ZZ).

Output Enable controls the outputs at any given time.

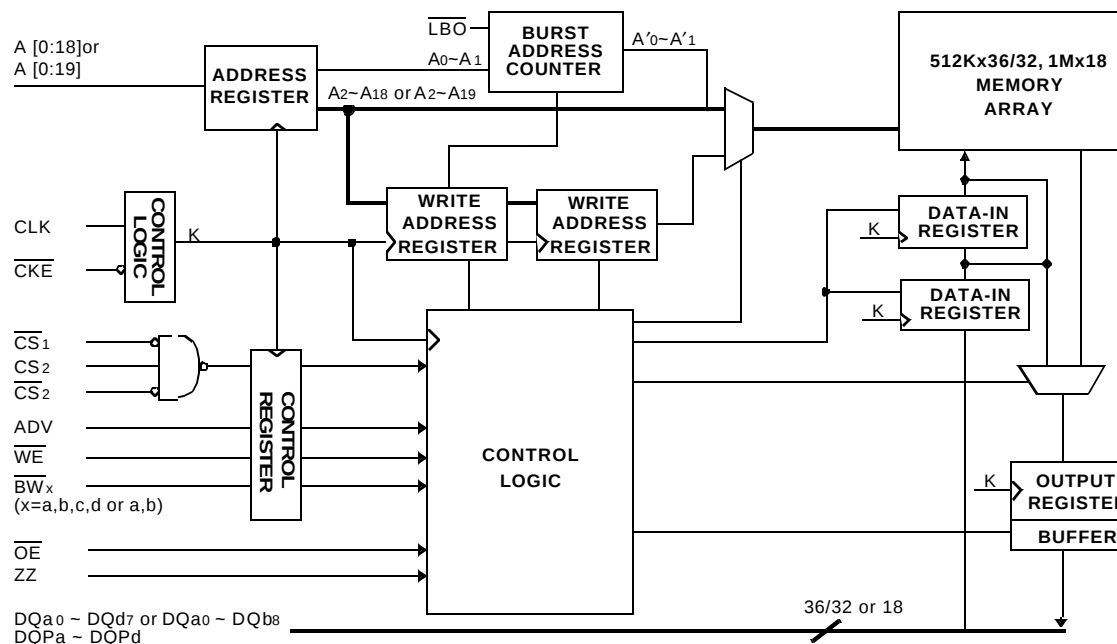
Write cycles are internally self-timed and initiated by the rising edge of the clock input. This feature eliminates complex off-chip write pulse generation

and provides increased timing flexibility for incoming signals.

For read cycles, pipelined SRAM output data is temporarily stored by an edge triggered output register and then released to the output buffers at the next rising edge of clock.

The K7N163609A, K7N163209A and K7N161809A are implemented with SAMSUNG's high performance CMOS technology and is available in 100pin TQFP, 119BGA and 165FBGA packages. Multiple power and ground pins minimize ground bounce.

LOGIC BLOCK DIAGRAM

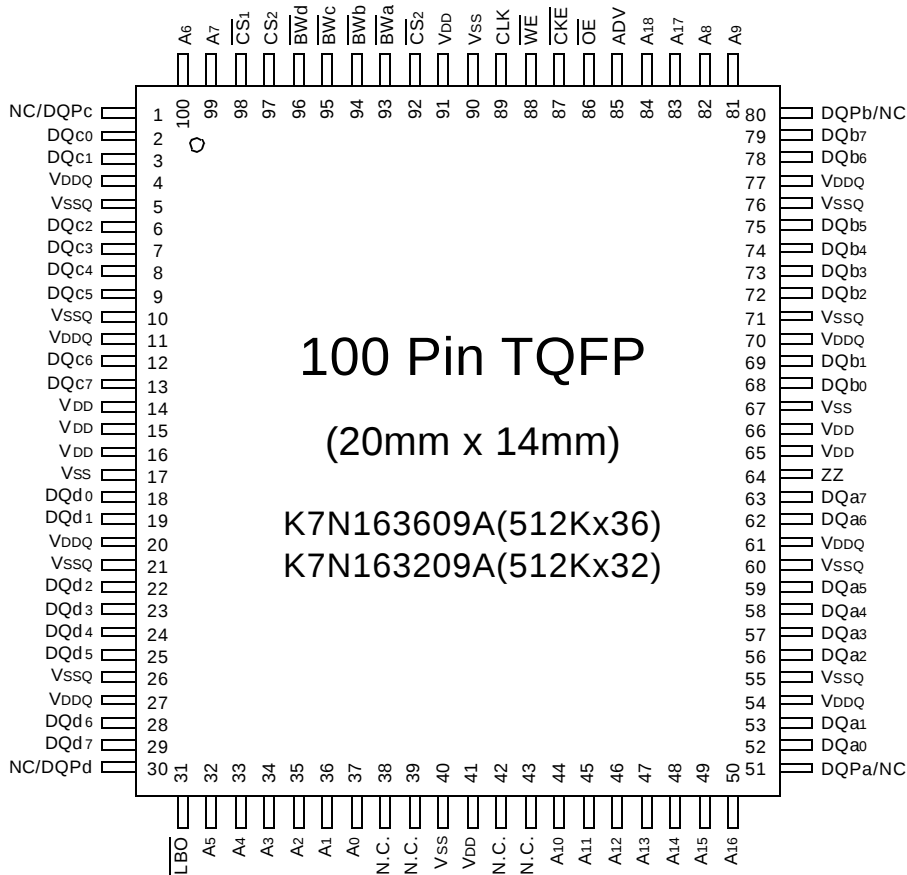


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PIN CONFIGURATION(TOP VIEW)



PIN NAME

SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A0 - A18	Address Inputs	32,33,34,35,36,37,44,45,46,47,48,49,50,81,82,83,84,99,100	VDD	Power Supply(+3.3V)	14,15,16,41,65,66,91
ADV	Address Advance/Load	85	VSS	Ground	17,40,67,90
WE	Read/Write Control Input	88	N.C.	No Connect	38,39,42,43
CLK	Clock	89	DQa0~a7	Data Inputs/Outputs	52,53,56,57,58,59,62,63
CKE	Clock Enable	87	DQb0~b7	Data Inputs/Outputs	68,69,72,73,74,75,78,79
CS1	Chip Select	98	DQc0~c7	Data Inputs/Outputs	2,3,6,7,8,9,12,13
CS2	Chip Select	97	DQd0~d7	Data Inputs/Outputs	18,19,22,23,24,25,28,29
CS2	Chip Select	92	DQPa~Pd	Data Inputs/Outputs	51,80,1,30
BWx(x=a,b,c,d)	Byte Write Inputs	93,94,95,96			
OE	Output Enable	86	VDDQ	Output Power Supply (3.3V or 2.5V)	4,11,20,27,54,61,70,77
ZZ	Power Sleep Mode	64	VSSQ	Output Ground	5,10,21,26,55,60,71,76
LBO	Burst Mode Control	31			

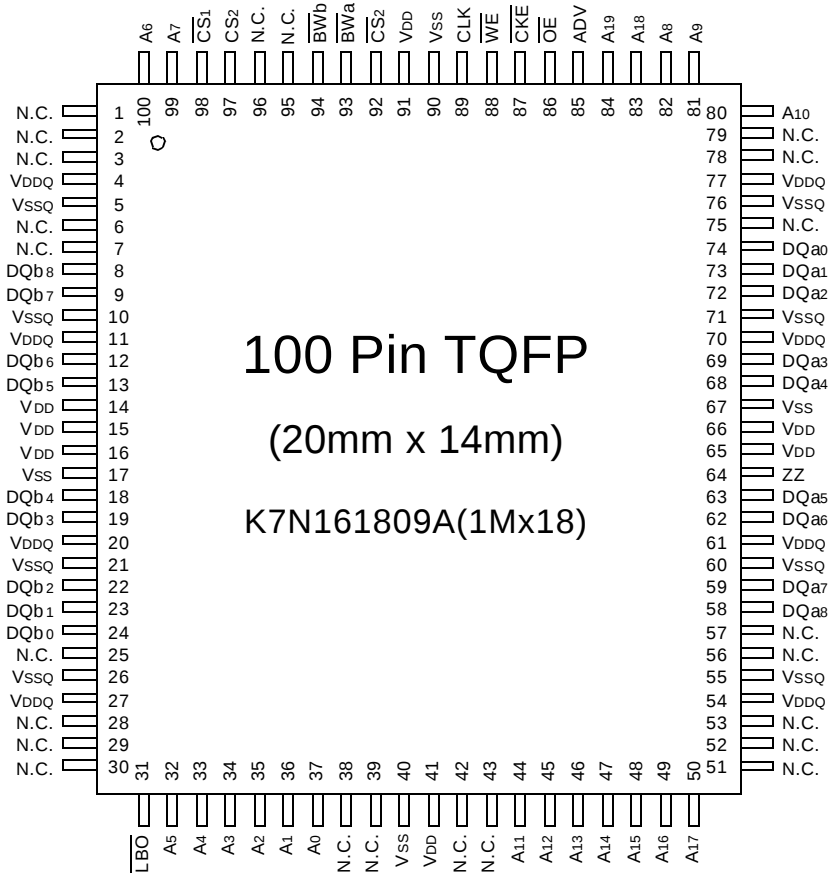
Note : 1. A0 and A1 are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

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PIN CONFIGURATION(TOP VIEW)



PIN NAME

SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A0 - A19	Address Inputs	32,33,34,35,36,37,44 45,46,47,48,49,50,80 81,82,83,84,99,100	VDD	Power Supply(+3.3V)	14,15,16,41,65,66,91
			VSS	Ground	17,40,67,90
ADV	Address Advance/Load	85	N.C.	No Connect	1,2,3,6,7,25,28,29,30, 38,39,42,43,51,52,53, 56,57,75,78,79,95,96
WE	Read/Write Control Input	88			
CLK	Clock	89			
CKE	Clock Enable	87			
CS1	Chip Select	98	DQa0~a8	Data Inputs/Outputs	58,59,62,63,68,69,72,73,74
CS2	Chip Select	97	DQb0~b8	Data Inputs/Outputs	8,9,12,13,18,19,22,23,24
CS2	Chip Select	92			
BWx(x=a,b)	Byte Write Inputs	93,94			
OE	Output Enable	86	VDDQ	Output Power Supply (3.3V or 2.5V)	4,11,20,27,54,61,70,77
ZZ	Power Sleep Mode	64	VSSQ	Output Ground	5,10,21,26,55,60,71,76
LBO	Burst Mode Control	31			

NOTE : A0 and A1 are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

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119BGA PACKAGE PIN CONFIGURATIONS(TOP VIEW)

K7N163609A(512Kx36)

	1	2	3	4	5	6	7
A	VDDQ	A	A	A	A	A	VDDQ
B	NC	CS2	A	ADV	A	$\overline{CS2}$	NC
C	NC	A	A	VDD	A	A	NC
D	DQc	DQPc	VSS	NC	VSS	DQPb	DQb
E	DQc	DQc	VSS	$\overline{CS1}$	VSS	DQb	DQb
F	VDDQ	DQc	VSS	$\overline{OE}$	VSS	DQb	VDDQ
G	DQc	DQc	$\overline{BWc}$	A	$\overline{BWb}$	DQb	DQb
H	DQc	DQc	VSS	$\overline{WE}$	VSS	DQb	DQb
J	VDDQ	VDD	NC	VDD	NC	VDD	VDDQ
K	DQd	DQd	VSS	CLK	VSS	DQa	DQa
L	DQd	DQd	$\overline{BWd}$	NC	$\overline{BWa}$	DQa	DQa
M	VDDQ	DQd	VSS	$\overline{CKE}$	VSS	DQa	VDDQ
N	DQd	DQd	VSS	A1*	VSS	DQa	DQa
P	DQd	DQPd	VSS	A0*	VSS	DQPa	DQa
R	NC	A	$\overline{LBO}$	VDD	NC	A	NC
T	NC	NC	A	A	A	NC	ZZ
U	VDDQ	TMS	TDI	TCK	TDO	NC	VDDQ

Note : * A₀ and A₁ are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

PIN NAME

SYMBOL	PIN NAME	SYMBOL	PIN NAME
A	Address Inputs	VDD	Power Supply
A ₀ ,A ₁	Burst Address Inputs	VSS	Ground
ADV	Address Advance/Load	N.C.	No Connect
$\overline{WE}$	Read/Write Control Input		
CLK	Clock	DQa	Data Inputs/Outputs
$\overline{CKE}$	Clock Enable	DQb	Data Inputs/Outputs
CS ₁	Chip Select	DQc	Data Inputs/Outputs
CS ₂	Chip Select	DQd	Data Inputs/Outputs
$\overline{CS2}$	Chip Select	DQPa~Pd	Data Inputs/Outputs
$\overline{BWx}$	Byte Write Inputs		
(x=a,b,c,d)		VDDQ	Output Power Supply
$\overline{OE}$	Output Enable		
ZZ	Power Sleep Mode		
$\overline{LBO}$	Burst Mode Control		
TCK	JTAG Test Clock		
TMS	JTAG Test Mode Select		
TDI	JTAG Test Data Input		
TDO	JTAG Test Data Output		

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119BGA PACKAGE PIN CONFIGURATIONS(TOP VIEW)

K7N161809A(1Mx18)

	1	2	3	4	5	6	7
A	VDDQ	A	A	A	A	A	VDDQ
B	NC	CS2	A	ADV	A	CS2	NC
C	NC	A	A	VDD	A	A	NC
D	DQb	NC	VSS	NC	VSS	DQPa	NC
E	NC	DQb	VSS	CS1	VSS	NC	DQa
F	VDDQ	NC	VSS	OE	VSS	DQa	VDDQ
G	NC	DQb	BWb	A	VSS	NC	DQa
H	DQb	NC	VSS	WE	VSS	DQa	NC
J	VDDQ	VDD	NC	VDD	NC	VDD	VDDQ
K	NC	DQb	VSS	CLK	VSS	NC	DQa
L	DQb	NC	VSS	NC	BWa	DQa	NC
M	VDDQ	DQb	VSS	CKE	VSS	NC	VDDQ
N	DQb	NC	VSS	A1*	VSS	DQa	NC
P	NC	DQPb	VSS	A0*	VSS	NC	DQa
R	NC	A	LBO	VDD	NC	A	NC
T	NC	A	A	NC	A	A	ZZ
U	VDDQ	TMS	TDI	TCK	TDO	NC	VDDQ

Note : * A₀ and A₁ are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

PIN NAME

SYMBOL	PIN NAME	SYMBOL	PIN NAME
A	Address Inputs	VDD	Power Supply
A ₀ ,A ₁	Burst Address Inputs	VSS	Ground
ADV	Address Advance/Load	N.C.	No Connect
WE	Read/Write Control Input		
CLK	Clock		
CKE	Clock Enable	DQa	Data Inputs/Outputs
CS1	Chip Select	DQb	Data Inputs/Outputs
CS2	Chip Select	DQPa, Pb	Data Inputs/Outputs
CS2	Chip Select		
BWx	Byte Write Inputs	VDDQ	Output Power Supply
(x=a,b)			
OE	Output Enable		
ZZ	Power Sleep Mode		
LBO	Burst Mode Control		
TCK	JTAG Test Clock		
TMS	JTAG Test Mode Select		
TDI	JTAG Test Data Input		
TDO	JTAG Test Data Output		

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165-PIN FGPA PACKAGE CONFIGURATIONS(TOP VIEW)

K7N163609A(512Kx36)

	1	2	3	4	5	6	7	8	9	10	11
A	NC	A	$\overline{CS1}$	$\overline{BWc}$	$\overline{BWb}$	$\overline{CS2}$	$\overline{CKE}$	ADV	A	A	NC
B	NC	A	CS2	$\overline{BWd}$	$\overline{BWa}$	CLK	$\overline{WE}$	$\overline{OE}$	A	A	NC
C	DQPc	NC	VDDQ	VSS	VSS	VSS	VSS	VSS	VDDQ	NC	DQPb
D	DQc	DQc	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQb	DQb
E	DQc	DQc	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQb	DQb
F	DQc	DQc	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQb	DQb
G	DQc	DQc	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQb	DQb
H	NC	VDD	NC	VDD	VSS	VSS	VSS	VDD	NC	NC	ZZ
J	DQd	DQd	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	DQa
K	DQd	DQd	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	DQa
L	DQd	DQd	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	DQa
M	DQd	DQd	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	DQa
N	DQPa	NC	VDDQ	VSS	NC	NC	NC	VSS	VDDQ	NC	DQPa
P	NC	NC	A	A	TDI	A1*	TDO	A	A	A	NC
R	$\overline{LBO}$	NC	A	A	TMS	A0*	TCK	A	A	A	A

Note : * A0 and A1 are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

PIN NAME

SYMBOL	PIN NAME	SYMBOL	PIN NAME
A	Address Inputs	VDD	Power Supply
A0,A1	Burst Address Inputs	VSS	Ground
ADV	Address Advance/Load	N.C.	No Connect
$\overline{WE}$	Read/Write Control Input		
CLK	Clock	DQa	Data Inputs/Outputs
$\overline{CKE}$	Clock Enable	DQb	Data Inputs/Outputs
CS1	Chip Select	DQc	Data Inputs/Outputs
CS2	Chip Select	DQd	Data Inputs/Outputs
CS2	Chip Select	DQPa-Pd	Data Inputs/Outputs
$\overline{BWx}$ (x=a,b,c,d)	Byte Write Inputs	VDDQ	Output Power Supply
$\overline{OE}$	Output Enable		
ZZ	Power Sleep Mode		
$\overline{LBO}$	Burst Mode Control		
TCK	JTAG Test Clock		
TMS	JTAG Test Mode Select		
TDI	JTAG Test Data Input		
TDO	JTAG Test Data Output		

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165-PIN FGPA PACKAGE CONFIGURATIONS(TOP VIEW)

K7N161809A(1Mx18)

	1	2	3	4	5	6	7	8	9	10	11
A	NC	A	$\overline{\text{CS}}1$	$\overline{\text{BW}}b$	NC	$\overline{\text{CS}}2$	$\overline{\text{CKE}}$	ADV	A	A	A
B	NC	A	CS2	NC	$\overline{\text{BW}}a$	CLK	$\overline{\text{WE}}$	$\overline{\text{OE}}$	A	A	NC
C	NC	NC	VDDQ	VSS	VSS	VSS	VSS	VSS	VDDQ	NC	DQPa
D	NC	DQb	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	DQa
E	NC	DQb	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	DQa
F	NC	DQb	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	DQa
G	NC	DQb	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	DQa
H	NC	VDD	NC	VDD	VSS	VSS	VSS	VDD	NC	NC	ZZ
J	DQb	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	NC
K	DQb	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	NC
L	DQb	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	NC
M	DQb	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	NC
N	DQPa	NC	VDDQ	VSS	NC	NC	NC	VSS	VDDQ	NC	NC
P	NC	NC	A	A	TDI	A1*	TDO	A	A	A	NC
R	$\overline{\text{LBO}}$	NC	A	A	TMS	A0*	TCK	A	A	A	A

Note : * A0 and A1 are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

PIN NAME

SYMBOL	PIN NAME	SYMBOL	PIN NAME
A	Address Inputs	VDD	Power Supply
A0,A1	Burst Address Inputs	VSS	Ground
ADV	Address Advance/Load	N.C.	No Connect
$\overline{\text{WE}}$	Read/Write Control Input		
CLK	Clock		
$\overline{\text{CKE}}$	Clock Enable	DQa	Data Inputs/Outputs
$\overline{\text{CS}}1$	Chip Select	DQb	Data Inputs/Outputs
$\overline{\text{CS}}2$	Chip Select	DQPa, Pb	Data Inputs/Outputs
$\overline{\text{CS}}2$	Chip Select		
$\overline{\text{BW}}x$	Byte Write Inputs	VDDQ	Output Power Supply
(x=a,b)			
$\overline{\text{OE}}$	Output Enable		
ZZ	Power Sleep Mode		
$\overline{\text{LBO}}$	Burst Mode Control		
TCK	JTAG Test Clock		
TMS	JTAG Test Mode Select		
TDI	JTAG Test Data Input		
TDO	JTAG Test Data Output		

FUNCTION DESCRIPTION

The K7N163609A, K7N163209A and K7N161809A are NtRAM™ designed to sustain 100% bus bandwidth by eliminating turnaround cycle when there is transition from Read to Write, or vice versa.

All inputs (with the exception of $\overline{OE}$, $\overline{LBO}$ and $\overline{ZZ}$) are synchronized to rising clock edges.

All read, write and deselect cycles are initiated by the ADV input. Subsequent burst addresses can be internally generated by the burst advance pin (ADV). ADV should be driven to Low once the device has been deselected in order to load a new address for next operation.

Clock Enable($\overline{CKE}$) pin allows the operation of the chip to be suspended as long as necessary. When $\overline{CKE}$ is high, all synchronous inputs are ignored and the internal device registers will hold their previous values.

NtRAM™ latches external address and initiates a cycle, when $\overline{CKE}$, ADV are driven to low and all three chip enables($\overline{CS1}$, $\overline{CS2}$, $\overline{CS2}$) are active .

Output Enable($\overline{OE}$) can be used to disable the output at any given time.

Read operation is initiated when at the rising edge of the clock, the address presented to the address inputs are latched in the address register, $\overline{CKE}$ is driven low, all three chip enables($\overline{CS1}$, $\overline{CS2}$, $\overline{CS2}$) are active, the write enable input signals $\overline{WE}$ are driven high, and ADV driven low. The internal array is read between the first rising edge and the second rising edge of the clock and the data is latched in the output register. At the second clock edge the data is driven out of the SRAM. Also during read operation $\overline{OE}$ must be driven low for the device to drive out the requested data.

Write operation occurs when $\overline{WE}$ is driven low at the rising edge of the clock. $\overline{BW[d:a]}$ can be used for byte write operation. The pipelined NtRAM™ uses a late-late write cycle to utilize 100% of the bandwidth.

At the first rising edge of the clock, $\overline{WE}$ and address are registered, and the data associated with that address is required two cycle later.

Subsequent addresses are generated by ADV High for the burst access as shown below. The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion.

The burst sequence is determined by the state of the $\overline{LBO}$ pin. When this pin is low, linear burst sequence is selected.

And when this pin is high, Interleaved burst sequence is selected.

During normal operation, $\overline{ZZ}$ must be driven low. When $\overline{ZZ}$ is driven high, the SRAM will enter a Power Sleep Mode after 2 cycles. At this time, internal state of the SRAM is preserved. When $\overline{ZZ}$ returns to low, the SRAM normally operates after 2 cycles of wake up time.

BURST SEQUENCE TABLE

(Interleaved Burst, $\overline{LBO}$ =High)

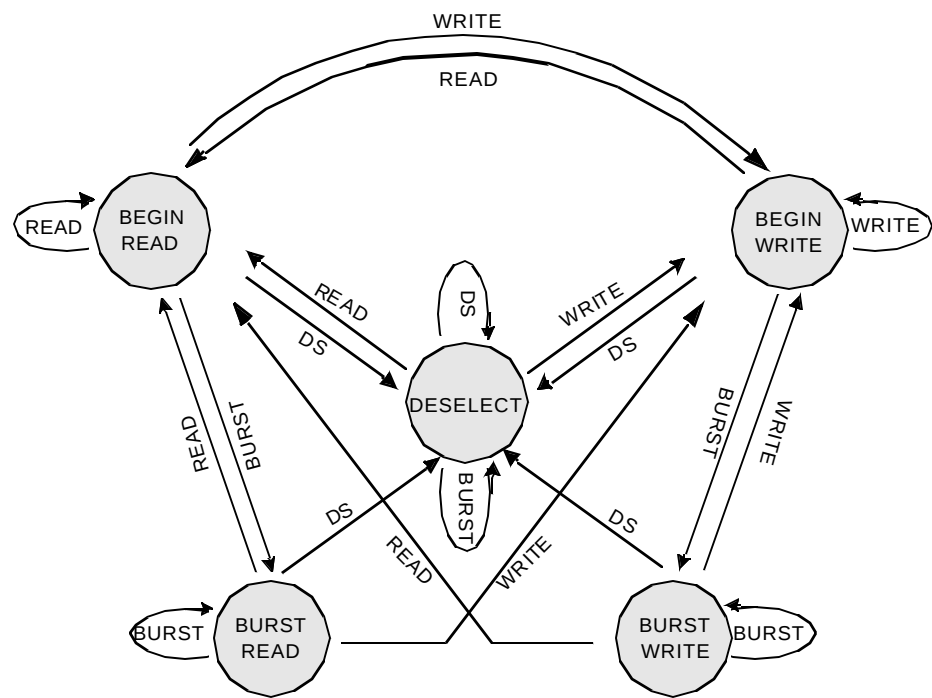
$\overline{\text{LBOPIN}}$	HIGH	Case 1		Case 2		Case 3		Case 4	
		A ₁	A ₀	A ₁	A ₀	A ₁	A ₀	A ₁	A ₀
First Address ↓ Fourth Address		0	0	0	1	1	0	1	1
		0	1	0	0	1	1	1	0
		1	0	1	1	0	0	0	1
		1	1	1	0	0	1	0	0

(Linear Burst, $\overline{LBO}$ =Low)

$\overline{\text{LBO}}$ PIN	LOW	Case 1		Case 2		Case 3		Case 4	
		A ₁	A ₀	A ₁	A ₀	A ₁	A ₀	A ₁	A ₀
First Address ↓ Fourth Address		0	0	0	1	1	0	1	1
		0	1	1	0	1	1	0	0
		1	0	1	1	0	0	0	1
		1	1	0	0	0	1	1	0

Note : 1. $\overline{LBO}$ pin must be tied to High or Low, and Floating State must not be allowed.

STATE DIAGRAM FOR NtRAM™



COMMAND	ACTION
DS	DESELECT
READ	BEGIN READ
WRITE	BEGIN WRITE
BURST	BEGIN READ BEGIN WRITE CONTINUE DESELECT

Notes : 1. An IGNORE CLOCK EDGE cycle is not shown in the above diagram. This is because CKE HIGH only blocks the clock(CLK) input and does not change the state of the device.
2. States change on the rising edge of the clock(CLK)

TRUTH TABLES

SYNCHRONOUS TRUTH TABLE

$\overline{CS_1}$	CS_2	$\overline{CS_2}$	ADV	$\overline{WE}$	$\overline{BW_x}$	$\overline{OE}$	$\overline{CKE}$	CLK	ADDRESS ACCESSED	Operation
H	X	X	L	X	X	X	L	↑	N/A	Not Selected
X	L	X	L	X	X	X	L	↑	N/A	Not Selected
X	X	H	L	X	X	X	L	↑	N/A	Not Selected
X	X	X	H	X	X	X	L	↑	N/A	Not Selected Continue
L	H	L	L	H	X	L	L	↑	External Address	Begin Burst Read Cycle
X	X	X	H	X	X	L	L	↑	Next Address	Continue Burst Read Cycle
L	H	L	L	H	X	H	L	↑	External Address	NOP/Dummy Read
X	X	X	H	X	X	H	L	↑	Next Address	Dummy Read
L	H	L	L	L	L	X	L	↑	External Address	Begin Burst Write Cycle
X	X	X	H	X	L	X	L	↑	Next Address	Continue Burst Write Cycle
L	H	L	L	L	H	X	L	↑	N/A	NOP/Write Abort
X	X	X	H	X	H	X	L	↑	Next Address	Write Abort
X	X	X	X	X	X	X	H	↑	Current Address	Ignore Clock

- Notes :** 1. X means "Don't Care". 2. The rising edge of clock is symbolized by (↑).
3. A continue deselect cycle can only be entered if a deselect cycle is executed first.
4. $\overline{WRITE} = L$ means Write operation in WRITE TRUTH TABLE.
 $\overline{WRITE} = H$ means Read operation in WRITE TRUTH TABLE.
5. Operation finally depends on status of asynchronous input pins(ZZ and $\overline{OE}$).

WRITE TRUTH TABLE(x36/x32)

$\overline{WE}$	$\overline{BW_a}$	$\overline{BW_b}$	$\overline{BW_c}$	$\overline{BW_d}$	OPERATION
H	X	X	X	X	READ
L	L	H	H	H	WRITE BYTE a
L	H	L	H	H	WRITE BYTE b
L	H	H	L	H	WRITE BYTE c
L	H	H	H	L	WRITE BYTE d
L	L	L	L	L	WRITE ALL BYTES
L	H	H	H	H	WRITE ABORT/NOP

- Notes :** 1. X means "Don't Care".
2. All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).

WRITE TRUTH TABLE(x18)

$\overline{WE}$	$\overline{BW_a}$	$\overline{BW_b}$	OPERATION
H	X	X	READ
L	L	H	WRITE BYTE a
L	H	L	WRITE BYTE b
L	L	L	WRITE ALL BYTES
L	H	H	WRITE ABORT/NOP

- Notes :** 1. X means "Don't Care".
2. All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).

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ASYNCHRONOUS TRUTH TABLE

OPERATION	ZZ	OE	I/O STATUS
Sleep Mode	H	X	High-Z
Read	L	L	DQ
	L	H	High-Z
Write	L	X	Din, High-Z
Deselected	L	X	High-Z

Notes

1. X means "Don't Care".
2. Sleep Mode means power Sleep Mode of which stand-by current does not depend on cycle time.
3. Deselected means power Sleep Mode of which stand-by current depends on cycle time.

ABSOLUTE MAXIMUM RATINGS*

PARAMETER		SYMBOL	RATING	UNIT
Voltage on V _{DD} Supply Relative to V _{SS}		V _{DD}	-0.3 to 4.6	V
Voltage on Any Other Pin Relative to V _{SS}		V _{IN}	-0.3 to V _{DD} +0.3	V
Power Dissipation		P _D	1.6	W
Storage Temperature		T _{STG}	-65 to 150	°C
Operating Temperature	Commercial	T _{OPR}	0 to 70	°C
	Industrial	T _{OPR}	-40 to 85	°C
Storage Temperature Range Under Bias		T _{BIAS}	-10 to 85	°C

*Notes : Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING CONDITIONS at 3.3V I/O(0°C ≤ T_A ≤ 70°C)

PARAMETER	SYMBOL	MIN	Typ.	MAX	UNIT
Supply Voltage	V _{DD}	3.135	3.3	3.465	V
	V _{DDQ}	3.135	3.3	3.465	V
Ground	V _{SS}	0	0	0	V

OPERATING CONDITIONS at 2.5V I/O(0°C ≤ T_A ≤ 70°C)

PARAMETER	SYMBOL	MIN	Typ.	MAX	UNIT
Supply Voltage	V _{DD}	3.135	3.3	3.465	V
	V _{DDQ}	2.375	2.5	2.9	V
Ground	V _{SS}	0	0	0	V

CAPACITANCE*(T_A=25°C, f=1MHz)

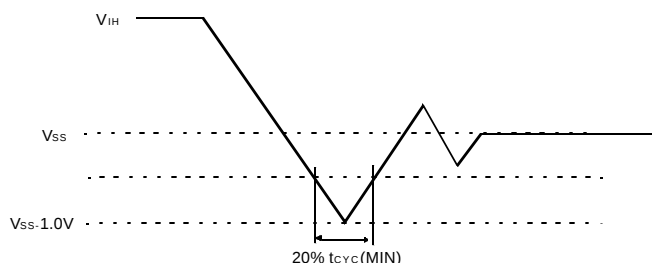
Parameter	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C _{IN}	V _{IN} =0V	-	5	pF
Output Capacitance	C _{OUT}	V _{OUT} =0V	-	7	pF

*Notes : Sampled not 100% tested.

DC ELECTRICAL CHARACTERISTICS($V_{DD}=3.3V+0.165V/-0.165V$, $T_A=0^{\circ}C$ to $+70^{\circ}C$)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNIT	NOTES
Input Leakage Current(except ZZ)	I _{IL}	$V_{DD}=Max$; $V_{IN}=V_{SS}$ to V_{DD}	-2	+2	μA	
Output Leakage Current	I _{OL}	Output Disabled, $V_{out}=V_{SS}$ to V_{DDQ}	-2	+2	μA	
Operating Current	I _{CC}	Device Selected, I _{OUT} =0mA, ZZ≤V _{IL} , Cycle Time ≥ t _{cyc} Min	-25	-	440	mA 1,2
			-22	-	400	
			-20	-	370	
Standby Current	I _{SB}	Device deselected, I _{OUT} =0mA, ZZ≤V _{IL} , f=Max, All Inputs≤0.2V or ≥ V _{DD} -0.2V	-25	-	120	mA
			-22	-	110	
			-20	-	100	
	I _{SB1}	Device deselected, I _{OUT} =0mA, ZZ≤0.2V, f=0, All Inputs=fixed (V _{DD} -0.2V or 0.2V)	-	70	mA	
	I _{SB2}	Device deselected, I _{OUT} =0mA, ZZ≥V _{DD} -0.2V, f=Max, All Inputs≤V _{IL} or ≥V _{IH}	-	60	mA	
Output Low Voltage(3.3V I/O)	V _{OL}	I _{OL} =8.0mA	-	0.4	V	
Output High Voltage(3.3V I/O)	V _{OH}	I _{OH} =-4.0mA	2.4	-	V	
Output Low Voltage(2.5V I/O)	V _{OL}	I _{OL} =1.0mA	-	0.4	V	
Output High Voltage(2.5V I/O)	V _{OH}	I _{OH} =-1.0mA	2.0	-	V	
Input Low Voltage(3.3V I/O)	V _{IL}		-0.3*	0.8	V	
Input High Voltage(3.3V I/O)	V _{IH}		2.0	V _{DD} +0.3**	V	3
Input Low Voltage(2.5V I/O)	V _{IL}		-0.3*	0.7	V	
Input High Voltage(2.5V I/O)	V _{IH}		1.7	V _{DD} +0.3**	V	3

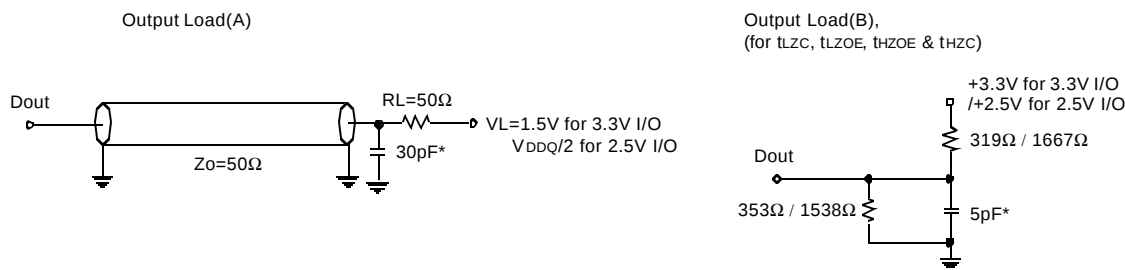
Notes : 1. Reference AC Operating Conditions and Characteristics for input and timing.
2. Data states are all zero.
3. In Case of I/O Pins, the Max. V_{IH}=V_{DDQ}+0.3V



TEST CONDITIONS

($V_{DD}=3.3V+0.165V/-0.165V$, $V_{DDQ}=3.3V+0.165V/-0.165V$ or $V_{DD}=3.3V+0.165V/-0.165V$, $V_{DDQ}=2.5V+0.4V/-0.125V$, $T_A=0$ to $70^{\circ}C$)

PARAMETER	VALUE
Input Pulse Level(for 3.3V I/O)	0 to 3.0V
Input Pulse Level(for 2.5V I/O)	0 to 2.5V
Input Rise and Fall Time(Measured at 20% to 80% for 3.3V I/O)	1.0V/ns
Input Rise and Fall Time(Measured at 20% to 80% for 2.5V I/O)	1.0V/ns
Input and Output Timing Reference Levels for 3.3V I/O	1.5V
Input and Output Timing Reference Levels for 2.5V I/O	V _{DDQ} /2
Output Load	See Fig. 1



* Including Scope and Jig Capacitance

Fig. 1

AC TIMING CHARACTERISTICS(VDD=3.3V+0.165V/-0.165V, TA=0 to 70°C)

PARAMETER	SYMBOL	-25		-22		-20		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Cycle Time	tCYC	4.0	-	4.4	-	5.0	-	ns
Clock Access Time	tCD	-	2.6	-	2.8	-	3.2	ns
Output Enable to Data Valid	tOE	-	2.6	-	2.8	-	3.2	ns
Clock High to Output Low-Z	tLZC	0.8	-	1.0	-	1.0	-	ns
Output Hold from Clock High	tOH	0.8	-	1.0	-	1.0	-	ns
Output Enable Low to Output Low-Z	tLZOE	0	-	0	-	0	-	ns
Output Enable High to Output High-Z	tHZOE	-	2.6	-	2.8	-	3.0	ns
Clock High to Output High-Z	tHZC	-	2.6	-	2.8	-	3.0	ns
Clock High Pulse Width	tCH	1.7	-	2.0	-	2.0	-	ns
Clock Low Pulse Width	tCL	1.7	-	2.0	-	2.0	-	ns
Address Setup to Clock High	tAS	1.2	-	1.4	-	1.4	-	ns
CKE Setup to Clock High	tCES	1.2	-	1.4	-	1.4	-	ns
Data Setup to Clock High	tDS	1.2	-	1.4	-	1.4	-	ns
Write Setup to Clock High (WE, BWx)	tWS	1.2	-	1.4	-	1.4	-	ns
Address Advance Setup to Clock High	tADVS	1.2	-	1.4	-	1.4	-	ns
Chip Select Setup to Clock High	tCSS	1.2	-	1.4	-	1.4	-	ns
Address Hold from Clock High	tAH	0.3	-	0.4	-	0.4	-	ns
CKE Hold from Clock High	tCEH	0.3	-	0.4	-	0.4	-	ns
Data Hold from Clock High	tDH	0.3	-	0.4	-	0.4	-	ns
Write Hold from Clock High (WE, BWEx)	tWH	0.3	-	0.4	-	0.4	-	ns
Address Advance Hold from Clock High	tADVH	0.3	-	0.4	-	0.4	-	ns
Chip Select Hold from Clock High	tCSH	0.3	-	0.4	-	0.4	-	ns
ZZ High to Power Down	tPDS	2	-	2	-	2	-	cycle
ZZ Low to Power Up	tPUS	2	-	2	-	2	-	cycle

Notes : 1. All address inputs must meet the specified setup and hold times for all rising clock(CLK) edges when ADV is sampled low and CS is sampled low. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.
2. Chip selects must be valid at each rising edge of CLK(when ADV is Low) to remain enabled.
3. A write cycle is defined by WE low having been registered into the device at ADV Low. A Read cycle is defined by WE High with ADV Low. Both cases must meet setup and hold times.
4. To avoid bus contention, At a given voltage and temperature tLZC is more than tHZC.
The specs as shown do not imply bus contention because tLZC is a Min. parameter that is worst case at totally different test conditions (0°C,3.465V) than tHZC, which is a Max. parameter(worst case at 70°C,3.135V)
It is not possible for two SRAMs on the same board to be at such different voltage and temperature.

SLEEP MODE

SLEEP MODE is a low current, power-down mode in which the device is deselected and current is reduced to I_{SB2} . The duration of SLEEP MODE is dictated by the length of time the ZZ is in a High state.

After entering SLEEP MODE, all inputs except ZZ become disabled and all outputs go to High-Z.

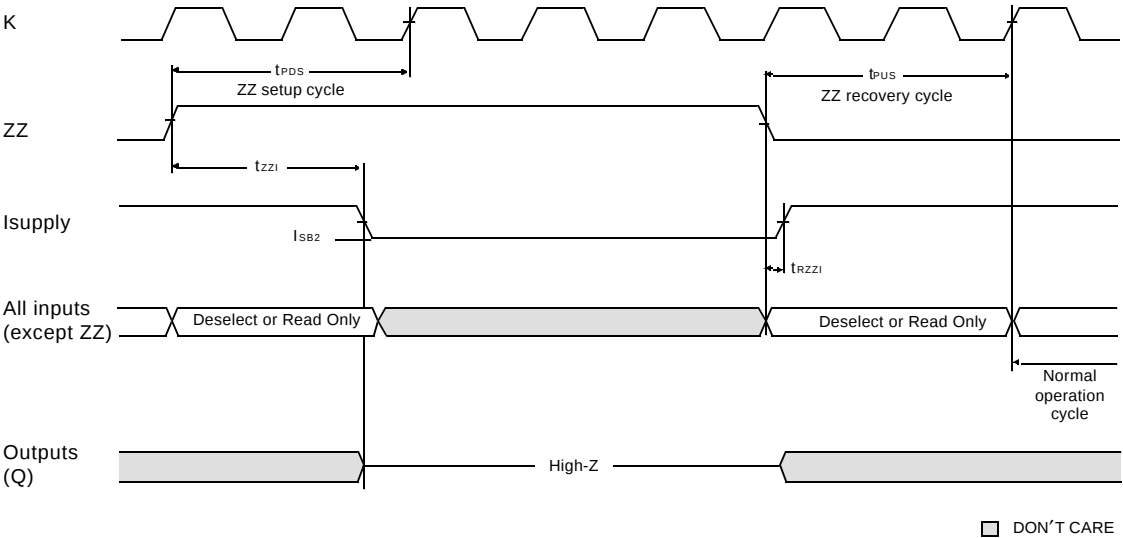
The ZZ pin is an asynchronous, active high input that causes the device to enter SLEEP MODE.

When the ZZ pin becomes a logic High, I_{SB2} is guaranteed after the time t_{ZZI} is met. Any operation pending when entering SLEEP MODE is not guaranteed to successful complete. Therefore, SLEEP MODE (READ or WRITE) must not be initiated until valid pending operations are completed. Similarly, when exiting SLEEP MODE during t_{PUS} , only a DESELECT or READ cycle should be given while the SRAM is transitioning out of SLEEP MODE.

SLEEP MODE ELECTRICAL CHARACTERISTICS

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS
Current during SLEEP MODE	$ZZ \geq V_{IH}$	I_{SB2}		10	mA
ZZ active to input ignored		t_{PDS}	2		cycle
ZZ inactive to input sampled		t_{PUS}	2		cycle
ZZ active to SLEEP current		t_{ZZI}		2	cycle
ZZ inactive to exit SLEEP current		t_{RZZI}	0		

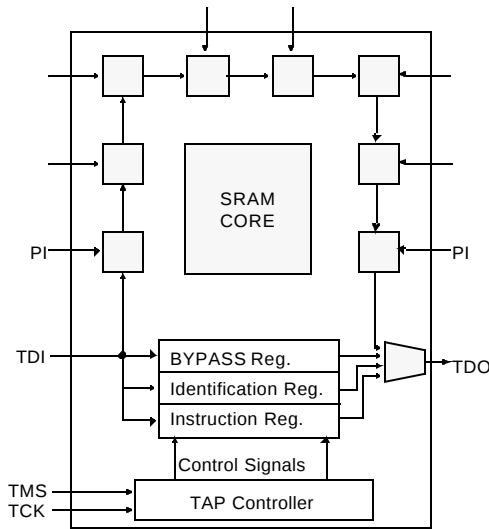
SLEEP MODE WAVEFORM



IEEE 1149.1 TEST ACCESS PORT AND BOUNDARY SCAN-JTAG

This part contains an IEEE standard 1149.1 Compatible Test Access Port (TAP). The package pads are monitored by the Serial Scan circuitry when in test mode. This is to support connectivity testing during manufacturing and system diagnostics. Internal data is not driven out of the SRAM under JTAG control. In conformance with IEEE 1149.1, the SRAM contains a TAP controller, Instruction Register, Bypass Register and ID register. The TAP controller has a standard 16-state machine that resets internally upon power-up, therefore, TRST signal is not required. It is possible to use this device without utilizing the TAP. To disable the TAP controller without interfacing with normal operation of the SRAM, TCK must be tied to Vss to preclude mid level input. TMS and TDI are designed so an undriven input will produce a response identical to the application of a logic 1, and may be left unconnected. But they may also be tied to VDD through a resistor. TDO should be left unconnected.

JTAG Block Diagram



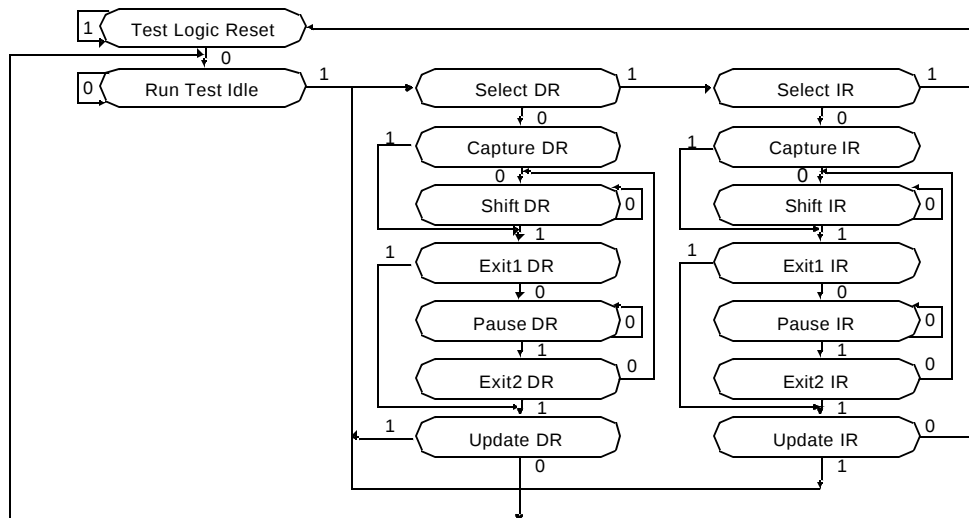
JTAG Instruction Coding

IR2	IR1	IR0	Instruction	TDO Output	Notes
0	0	0	SAMPLE-Z	Boundary Scan Register	1
0	0	1	IDCODE	Identification Register	2
0	1	0	SAMPLE-Z	Boundary Scan Register	1
0	1	1	BYPASS	Bypass Register	3
1	0	0	SAMPLE	Boundary Scan Register	4
1	0	1	BYPASS	Bypass Register	3
1	1	0	BYPASS	Bypass Register	3
1	1	1	BYPASS	Bypass Register	3

NOTE :

1. Places DQs in Hi-Z in order to sample all input data regardless of other SRAM inputs.
2. TDI is sampled as an input to the first ID register to allow for the serial shift of the external TDI data.
3. Bypass register is initiated to Vss when BYPASS instruction is invoked. The Bypass Register also holds serially loaded TDI when exiting the Shift DR states.
4. SAMPLE instruction dose not places DQs in Hi-Z.

TAP Controller State Diagram



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SCAN REGISTER DEFINITION

Part	Instruction Register	Bypass Register	ID Register	Boundary Scan
512Kx36	3 bits	1 bits	32 bits	75 bits
1Mx18	3 bits	1 bits	32 bits	75 bits

ID REGISTER DEFINITION

Part	Revision Number (31:28)	Part Configuration (27:18)	Vendor Definition (17:12)	Samsung JEDEC Code (11: 1)	Start Bit(0)
512Kx36	0000	00111 00100	XXXXXX	00001001110	1
1Mx18	0000	01000 00011	XXXXXX	00001001110	1

119BGA BOUNDARY SCAN EXIT ORDER(x36)

1	2T	NC		CLK	4K	39
2	1R	NC		A	4G	40
3	4T	A		ADV	4B	41
4	4H	WE		A	4A	42
5	5R	NC		CKE	4M	43
6	5T	A		BWc	3G	44
7	5L	BW _a		A	3B	45
8	7R	NC		A	3A	46
9	6R	A		CS2	2B	47
10	7T	ZZ		CS1	4E	48
11	6P	DQPa		A	3C	49
12	7N	DQa		A	2C	50
13	6M	DQa		A	2A	51
14	7L	DQa		DQPc	2D	52
15	6K	DQa		DQc	1E	53
16	7P	DQa		DQc	2F	54
17	6N	DQa		DQc	1G	55
18	6L	DQa		DQc	2H	56
19	7K	DQa		DQc	1D	57
20	5J	NC		DQc	2E	58
21	6H	DQb		DQc	2G	59
22	7G	DQb		DQc	1H	60
23	6F	DQb		DQd	2K	61
24	7E	DQb		DQd	1L	62
25	7D	DQb		DQd	2M	63
26	7H	DQb		DQd	1N	64
27	6G	DQb		DQd	1P	65
28	6E	DQb		DQd	1K	66
29	6D	DQPb		DQd	2L	67
30	7B	NC		DQd	2N	68
31	6C	A		DQPd	2P	69
32	5C	A		BW _d	3L	70
33	6A	A		LBO	3R	71
34	5B	A		A	2R	72
35	5A	A		A	3T	73
36	4F	OE		A1	4N	74
37	5G	BW _b		A0	4P	75
38	6B	CS2				

119BGA BOUNDARY SCAN EXIT ORDER(x18)

1	2T	A		CLK	4K	39
2	1R	NC		A	4G	40
3	6T	A		ADV	4B	41
4	4H	WE		A	4A	42
5	5R	NC		CKE	4M	43
6	5T	A		BW _b	3G	44
7	5L	BW _a		A	3B	45
8	7R	NC		A	3A	46
9	6R	A		CS2	2B	47
10	7T	ZZ		CS1	4E	48
11	6P	NC		A	3C	49
12	7N	NC		A	2C	50
13	6M	NC		A	2A	51
14	7L	NC		NC	2D	52
15	6K	NC		NC	1E	53
16	7P	DQa		NC	2F	54
17	6N	DQa		NC	1G	55
18	6L	DQa		NC	2H	56
19	7K	DQa		DQb	1D	57
20	5J	NC		DQb	2E	58
21	6H	DQa		DQb	2G	59
22	7G	DQa		DQb	1H	60
23	6F	DQa		DQb	2K	61
24	7E	DQa		DQb	1L	62
25	6D	DQPa		DQb	2M	63
26	7H	NC		DQb	1N	64
27	6G	NC		DQPb	2P	65
28	6E	NC		NC	1K	66
29	7D	NC		NC	2L	67
30	7B	NC		NC	2N	68
31	6C	A		NC	1P	69
32	5C	A		NC	3L	70
33	6A	A		LBO	3R	71
34	5B	A		A	2R	72
35	5A	A		A	3T	73
36	4F	OE		A1	4N	74
37	5G	NC		A0	4P	75
38	6B	CS2				

NOTE, NC ; Don't Care

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K7N161809A

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165FBGA BOUNDARY SCAN EXIT ORDER(x36)

1	1R	$\overline{\text{LBO}}$		CLK	6B	39
2	6N	NC		NC	11B	40
3	11P	NC		NC	1A	41
4	8P	A		$\overline{\text{CS2}}$	6A	42
5	8R	A		$\overline{\text{BWa}}$	5B	43
6	9R	A		$\overline{\text{BWb}}$	5A	44
7	9P	A		$\overline{\text{BWc}}$	4A	45
8	10P	A		$\overline{\text{BWd}}$	4B	46
9	10R	A		CS2	3B	47
10	11R	A		$\overline{\text{CS1}}$	3A	48
11	11H	ZZ		A	2A	49
12	11N	DQa		A	2B	50
13	11M	DQa		NC	1B	51
14	11L	DQa		DQc	1C	52
15	11K	DQa		DQc	1D	53
16	11J	DQa		DQc	1E	54
17	10M	DQa		DQc	1F	55
18	10L	DQa		DQc	1G	56
19	10K	DQa		DQc	2D	57
20	10J	DQa		DQc	2E	58
21	11G	DQb		DQc	2F	59
22	11F	DQb		DQc	2G	60
23	11E	DQb		DQd	1J	61
24	11D	DQb		DQd	1K	62
25	10G	DQb		DQd	1L	63
26	10F	DQb		DQd	1M	64
27	10E	DQb		DQd	2J	65
28	10D	DQb		DQd	2K	66
29	11C	DQb		DQd	2L	67
30	11A	NC		DQd	2M	68
31	10A	A		DQd	1N	69
32	10B	A		A	3P	70
33	9A	A		A	3R	71
34	9B	A		A	4R	72
35	8A	ADV		A	4P	73
36	8B	$\overline{\text{OE}}$		A1	6P	74
37	7A	$\overline{\text{CKE}}$		A0	6R	75
38	7B	$\overline{\text{WE}}$				

165FBGA BOUNDARY SCAN EXIT ORDER(x18)

1	1R	$\overline{\text{LBO}}$		CLK	6B	39
2	6N	NC		NC	11B	40
3	11P	NC		NC	1A	41
4	8P	A		$\overline{\text{CS2}}$	6A	42
5	8R	A		$\overline{\text{BWa}}$	5B	43
6	9R	A		$\overline{\text{NC}}$	5A	44
7	9P	A		$\overline{\text{BWb}}$	4A	45
8	10P	A		$\overline{\text{NC}}$	4B	46
9	10R	A		CS2	3B	47
10	11R	A		$\overline{\text{CS1}}$	3A	48
11	11H	ZZ		A	2A	49
12	11N	NC		A	2B	50
13	11M	NC		NC	1B	51
14	11L	NC		NC	1C	52
15	11K	NC		NC	1D	53
16	11J	NC		NC	1E	54
17	10M	DQa		NC	1F	55
18	10L	DQa		NC	1G	56
19	10K	DQa		DQb	2D	57
20	10J	DQa		DQb	2E	58
21	11G	DQb		DQb	2F	59
22	11F	DQb		DQb	2G	60
23	11E	DQb		DQb	1J	61
24	11D	DQb		DQb	1K	62
25	11C	DQb		DQb	1L	63
26	10F	NC		DQb	1M	64
27	10E	NC		DQb	1N	65
28	10D	NC		NC	2K	66
29	10G	NC		NC	2L	67
30	11A	A		NC	2M	68
31	10A	A		NC	2J	69
32	10B	A		A	3P	70
33	9A	A		A	3R	71
34	9B	A		A	4R	72
35	8A	ADV		A	4P	73
36	8B	$\overline{\text{OE}}$		A1	6P	74
37	7A	$\overline{\text{CKE}}$		A0	6R	75
38	7B	$\overline{\text{WE}}$				

NOTE, NC ; Don't Care

JTAG DC OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Note
Power Supply Voltage	V _{DD}	3.135	3.3	3.465	V	
Input High Level (3.3V I/O / 2.5V I/O)	V _{IH}	2.0 / 1.7	-	V _{DD} +0.3	V	1
Input Low Level (3.3V I/O / 2.5V I/O)	V _{IL}	-0.3	-	0.8 / 0.7	V	
Output High Voltage(3.3V I/O / 2.5V I/O)	V _{OH}	2.4 / 2.0	-	-	V	
Output Low Voltage(3.3V I/O / 2.5V I/O)	V _{OL}	-	-	0.4 / 0.4	V	

NOTE : The input level of SRAM pin is to follow the SRAM DC specification.

1. In Case of I/O Pins, the Max. V_{IH}=V_{DDQ}+0.3V.

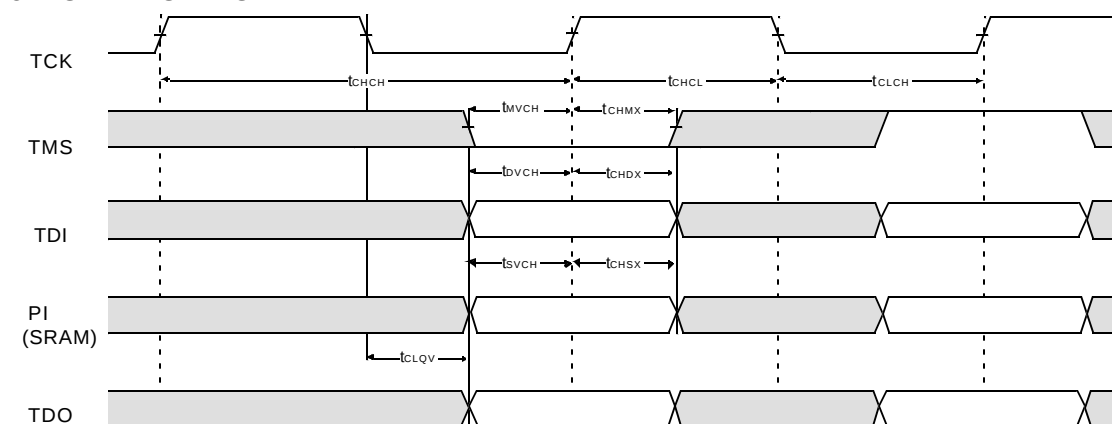
JTAG AC TEST CONDITIONS

Parameter	Symbol	Min	Unit	Note
Input High/Low Level(3.3V I/O , 2.5V I/O)	V _{IH} /V _{IL}	3.0/0 , 2.5/0	V	
Input Rise/Fall Time(3.3V I/O , 2.5V I/O)	TR/TF	1.0/1.0 , 1.0/1.0	ns	
Input and Output Timing Reference Level		V _{DDQ} /2	V	

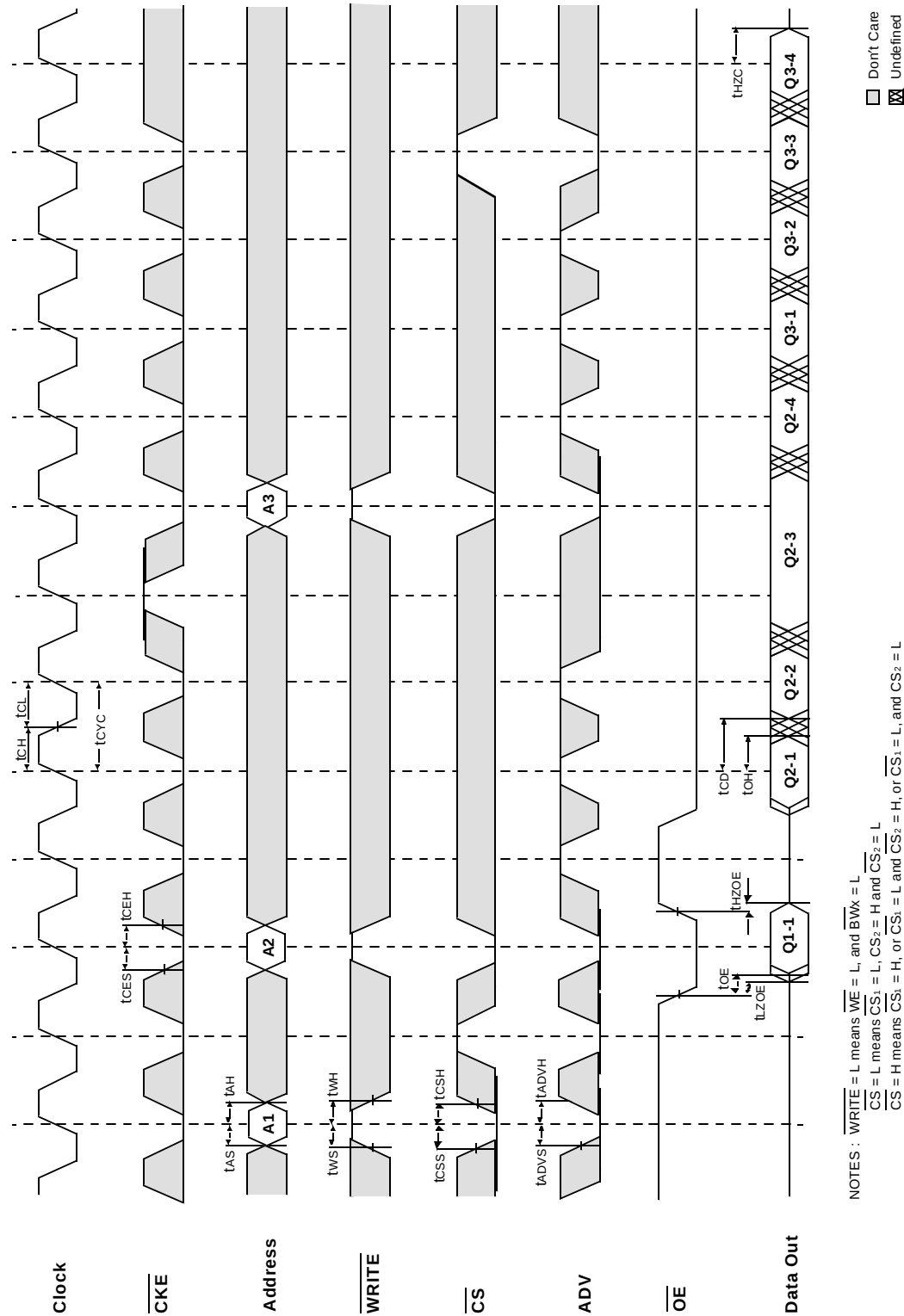
JTAG AC Characteristics

Parameter	Symbol	Min	Max	Unit	Note
TCK Cycle Time	t _{CHCH}	50	-	ns	
TCK High Pulse Width	t _{CHCL}	20	-	ns	
TCK Low Pulse Width	t _{CLCH}	20	-	ns	
TMS Input Setup Time	t _{MVCH}	5	-	ns	
TMS Input Hold Time	t _{CHMX}	5	-	ns	
TDI Input Setup Time	t _{DVCH}	5	-	ns	
TDI Input Hold Time	t _{CHDX}	5	-	ns	
SRAM Input Setup Time	t _{SVCH}	5	-	ns	
SRAM Input Hold Time	t _{CHSX}	5	-	ns	
Clock Low to Output Valid	t _{CLQV}	0	10	ns	

JTAG TIMING DIAGRAM



TIMING WAVEFORM OF READ CYCLE

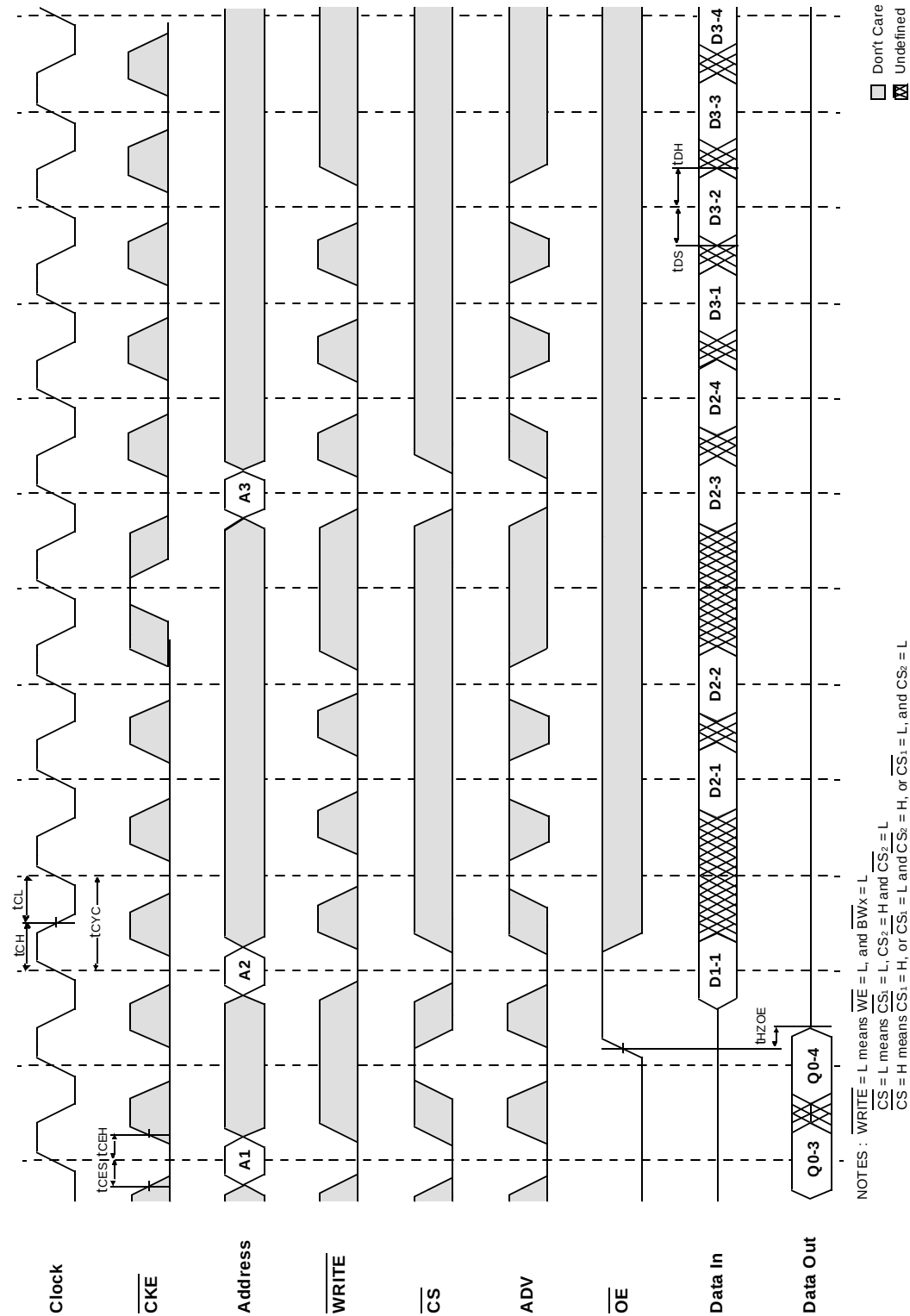


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TIMING WAVEFORM OF WRTE CYCLE

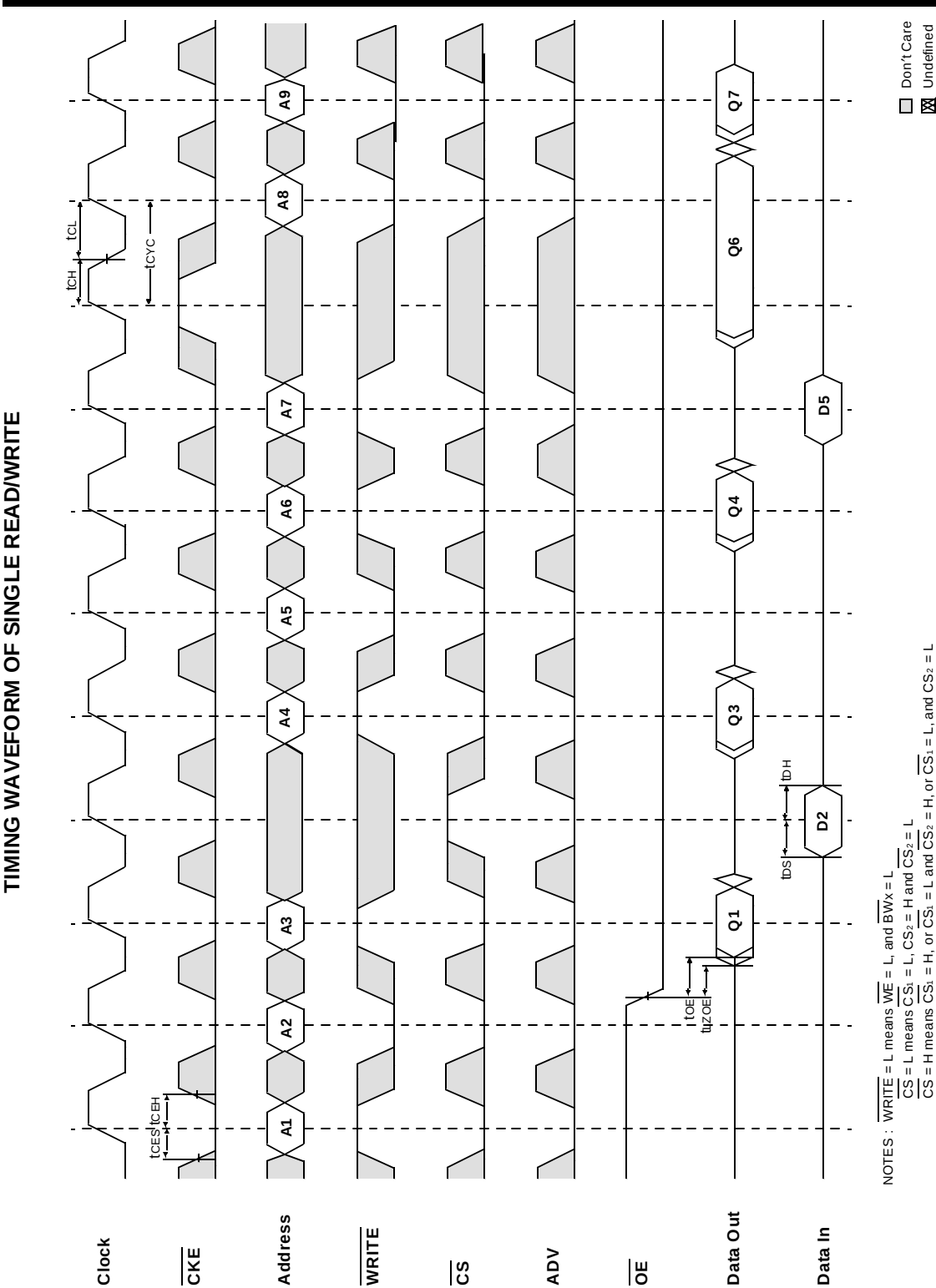


NOTES : $\overline{WRITE} = L$ means $\overline{WE} = L$, and $\overline{BWx} = L$
 $\overline{CS} = L$ means $\overline{CS_1} = L$, $\overline{CS_2} = H$ and $\overline{CS_2} = L$
 $\overline{CS} = H$ means $\overline{CS_1} = H$, or $\overline{CS_1} = L$ and $\overline{CS_2} = H$, or $\overline{CS_1} = L$, and $\overline{CS_2} = L$

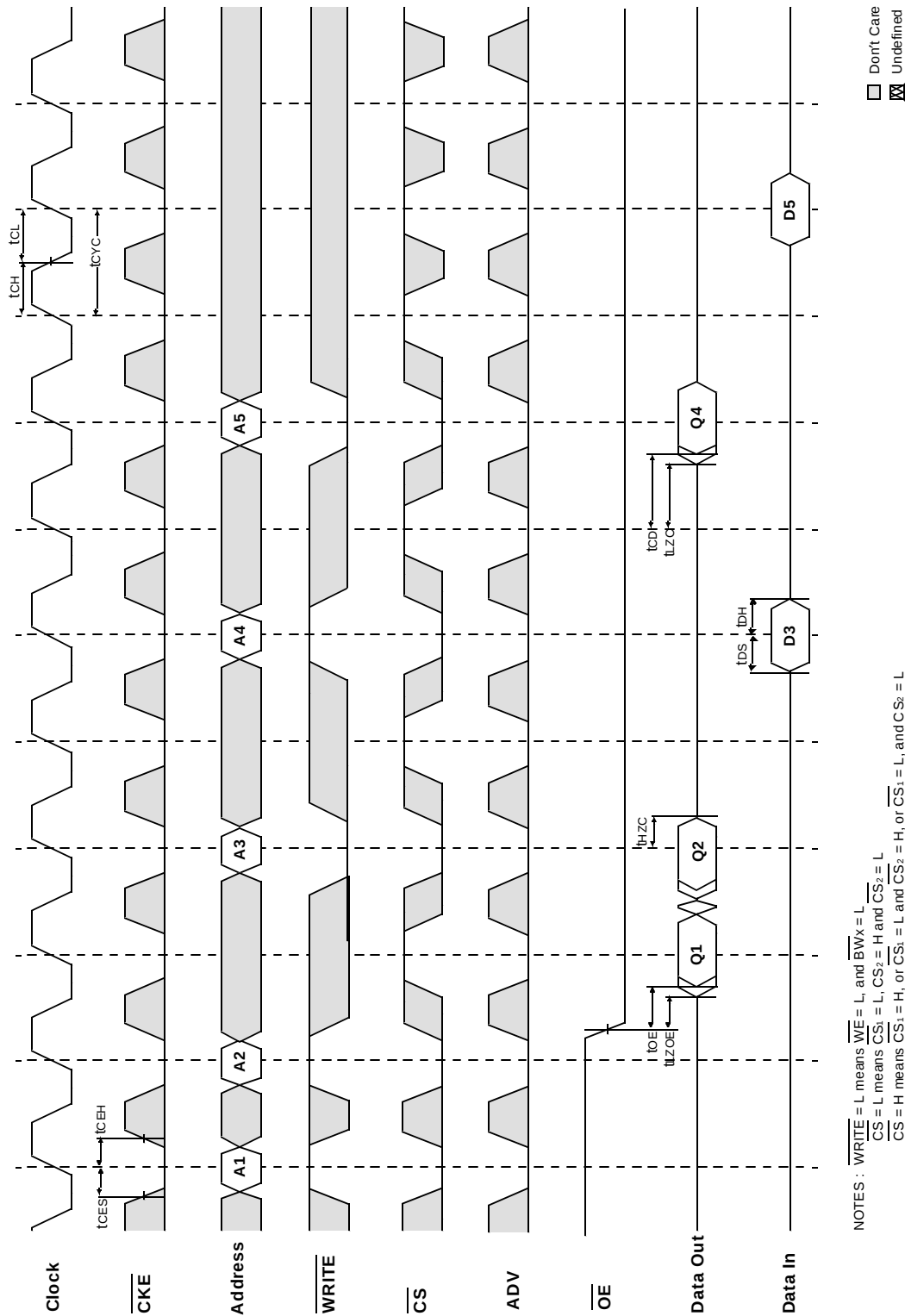
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TIMING WAVEFORM OF CS OPERATION



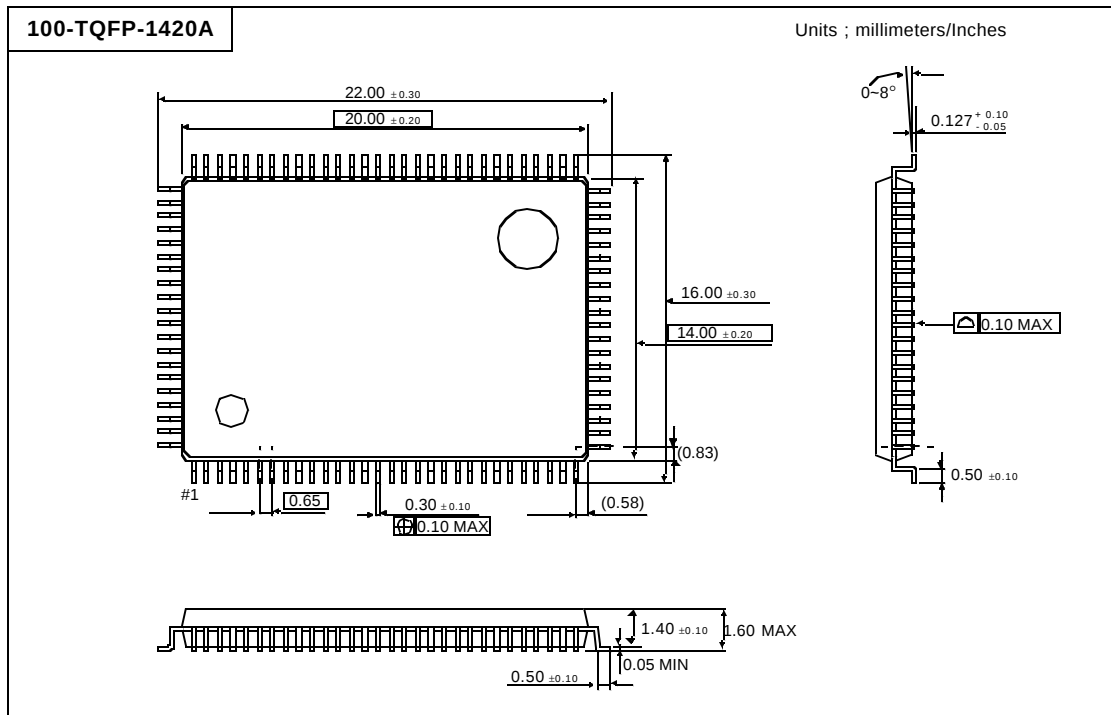
NOTES : $\overline{WRITE} = L$ means $\overline{WE} = L$, and $\overline{BWx} = L$
 $\overline{CS} = L$ means $\overline{CS_1} = L$, $\overline{CS_2} = H$ and $\overline{CS_2} = L$
 $\overline{CS} = H$ means $\overline{CS_1} = H$, or $\overline{CS_1} = L$ and $\overline{CS_2} = H$, or $\overline{CS_1} = L$, and $\overline{CS_2} = L$

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PACKAGE DIMENSIONS

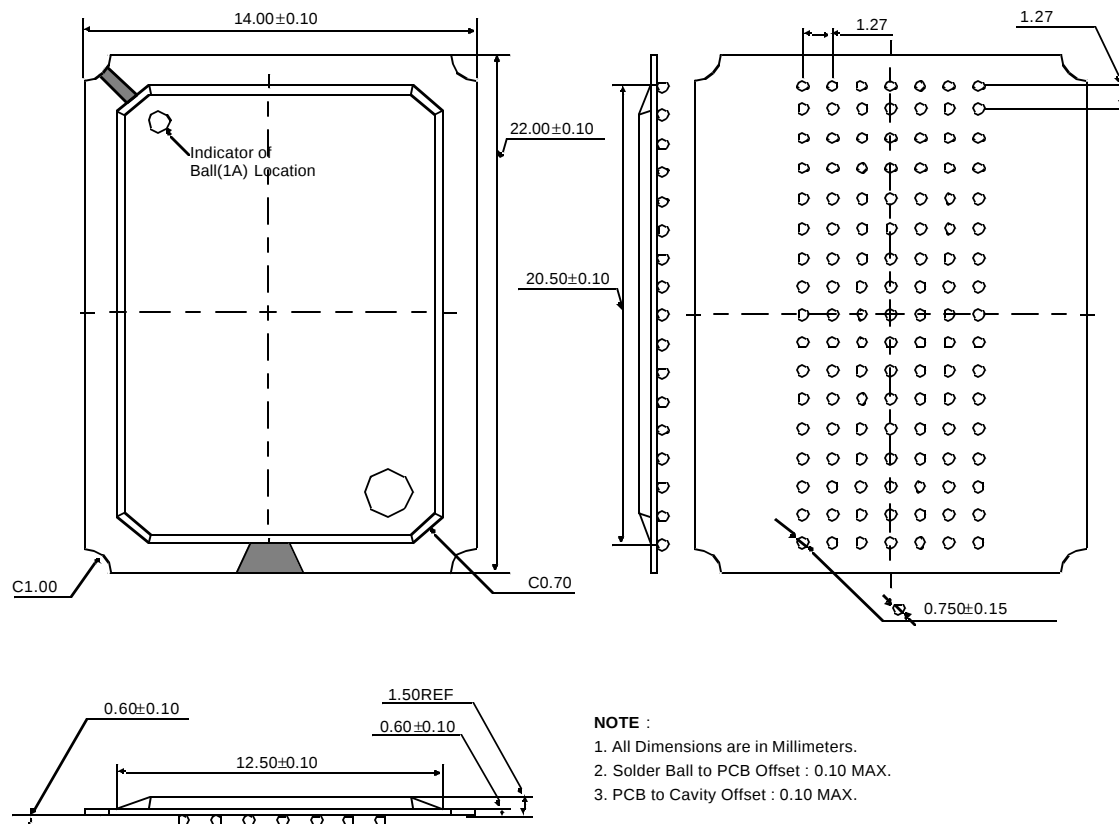


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119BGA PACKAGE DIMENSIONS



NOTE :

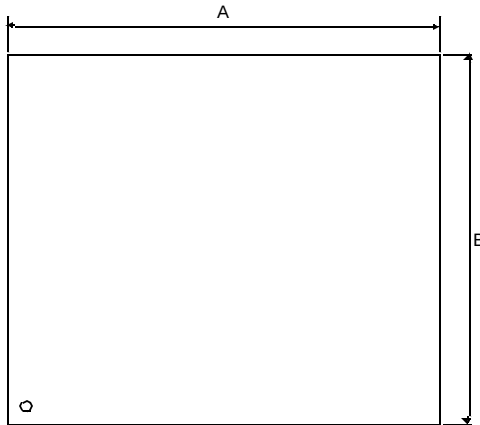
1. All Dimensions are in Millimeters.
2. Solder Ball to PCB Offset : 0.10 MAX.
3. PCB to Cavity Offset : 0.10 MAX.

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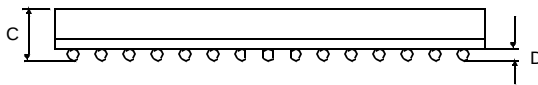
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165 FBGA PACKAGE DIMENSIONS

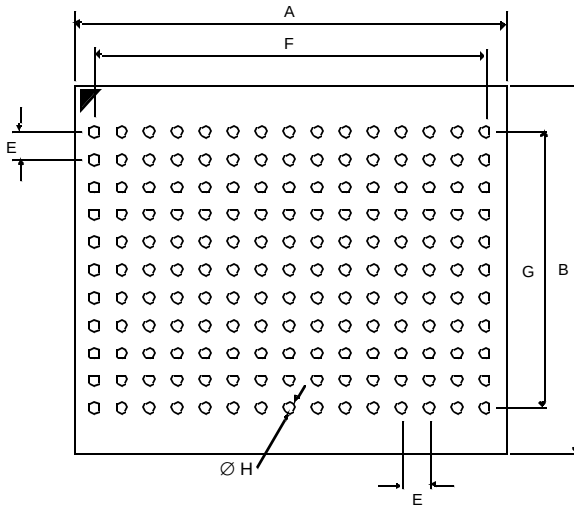
13mm x 15mm Body, 1.0mm Bump Pitch, 11x15 Ball Array



Top View



Side View



Bottom View

Symbol	Value	Units	Note	Symbol	Value	Units	Note
A	15 ± 0.1	mm		E	1.0	mm	
B	13 ± 0.1	mm		F	14.0	mm	
C	1.3 ± 0.1	mm		G	10.0	mm	
D	0.35 ± 0.05	mm		H	0.45 ± 0.05	mm	