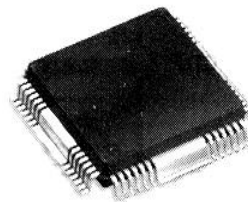


SPINDLE & VOICE COIL MOTOR ONE CHIP DRIVER

The KA3121 is a monolithic IC and an one-chip IC which is spindle motor driver, voice coil motor driver for the HDD motors. includes the following functions: retract and power management.

The spindle motor condition is monitored by the Ready output and the motor speed control is accomplished by internal PLL. The external digital ASIC controls the voice coil motor current via PWMH and PWML inputs and the power management circuit always monitors the power supply voltages.

48-QFPH-1414



FEATURES

SPINDLE MOTOR DRIVE PART

- Hard / soft switching
- Spindle motor brake after retract
- Adjustable brake delay time
- 2.0A maximum current capability
- Low output saturation voltage: 1V typical @1.6A using vertical PNP high side.
- Soft switching generator for soft switching
- Back EMF processing for sensorless motor commutation

ORDERING INFORMATION

Device	Package	Operating Temperature
KA3121	48-QFPH-1414	0 ~ 70°C

VOICE COIL MOTOR DRIVE PART

- Trimmed low offset current
- 1.2A maximum current capability
- Programmable seek and tracking following mode with adjustable current loop gain
- Automatic power down retract function
- Linear class AB output with low crossover distortion delay
- Low output saturation voltage: 1V typical @1.0A
- Internal full bridge with vertical PNP & NPN
- Intelligent retract (Reduced bouncing)

POWER MONITORING

- Power on reset with delay
- Hysteresis on both power comparators
- Over temperature & over current shut down
- 5V and 12V power monitor threshold accuracy $\pm 2\%$

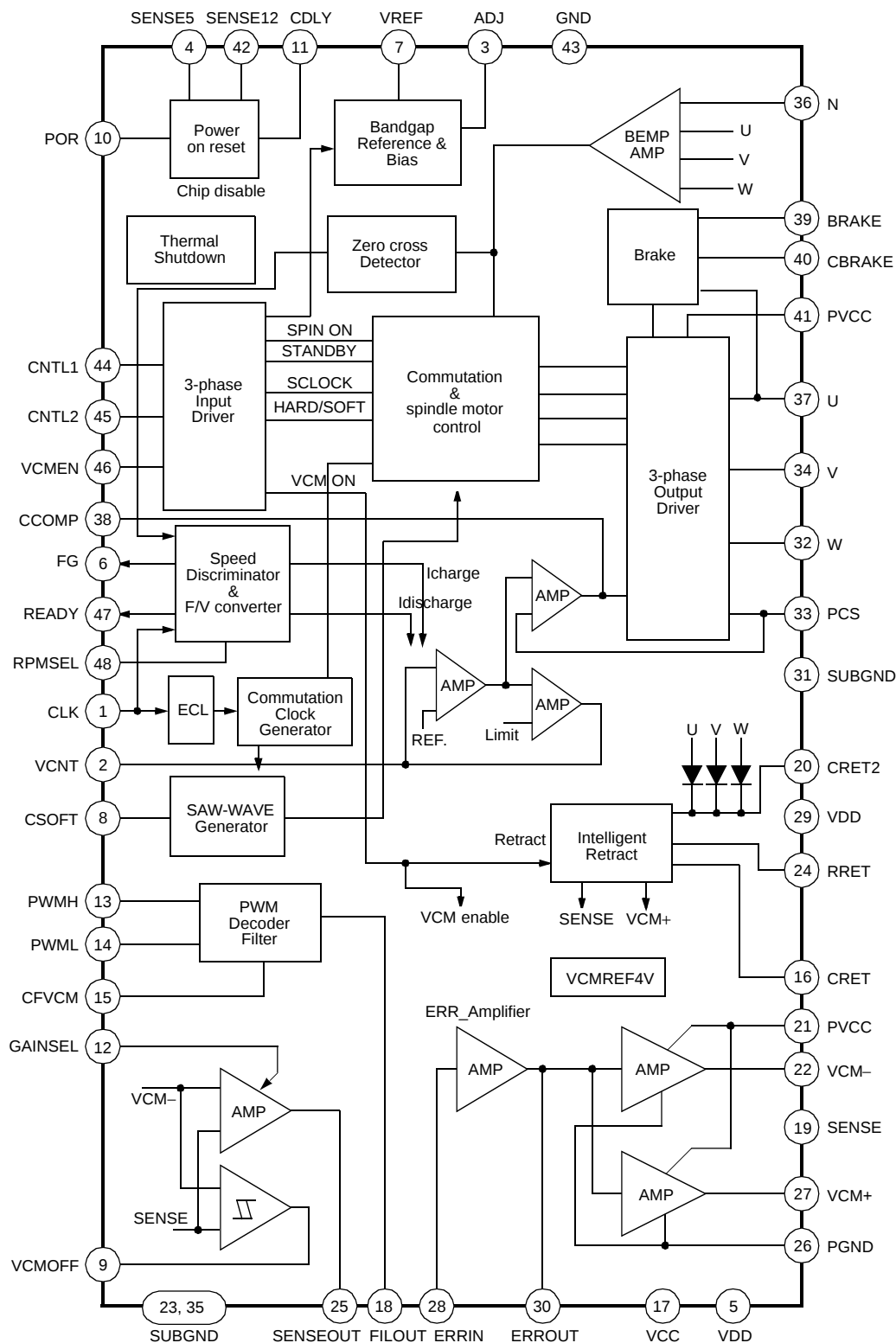
PACKAGE

- 48QFP (48 pin quad flat package heat-sink)

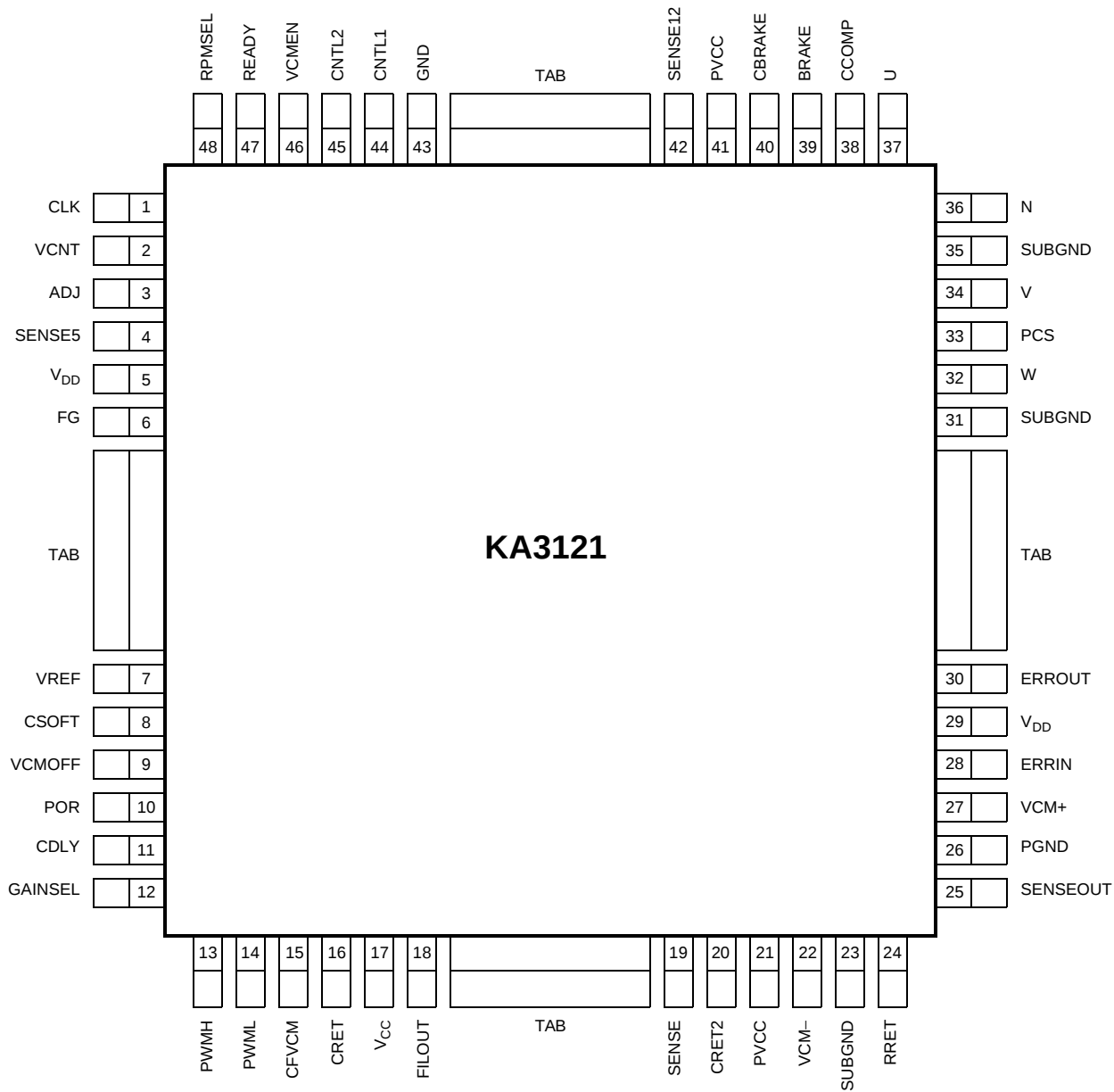
APPLICATION

- Hard disk drive (HDD) products

BLOCK DIAGRAM



PIN CONFIGURATION



PIN DESCRIPTION

Pin No.	Symbol	I/O	Description
1	CLK	I	System reference clock
2	VCNT	–	Capacitor F/V converter for speed control
3	ADJ	I	Adjustable pin of reference voltage
4	SENSE5	I	Adjustable pin for 5V power line sensing
5	V _{DD}	–	5V power line
6	FG	O	Frequency generation for spindle motor rotation speed
7	VREF	O	Reference voltage output
8	CSOFT	–	Capacitor to make wave for soft switching
9	VCMOFF	O	VCM output offset monitoring pin
10	POR	O	Power on reset output
11	CDLY	–	Power on reset delay with capacitor
12	GAINSEL	I	VCM power amplifier gain selection input
13	PWMH	I	PWM signal input (MSB) for VCM
14	PWML	I	PWM signal input (LSB) for VCM
15	CFVCM	–	Filter capacitor for VCM PWM control
16	CRET	–	Capacitor for delayed retract
17	V _{CC}	–	12V power line
18	FILOUT	O	VCM PWM output
19	SENSE	I	Sensing point to be connected to VCM sensing resistor
20	CRET2	–	Power for retract
21	PVCC	–	12V power line for VCM output
22	VCM–	–	VCM output to be connected to sensing resistor
23	SUBGND	–	VCM power transistor ISO ground
24	RRET	I	Adjustable pin for retract current set
25	SENSEOUT	O	VCM current sense amplifier output
26	PGND	–	Power ground for VCM
27	VMC+	–	VCM output to be connected to voice coil motor
28	ERRIN	I	VCM error amplifier input
29	V _{DD}	–	5V power supply
30	ERROUT	O	VCM error amplifier output pin for compensation
31	SUBGND	–	spindle motor power transistor ISO ground
32	W	O	spindle motor W-phase output

PIN DESCRIPTION (Continued)

Pin No.	Symbol	I/O	Description
33	PCS	O	Spindle motor current sensing
34	V	O	spindle motor V-phase output
35	SUBGND	–	spindle motor power transistor ISO ground
36	N	I	spindle motor neutral point
37	U	O	spindle motor U-phase drive output
38	CCOMP	–	Compensation of spindle motor output control
39	BRAKE	O	Dynamic brake pin for MOSFET drive
40	CBRAKE	–	Back-EMF charging pin for brake power
41	PVCC	–	12V power line for spindle motor output
42	SENSE12	I	Adjustable pin for 12V power line sensing
43	GND	–	Ground
44	CNTL1	I	Control input for spindle motor and brake
45	CNTL2	I	Control input for start-up clock and VCM & retract
46	VCMEN	I	VCM enable input independent of spindle motor
47	READY	O	Output of speed lock detector for SPM speed
48	RPMSEL	I	Spindle motor target RPM selection

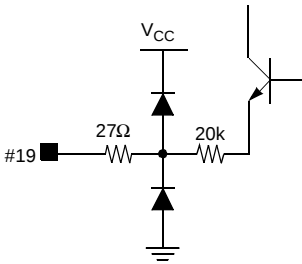
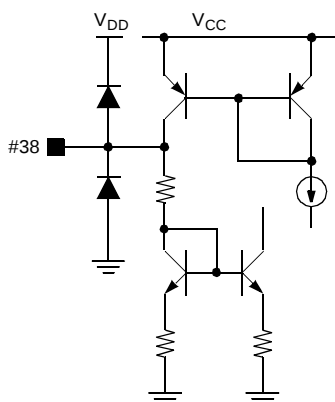
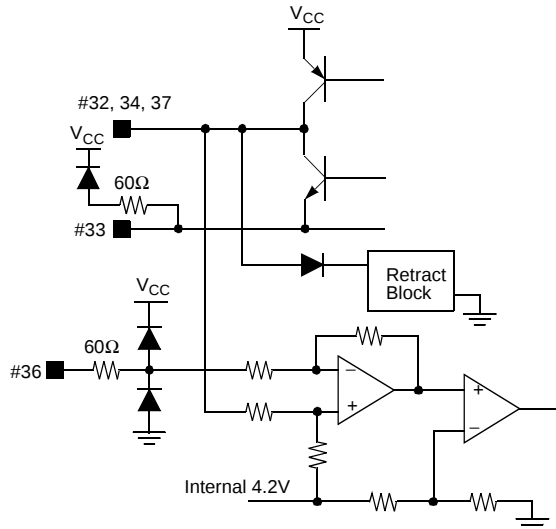
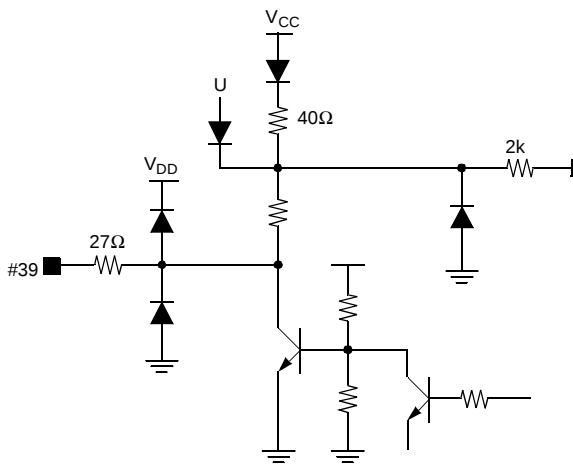
EQUIVALENT CIRCUITS

Regulator part	SENSE5 input
FG output	VCM offset compensation output
Power on reset part	VCM gain selection input

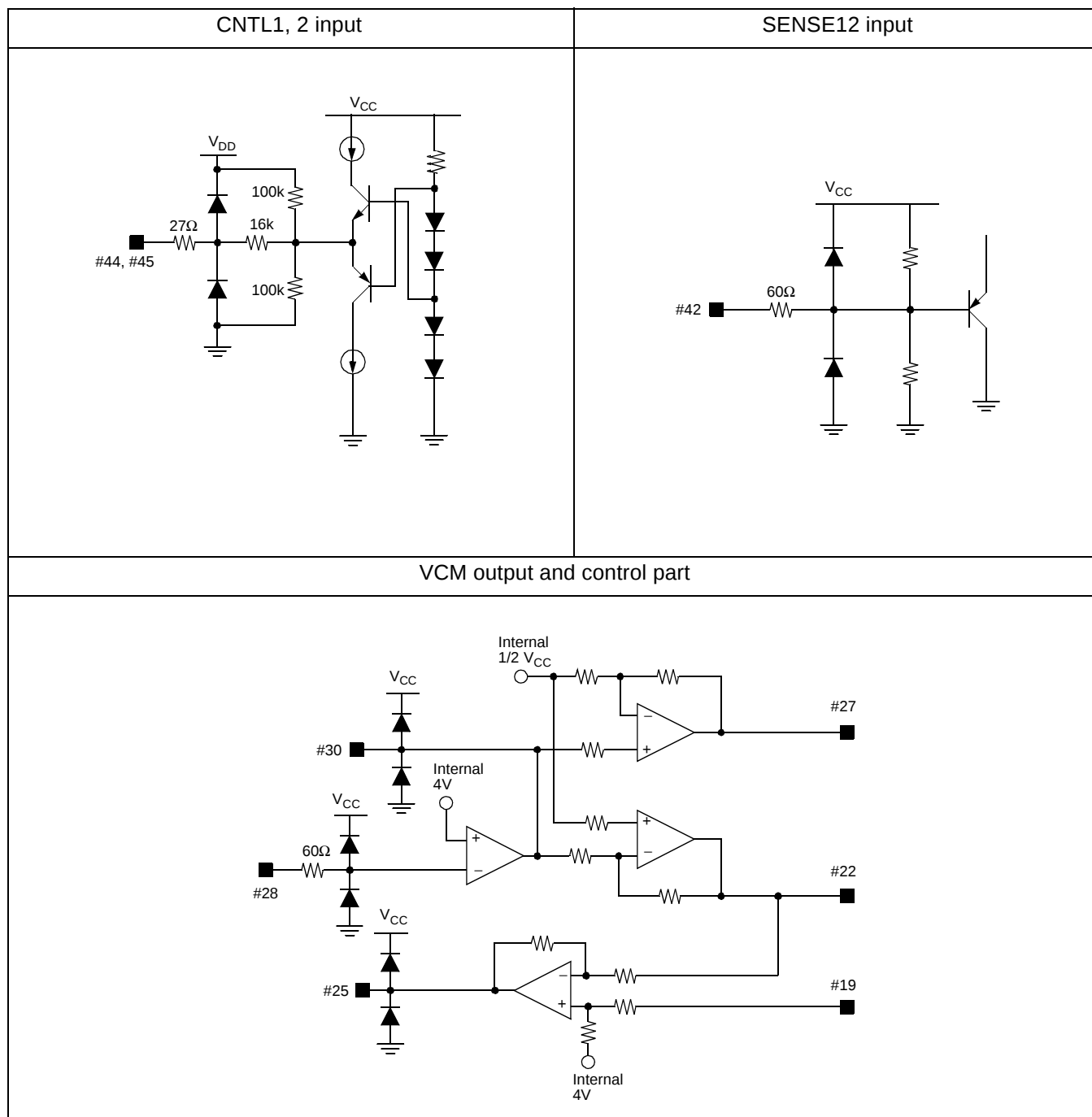
EQUIVALENT CIRCUITS (Continued)

VCM PWM high input	VCM PWM low input
VCM PWM filter Capacitor	Filtered VCM PWM command output
VCM current sense input	Capacitor for retract power

EQUIVALENT CIRCUITS (Continued)

Max. retract current set input	Spindle motor output compensation Capacitor
	
spindle motor output and Back-EMF sensing part	Dynamic brake part
	

EQUIVALENT CIRCUITS (Continued)

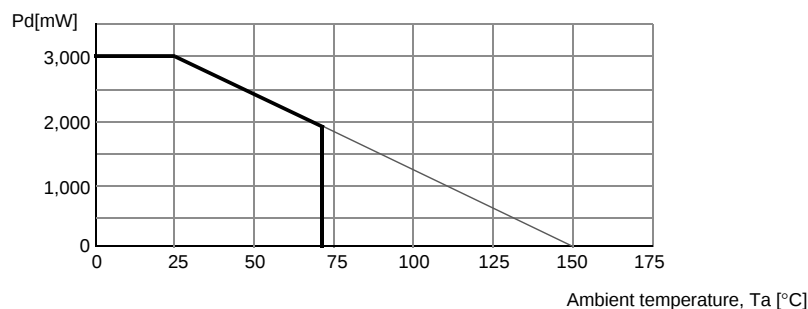


ABSOLUTE MAXIMUM RATING (Ta=25°C)

Characteristics	Symbol	Value	Unit
Maximum signal block supply voltage for 5V line	V_{DDMAX}	6	V
Maximum signal block supply voltage for 12V line	V_{CCMAX}	15	V
Maximum power block supply voltage for 12V line	PV_{CC}	15	V
Maximum output current	I_{OMAX}	2	A
Power dissipation	P_D	3.0 ^{note}	W
Storage temperature	T_{STG}	-55 ~ 125	°C
Maximum junction temperature	T_J	150	°C
Operating ambient temperature	T_A	0 ~ 70	°C

NOTE:

1. When mounted on 50mm × 50mm × 1mm PCB (Phenolic resin material)
2. Power dissipation is reduced 16mW / °C for using above Ta=25°C.
3. Do not exceed Pd and SOA.



RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{CC}, PV_{CC}	10.8	12.0	13.2	V
Supply voltage in logic part	V_{DD}	4.5	5.0	5.5	V

ELECTRICAL CHARACTERISTICS

(Ta=25°C, unless otherwise specified)

Characteristic	Symbol	Test conditions	Min.	Typ.	Max.	Unit
SUPPLY CURRENT						
5V line supply current 1	I _{DD1}	CNTL1=0V, CNTL2=0V	1	3	5	mA
5V line supply current 2	I _{DD2}	CNTL1=CNTL2=2.5V	1	3	5	mA
5V line supply current 3	I _{DD3}	CNTL1=5V, CNTL2=2.5V, VCMEN=0V	5	8	10	mA
5V line supply current 4	I _{DD4}	CNTL1=2.5V, CNTL2=0V	1	2	3	mA
12V line supply current 1	I _{CC1}	CNTL1=0V, CNTL2=0V	15	20	25	mA
12V line supply current 2	I _{CC2}	CNTL1=CNTL2=2.5V	5	8	10	mA
12V line supply current 3	I _{CC3}	CNTL1=5V, CNTL2=2.5V, VCMEN=0V	10	15	20	mA
12V line supply current 3	I _{CC4}	CNTL1=2.5V, CNTL2=0V	1	2	3	mA
POWER MONITOR						
Threshold voltage1 level for 12V	V _{TH12}	V _{CC} =Sweep, V _{DD} =5V	9.1	9.5	9.9	V
Threshold voltage2 level for 12V	V _{TH12B}	V _{CC} =Sweep, V _{DD} =5V	9.0	9.25	9.6	V
Hysteresis on 12V comparator	V _{HYS12}	V _{CC} =Sweep, V _{DD} =5V	120	240	360	mV
Adjustable pin voltage for 12V	V12	V _{CC} =12V, V _{DD} =5V	3.1	3.3	3.5	V
Threshold voltage1 level for 5V	V _{TH5}	V _{CC} =12V, V _{DD} =Sweep	4.3	4.5	4.7	V
Threshold voltage2 level for 5V	V _{TH5B}	V _{CC} =12V, V _{DD} =Sweep	4.2	4.4	4.6	V
Hysteresis on 5V comparator	V _{HYS5}	V _{CC} =12V, V _{DD} =Sweep	50	100	150	mV
Adjustable pin voltage for 5V	V5	V _{CC} =12V, V _{DD} =5V	2.75	2.9	3.05	V
POWER ON RESET GENERATOR						
Charging current for POR Capacitor	I _{CPOR}	V _{CC} =12V, V _{DD} =5V	8.5	12.5	17.0	μA
POR threshold voltage	V _{THPOR}	CDLY=Sweep	2.3	2.5	2.7	V
Output high voltage	V _{POH}	V _{CC} =12V, V _{DD} =5V	4.0	4.8	5.0	V
Output low voltage	V _{POL}	V _{CC} =12V, V _{DD} =5V	0	0.2	0.5	V

ELECTRICAL CHARACTERISTICS (Continued)

(Ta=25°C, unless otherwise specified)

Characteristic	Symbol	Test conditions	Min.	Typ.	Max.	Unit
CONTROL INPUT						
Logic control input1 MED voltage	V _{CTL10}	CNTL1=2.5V	2.3	2.5	2.7	V
Logic control input2 MED voltage	V _{CTL20}	CNTL1=2.5V	2.3	2.5	2.7	V
Logic control input1 MED current	I _{CTL10}	CNTL1=2.5V	-5	0	5	μA
Logic control input2 MED current	I _{CTL20}	CNTL1=2.5V	-5	0	5	μA
Logic control input1 high voltage	V _{CTL1H}	CNTL1=Sweep	3.4	3.8	4.2	V
Logic control input1 high current	I _{CTL1H}	CNTL1=5V	70	90	100	μA
Logic control input1 low voltage	V _{CTL1L}	CNTL1=Sweep	0.8	1.2	1.6	V
Logic control input1 low current	I _{CTL1L}	CNTL1=0V	-110	-90	-70	μA
Logic control input2 high voltage	V _{CTL2H}	CNTL2=5V	3.4	3.8	4.2	V
Logic control input2 high current	I _{CTL2H}	CNTL2=Sweep	70	90	100	μA
Logic control input2 low voltage	V _{CTL2L}	CNTL2=0V	0.8	1.2	1.6	V
Logic control input2 low current	I _{CTL2L}	CNTL3=5V	-110	-90	-70	μA
SPINDLE FG GENERATOR						
FG frequency	FG	U, V, W=120° shift pulse	2.9	3.0	3.1	kHz
FG duty	D _{TTG}	U, V, W=120° shift pulse	45	50	55	%
Soft switching FG high voltage	V _{SCMHI}	U, V, W=120° shift pulse	2.68	2.75	2.82	V
Soft switching FG low voltage	V _{SCMLO}	U, V, W=120° shift pulse	2.18	2.25	2.32	V
Soft switching FG charging current	I _{SCMCH}	U, V, W=120° shift pulse	42	50	58	μA
Soft switching FG discharging current	I _{SCMDC}	U, V, W=120° shift pulse	42	50	58	μA
SPINDLE READY						
READY output high voltage	V _{RDHI}	Shift pulse, CNTL1=5V	4.5	4.8	5.0	V
READY output low voltage	V _{RDLO}	Shift pulse, CNTL1=5V	0	0.2	0.5	V
SPINDLE RPMSEL						
RPMSEL input high voltage	V _{RPHI}	—	1.4	—	—	V
RPMSEL input high current	I _{RPHI}	—	10	14	18	μA
RPMSEL input low voltage	V _{RPLO}	—	—	—	1.4	V
RPMSEL input low current	I _{RPLO}	—	-5	0	0	μA

ELECTRICAL CHARACTERISTICS (Continued)

(Ta=25°C, unless otherwise specified)

Characteristic	Symbol	Test conditions	Min.	Typ.	Max.	Unit
SPEED CONTROL						
VCNT charging current	I _{VCCH}	Shift pulse, CNTL1=5V	-60	-50	-40	μA
VCNT discharging current	I _{VCDC}	Shift pulse, CNTL1=5V	40	50	60	μA
BRAKE						
CBrake output voltage	V _{BC}	V _{CC} =12V, V _{DD} =5V	11.0	11.3	11.5	V
Brake output high voltage	V _{BH}	CNTL1=0V	4.8	4.9	5.0	V
Brake output low voltage	V _{BL}	CNTL1=2.5V	0	0.2	0.5	V
SPINDLE OUTPUT						
U saturation voltage_upper5	V _{SU5U}	R _U =R _V =R _W =5Ω	0.2	0.3	0.5	V
V saturation voltage_upper5	V _{SV5U}	R _U =R _V =R _W =5Ω	0.2	0.3	0.5	V
W saturation voltage_upper5	V _{SW5U}	R _U =R _V =R _W =5Ω	0.2	0.3	0.5	V
U saturation voltage_lower5	V _{SU5L}	R _U =R _V =R _W =5Ω	0.2	0.3	0.5	V
V saturation voltage_lower5	V _{SV5L}	R _U =R _V =R _W =5Ω	0.2	0.3	0.5	V
W saturation voltage_lower5	V _{SW5L}	R _U =R _V =R _W =5Ω	0.2	0.3	0.5	V
U output frequency	F _U	CNTL2=12kHz	0.9	1	1.1	kHz
V output frequency	F _V	CNTL2=12kHz	0.9	1	1.1	kHz
W output frequency	F _W	CNTL2=12kHz	0.9	1	1.1	kHz
Leakage current	I _{SPL}	—	-50	0	50	μA
Transconductance gain_U	GM _U	R _U =R _V =R _W =5Ω	0.7	0.8	0.9	A/V
Transconductance gain_V	GM _V	R _U =R _V =R _W =5Ω	0.7	0.8	0.9	A/V
Transconductance gain_W	GM _W	R _U =R _V =R _W =5Ω	0.7	0.8	0.9	A/V
CCOMP charging current	I _{COMP}	VCTL=5V	-400	-500	-600	μA
REGULATOR						
Adjustable pin voltage	V _{ADJ}	V _{DD} =5V	1.2	1.3	1.4	V
Regulator line regulation	R _{LINE}	V _{DD} =Sweep	0	0.1	0.5	%
Regulator load regulation	R _{LOAD}	I _O =Sweep	0	0.1	0.5	%

ELECTRICAL CHARACTERISTICS (Continued)

(Ta=25°C, unless otherwise specified)

Characteristic	Symbol	Test conditions	Min.	Typ.	Max.	Unit
VCM PWM CONTROL						
High PWMH input current	I _{PWMH1}	PWMH=5V	100	113	130	μA
Low PWMH input current	I _{PWMH2}	PWMH=5V	-130	-113	-100	μA
High PWML input current	I _{PWML1}	PWML=5V	100	113	130	μA
VCM PWM CONTROL						
Low PWML input current	I _{PWML2}	PWML=0V	-130	-113	-100	μA
CFVCM charge / discharge current1	I _{CFVCM1}	PWMH=0V, PWML=0V	-530	-516	-500	μA
CFVCM voltage1	V _{CFVCM1}	PWMH=0V, PWML=0V	5.9	6.06	6.3	V
CFVCM charge / discharge current5	I _{CFVCM5}	PWMH=PWML=2.5V	-10	0	10	μA
CFVCM voltage5	V _{CFVCM5}	PWMH=PWML=2.5V	3.8	4.0	4.2	V
CFVCM charge / discharge current9	I _{CFVCM9}	PWMH=PWML=5V	-530	-516	-500	μA
CFVCM voltage9	V _{CFVCM9}	PWMH=PWML=5V	1.7	1.94	2.1	V
PWM current ratio	R _{PWM}	—	31	32	33	—
PWMH current variation	I _{VPWMH}	—	0.95	1	1.05	mA
PWML current variation	I _{VPWML}	—	29	31.3	34	μA
VCM OFFSET COMPARATOR						
VCM reference voltage	V _{REF4V}	V _{CC} =12V, V _{DD} =5V, CNTL3=5V	3.8	4	4.2	V
Offset comparator offset voltage	V _{OCOS}	ERRIN=Sweep	20	30	40	mV
Offset comparator hysteresis	V _{OCHYS}	ERRIN=Sweep	20	30	40	mV
Offset comparator high voltage	V _{OCH}	ERRIN=Sweep	4.5	4.8	5.0	V
Offset comparator low voltage	V _{OCL}	ERRIN=Sweep	0	0.2	0.5	V
VCM POWER AMPLIFIER						
Power Amplifier gain1	A _{PO1}	ERRIN=Sweep	16	17	18	—
Power Amplifier gain1	A _{PO2}	ERRIN=Sweep	16	17	18	—
Power Amplifier output high voltage1	V _{POH1}	ERRIN=Sweep	11.5	11.8	12.0	V
Power Amplifier output high voltage2	V _{POH2}	ERRIN=Sweep	11.5	11.8	12.0	V
Power Amplifier output low voltage1	V _{POL1}	ERRIN=Sweep	0	0.2	0.5	V
Power Amplifier. output low voltage2	V _{POL2}	ERRIN=Sweep	0	0.2	0.5	V

ELECTRICAL CHARACTERISTICS (Continued)

(Ta=25°C, unless otherwise specified)

Characteristic	Symbol	Test conditions	Min.	Typ.	Max.	Unit
VCM ERROR AMPLIFIER						
Amplifier output high voltage	V _{EOH}	PWMH=Sweep, PWML=2.5V	10.8	11.2	11.5	V
Amplifier output low voltage	V _{EOL}	PWMH=Sweep, PWML=2.5V	0.5	0.8	1.2	V
Amplifier output offset voltage	V _{OS}	PWMH=Sweep, PWML=2.5V	-20	0	20	mV
Short circuit current	I _{ESC}	PWMH=Sweep, PWML=2.5V	8	10	15	mA
VCM AMPLIFIER TOTAL						
VCM offset voltage	V _{OSVCM}	PWMH=PWML=2.5V	-5	0	5	mV
VCM transconductance gain high	GM _{VH}	ERRIN=Sweep, GAINSEL=5V	0.47	0.50	0.53	A/V
VCM transconductance gain low	GM _{VL}	ERRIN=Sweep, GAINSEL=5V	0.1	0.3	0.5	A/V
VCM+ saturation voltage lower	V _{VMS5}	ERRIN=2V, R _{VCM} =10Ω	0.1	0.3	0.5	V
VCM- saturation voltage upper	V _{VMS6}	ERRIN=2V, R _{VCM} =10Ω	0.1	0.3	0.5	V
VCM+ saturation voltage upper	V _{VMS7}	ERRIN=6V, R _{VCM} =10Ω	0.1	0.3	0.5	V
VCM- saturation voltage lower	V _{VMS8}	ERRIN=6V, R _{VCM} =10Ω	0.1	0.3	0.5	V
Leakage current power Amplifier1	I _{VCML1}	—	-50	0	50	μA
Leakage current power Amplifier2	I _{VCML2}	—	-50	0	50	μA
RETRACT						
Min. operating voltage of CRET2	V _{CRET2}	CRET2=Sweep	10.8	11.2	11.5	V
Source voltage	V _{SRC}	CRET2=5V	0.5	0.8	1.2	V
Sinking saturation voltage	V _{RTSAT}	CRET2=5V	-20	0	20	mV
VCM retract sinking current2	I _{RCT2}	R _{ret} =4.2kΩ	8	10	15	mA
THERMAL SHUT DOWN						
Operating temperature	T _{SD}	—	3.8	4	4.2	V
Thermal hysteresis	T _{HYS}	—	20	30	40	mV

APPLICATION INFORMATION

The KA3121 is a combination chip consisting of spindle motor and voice coil motor designed for HDD system.

SPINDLE MOTOR DRIVE PART

The Spindle motor driver drives the Brushless DC Motor (BLDCM) that is used to spin the disk. It contains the power drivers (2.0A, max) for the 3 phases of the motor, which is both the low and high side drivers (H-bridge). To reduce the output transistors saturation voltage, the vertical PNP transistor is used as the high side driver. The commutation timing and sequencing for the driver outputs is determined by the commutation control circuit. The driver outputs are also connected to comparators. They are used for back EMF sensing. The outputs of the Back-EMF comparators are connected to the zero cross detector and commutation & spindle motor control function block. The zero crossings in this signals are used to determine the timing of the commutation and measurement of spindle motor speed.

FREQUENCY GENERATION (FG) & READY

FG stands for Frequency Generation. Representing the current spindle motor speed frequency, it contains important information about the motor speed and motor spin. VCM enable when the READY signal output is High. FG frequency (Hz), motor speed (rpm) and pole number are directly related as shown below in the three phase motor. FG frequency calculation equation is as follow;

$$\text{FG frequency} = \text{motor speed} \times \text{pole number} \times 3 / 120$$

For example in a typical application,

Target speed = 5, 400[RPM], motor polenumber = 8[poles]

$$\text{FG frequency} = 5400 \times 8 \times 3 / 120 = 1080\text{Hz}$$

SPINDLE MOTOR SPEED CONTROL

Motor speed is measured by the speed reference clock via the masked FG signal which is proportional to motor speed. The speed discriminator compares FG frequency with the target motor speed (Speed reference clock) and sends signal to the buffer amplifier input by the F/V output as pulse signals ($I_{CHARGE}/I_{DISCHARGE}$). This F/V output signals internally compare the buffer amplifier reference voltage. And then the signals control CVCNT voltage by the charging or discharging the external capacitor connected the CVCNT pin.

Spindle motor (SPM) current controlled compares buffer output voltage via motor current which is sensing the external resistor connected the PCS pin.

The sense amplifier determines maximum output current during the start-up.

The Back-EMF is used in the sensorless BLDC motor driver to determine the rotor position. The detected rotor position is a very important information to control the motor speed and the commutation timing.

At standstill condition, there is no back-EMF voltage and no FG output. There is no information about the motor position. However the spindle motor must be started up at standstill.

To drive the spindle motor at the start-up mode, the control signal CNTL1 input is High and CNTL2 to be used as start up clock.

The control signal CNTL1 is continuously provides HIGH signal until the Back-EMF generated is enough large to produce the FG signal i.e. the spindle motor can be driven by the self commutation. During a fixed time, if the back-EMF generated is too small and the spindle motor is not driven by the self commutation, retry the start-up.

Table 1. Pin setup truth table

	CNTL1 ⁽¹⁾		CNTL2 ⁽²⁾		GAINSEL	
	SPM driver	Brake	Ready Off	Ready On	SPM driver	VCM gain
High (5V)	1	0	Start-up clock High	VCM On	Normal	0.125
Open (Floating)	0	0	Start-up clock Low	VCM Off	x	x
Low (0V)	0	1	x	Retract On	Start up ⁽³⁾ Hold	0.5

NOTES:

1. CNTL1: Spindle motor control
2. CNTL2: Start-up clock & VCM Amplifier control
3. Test only
4. "1": Enable; "0": disable; "S/W": switching

ACCELERATION MODE

When the Back-EMF detected is enough to be used as the information of motor position, the mode is changed from start-up to acceleration. The Back-EMF amplifier sends the commutation timing signal via MCLK according to the commutation clock generator output.

By using the back-EMF, the spindle motor is self-commuted at acceleration and running modes. During the motor drive, the spindle motor is commuted at that point which is electrically 30° delayed controlled by commutation clock generator.

RUNNING MODE

It is called to the running mode when the spindle motor speed arrives within $\pm 1\%$ of the target speed. The switching mode, commutation delay time, MCLK delay time (T_d) and masking time are changed at the running mode. The spindle motor speed is controlled by PWM signal within $\pm 0.01\%$. The soft switching using the current slope of the motor may reduce noise, EMI (Electromagnetic Interference) and spark voltage which is generated on the motor coil at the switching.

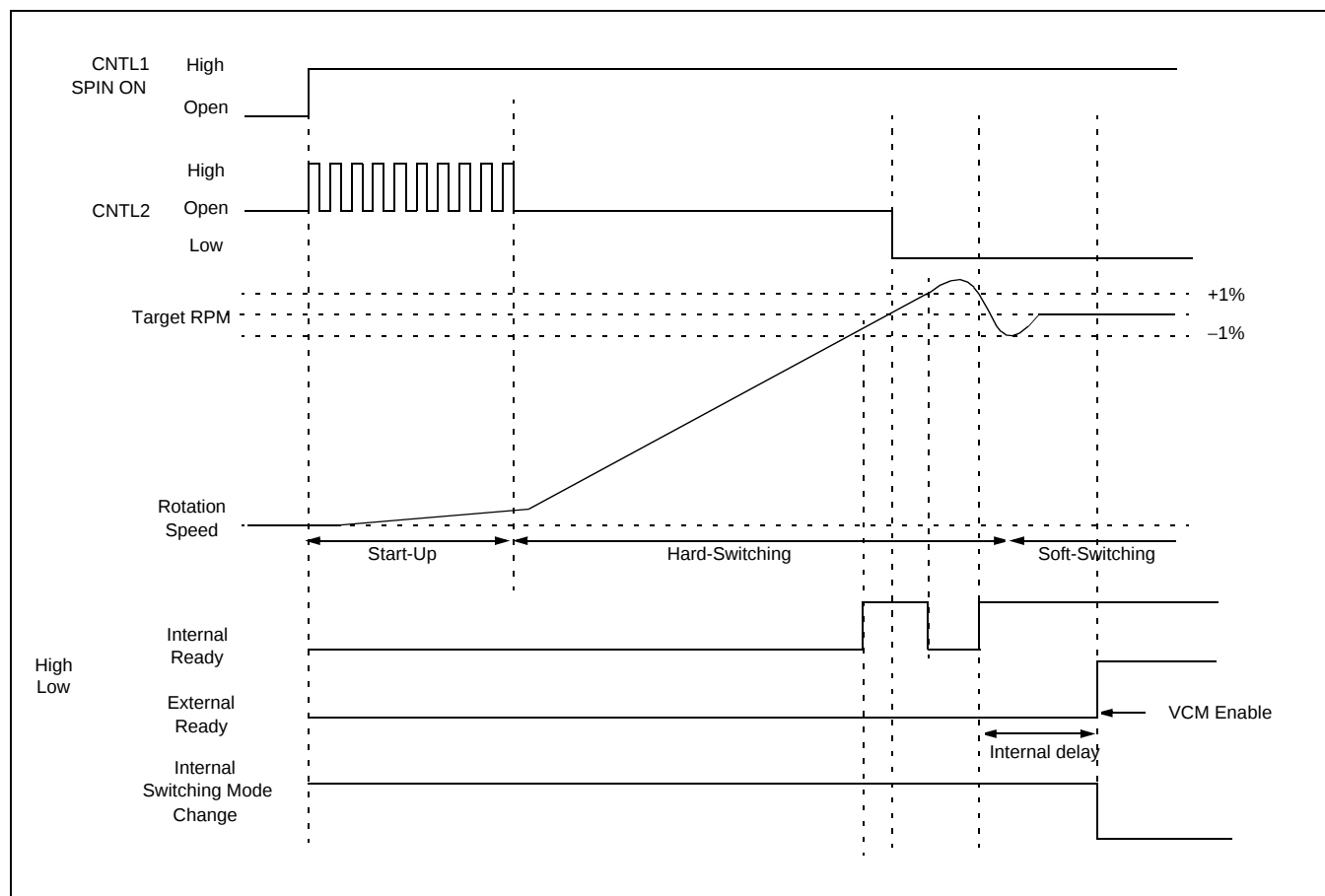
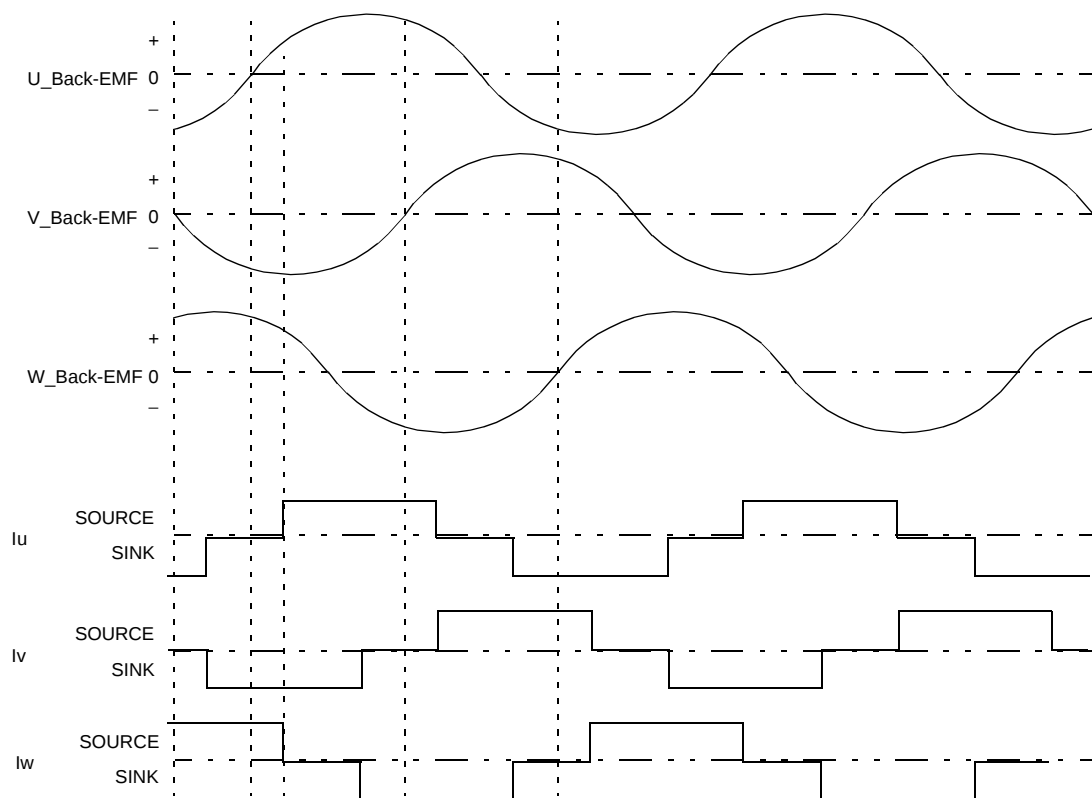


Figure 1. Motor start-up sequence

(1) Acceleration Mode: Hard-Switching Mode



(2) Running Mode: Soft-Switching Mode

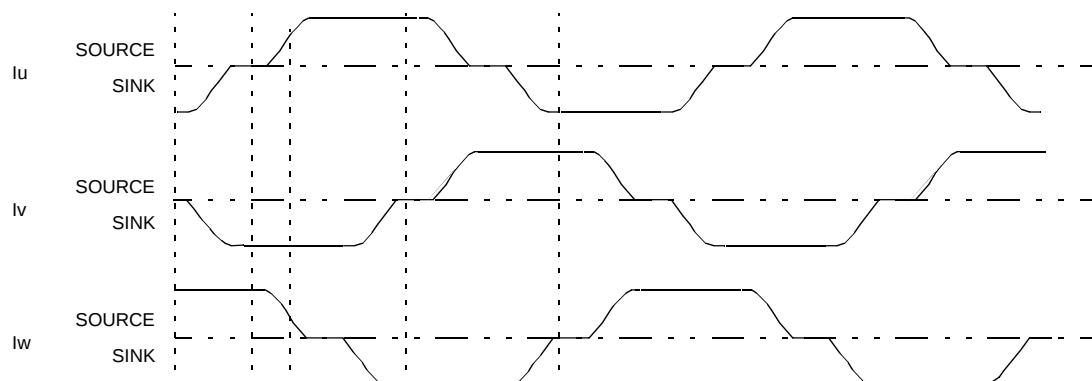


Figure 2. Acceleration and running the spindle motor

VCM driver

The schematic diagram illustrates a fully differential PWM generator circuit. It features two differential input pairs, PWMH input (pin 13) and PWML input (pin 14), each connected to a resistor divider (R1, R2) and a transconductance amplifier (Gm). The outputs of these amplifiers are connected to a common-mode feedback network (VREF(4V), R3) and a differential output stage (C1, C2). The output stage is connected to a common-mode feedback network (CFVCM, C1) and a differential output stage (C2, R4). The final output is PWMOUT (pin 15).

The diagram illustrates a motor driver circuit. It features a feedback loop where the motor current is sensed (Imotor) and fed back to a summing junction (pin 25). The summing junction output (pin 30) is integrated (pins 28, 18) to produce the motor drive signal (pin 27). The motor (L, RL) is driven by the motor drive signal (pin 27) and the sense resistor (Rsense). The system also includes a 4V reference (pin 3) and a 1/2VCC reference (pin 1).

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The transconductance of VCM AMPLIFIER gain, G_m , is:

$$G_m = \frac{I_{motor}}{V_{in}} = \frac{2 \cdot A_{error} \cdot A_{power} \cdot R_{25}}{2 \cdot R_{18} \cdot R_{sense} \cdot A_s \cdot A_{error} \cdot A_{power} + (R_{18} + R_{25})(Z_{motor} + R_{sense})}$$

$$G_m = \frac{A_{loop}}{1 + A_{loop}} \left(\frac{R_{25}}{R_{18} R_{sense} A_s} \right)$$

$$A_{loop} = \frac{2 \cdot R_{18} \cdot A_s \cdot A_{error} \cdot A_{power}}{(R_{18} + R_{25})(Z_{motor} + R_{sense})}$$

Therefore $A_{loop} \gg 1$,

$$G_m \cong \frac{R_{25}}{R_{18}} \cdot \frac{1}{R_{sense}} \cdot \frac{1}{A_s}$$

The Transconductance (G_m) can be adjusted by selecting the external components R_{18} , R_{25} and sense resistor R_{sense} .

if $R_{18} = 15k$, $R_{25} = 15k$, $R_{sense} = 1$

GAINSEL = 0(0V), $1 / A_s = 0.5$

$G_m = 0.5$

GAINSEL = 1(5V), $1 / A_s = 0.125$

$G_m = 0.125$

VCM current (I_{motor}) is:

GAINSEL = 0(0V)

$$I_{motor} = 4 \times \left[(PWMH - 0.5) + \frac{1}{64} (PWML - 0.5) \right] \times \frac{R_{25}}{R_{18}} \times \frac{1}{R_{sense}} \times 0.5$$

GAINSEL = 1(5V)

$$I_{motor} = 4 \times \left[(PWMH - 0.5) + \frac{1}{64} (PWML - 0.5) \right] \times \frac{R_{25}}{R_{18}} \times \frac{1}{R_{sense}} \times 0.125$$

Recommended value	$PWMH(100\%) = 1$
$R_{18} = R_{25} = 15k$	$PWMH(50\%) = 0.5$
$R_{sense} = 1$	$PWMH(0\%) = 0$

RETRACT CIRCUIT

The retract function is the operation where the VCM moves from the data zone to the parking zone when off normal state power and abnormal power interrupt cause the spindle motor to stop.

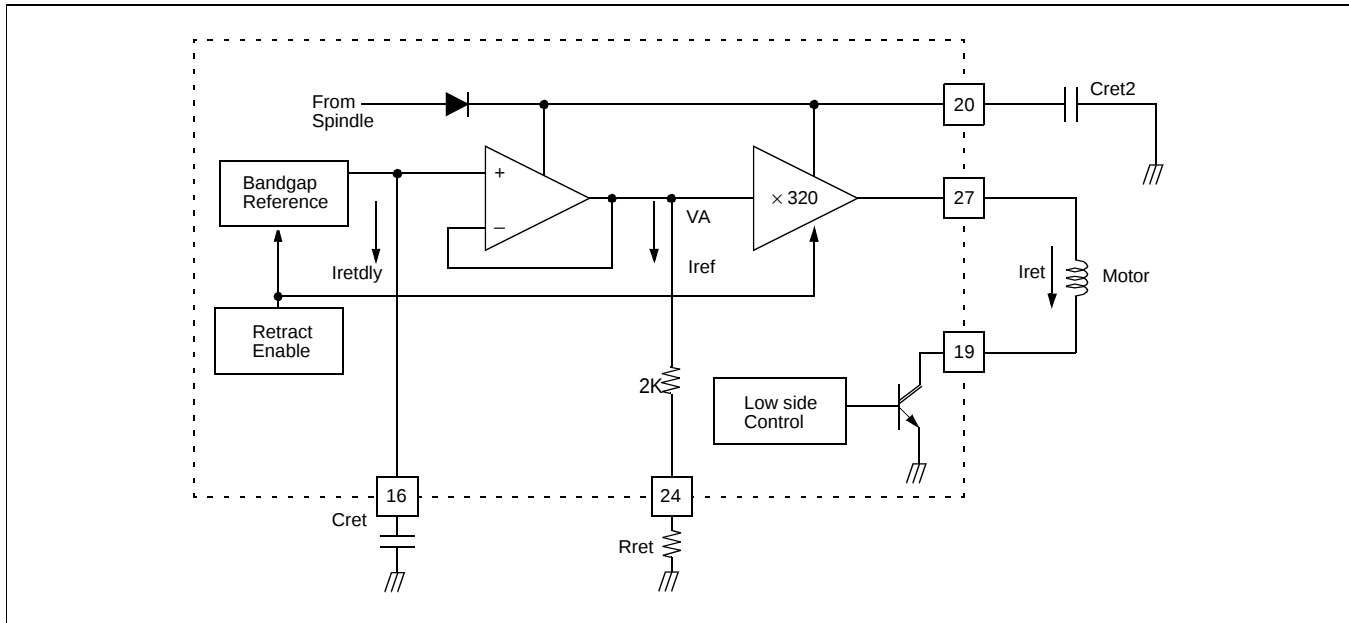


Figure 5. Retract block schematic

$$\begin{aligned}
 V_A &= 2.0V \\
 I_{ref} &= \frac{V_A}{R_{ret} + 2k} \\
 I_{ret} &= I_{ref} \times 320
 \end{aligned}$$

$$T_{retdly} = \frac{C_{ret} \times 2.0V}{I_{retdly}(= 100\mu)}$$

POWER MANAGEMENT FEATURES

LOW POWER INTERRUPT

The low power interrupt operation occurs when the power supply voltage (5V,12V) level drops below each threshold voltage. The threshold voltage (V_{th}) and time delay (T_{dly}) may be adjustable by the external component value.

$$T_{dly} = CDLY \frac{V_{th}}{I}, (V_{th} = 2.5V, I = 14.0\mu A)$$

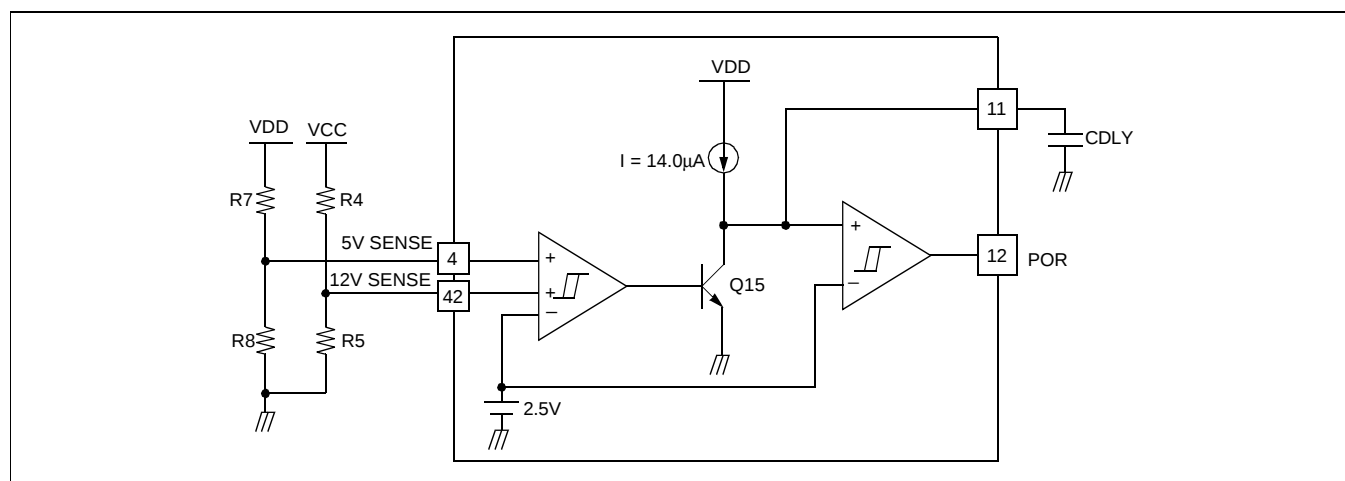


Figure 6. Power on reset block schematic

POWER ON RESET

The power-on reset circuit monitors the voltage level of both +5V and +12V power supplies. The power-on reset circuit disables the spindle motor out block, the whole VCM block, and the digital ASIC when the power supply voltage level drops below the reference voltage.

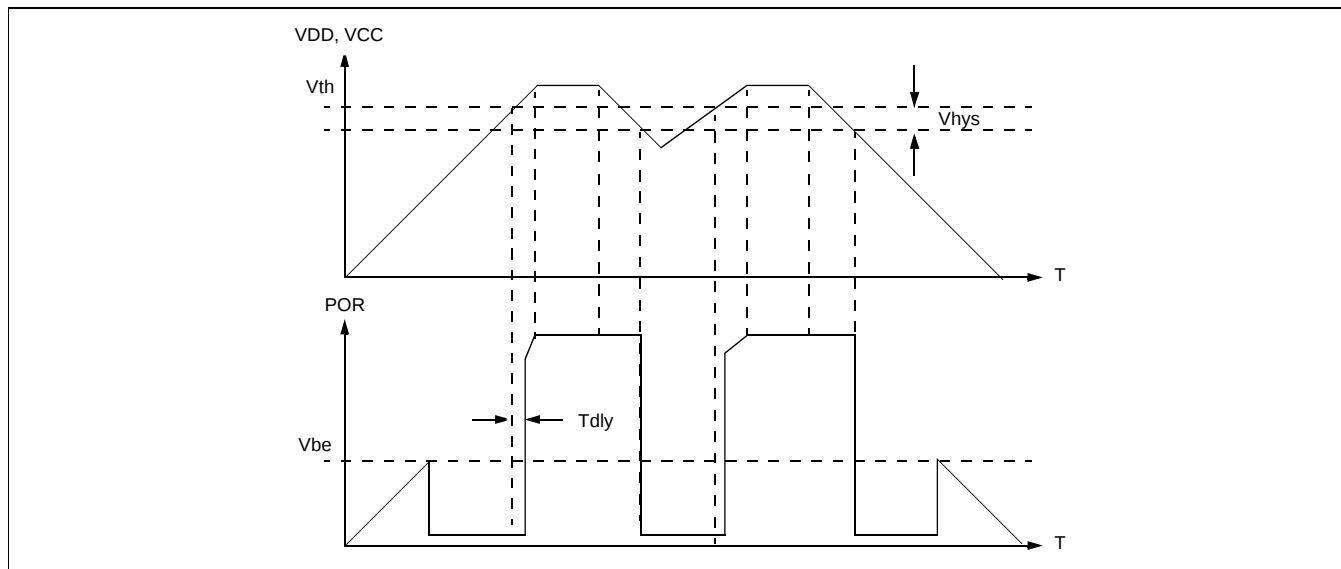


Figure 7. Power on reset function

$$V_{hys} = 4.2mV$$

$$V_{DD}; V_{hys}(5V) = \frac{R4 + R5}{R5} \times V_{hys}$$

$$V_{CC}; V_{hys}(12V) = \frac{R7 + R8}{R8} \times V_{hys}$$

Default (pin4, pin42 : not connected)

$$V_{DD}, th \cong 4.1V$$

$$V_{CC}, th \cong 9.4V$$

REGULATOR

The KA3121 includes the regulator block which supplies power of the digital ASIC. It consists of the bias block, the band gap reference, the error Amplifier and the external NPN power Tr. The regulator voltage can be adjusted by the external resistor, R3a, R3b..

$$V_{reg} = V_{ref} \left(1 + \frac{R3a}{R3b} \right), V_{ref} = 1.3V$$

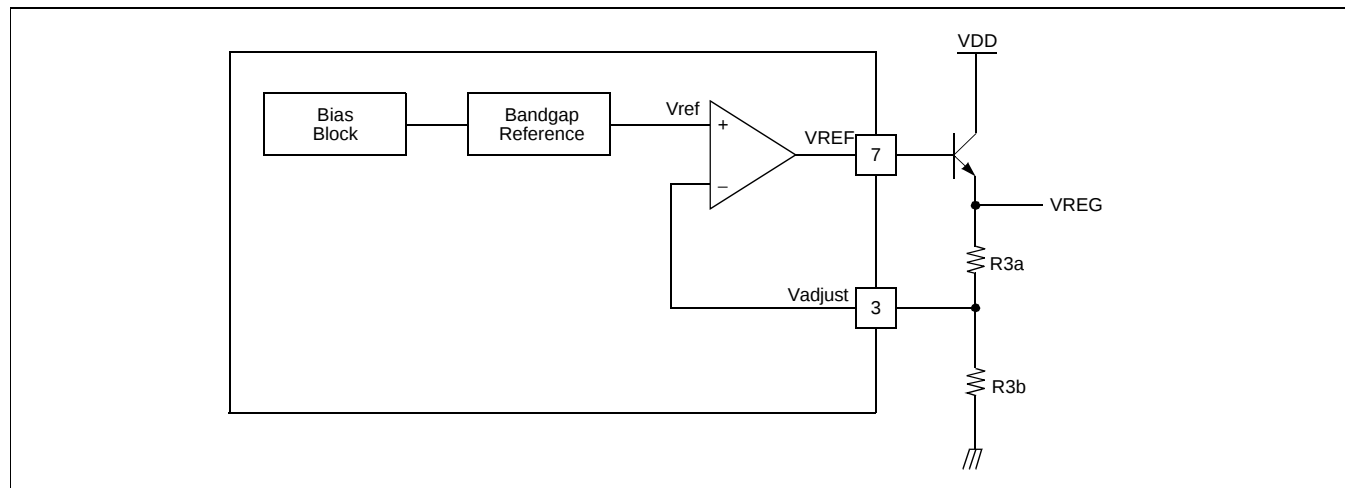


Figure 8. Regulator schematic

if R3a = 15k, R3b = 10k

$$V_{reg} = V_{ref} \left(1 + \frac{R3a}{R3b} \right) = 1.3 \times \left(1 + \frac{15k}{10k} \right) = 3.25V$$

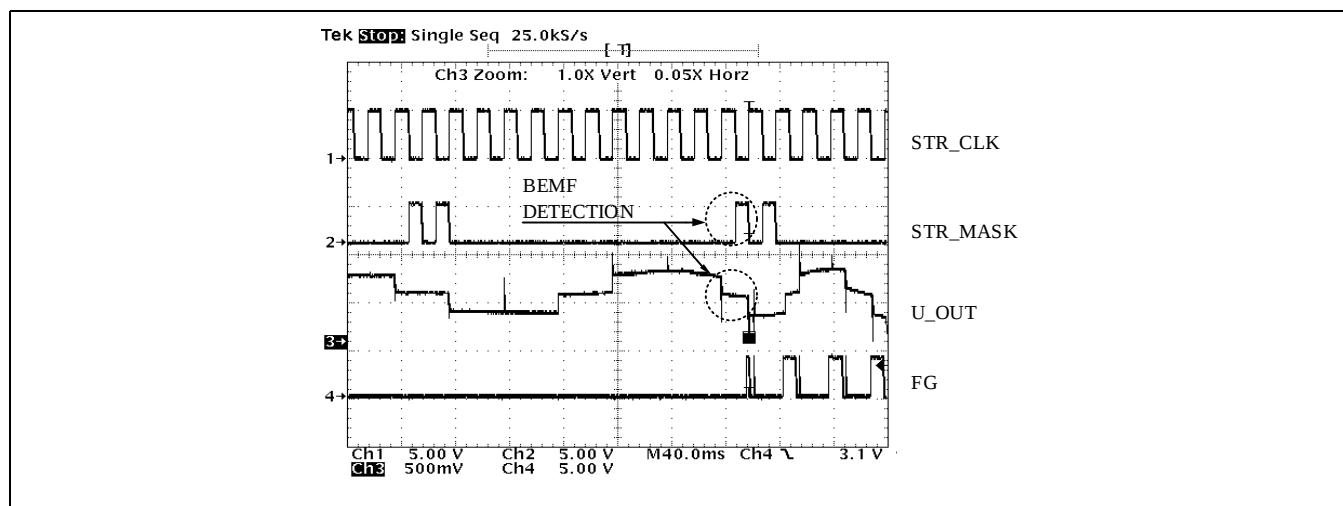


Figure 9. Start-up mode

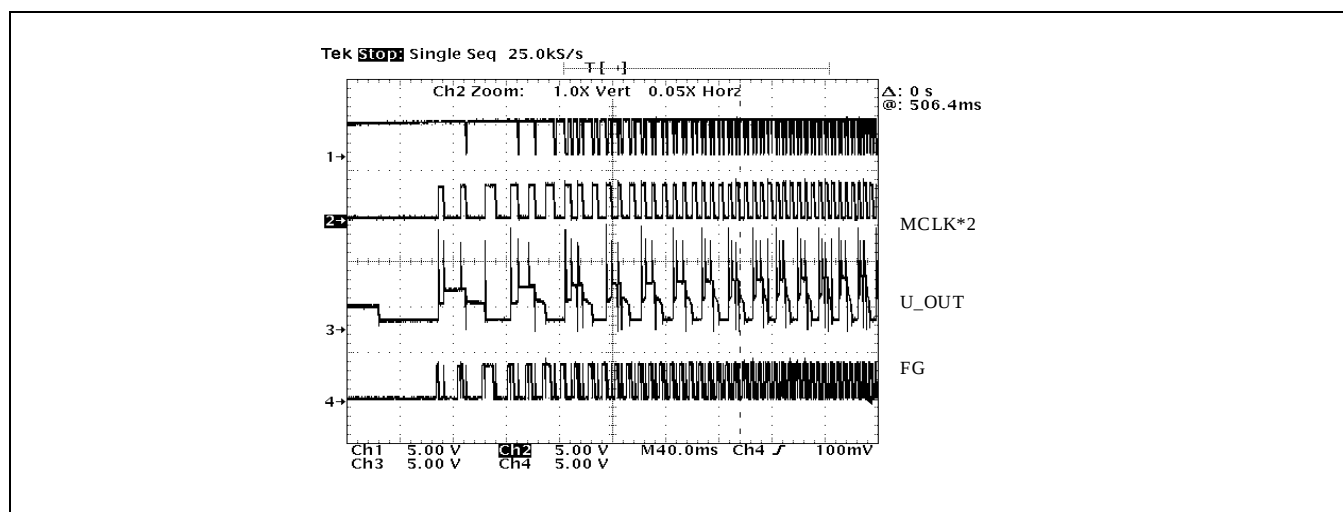


Figure 10. Acceleration mode 1

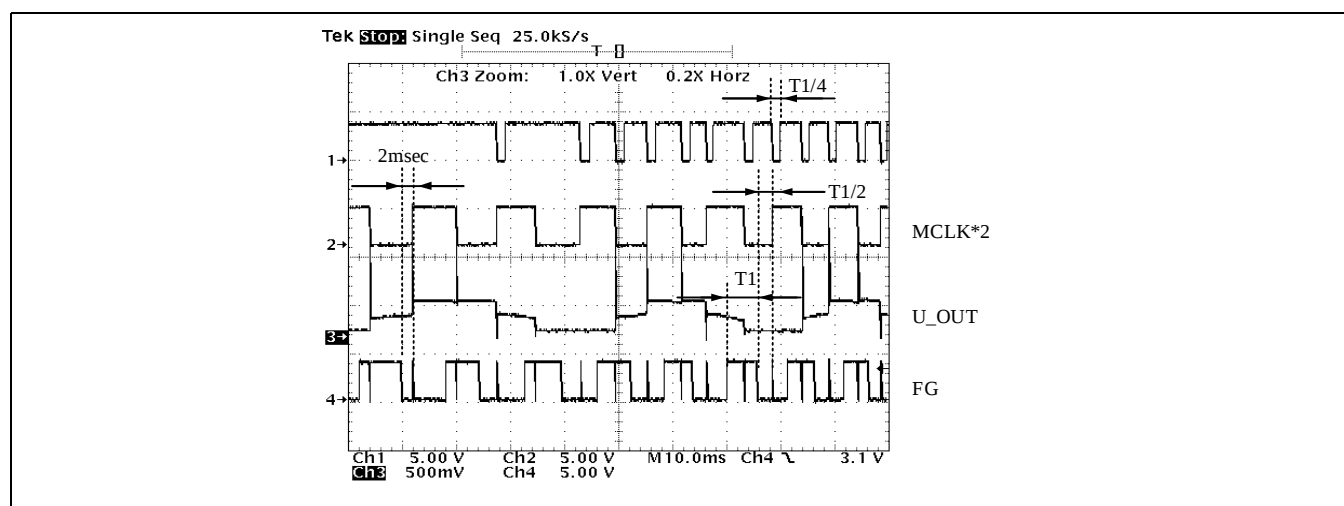


Figure 11. Acceleration mode 2

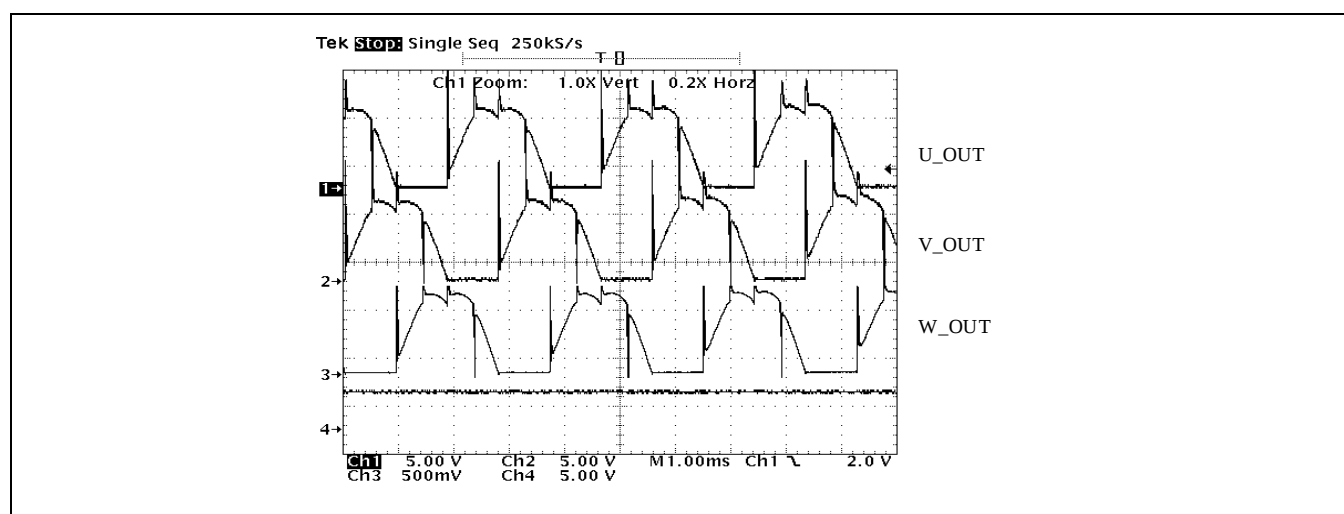


Figure 12. Output in hard-switching mode

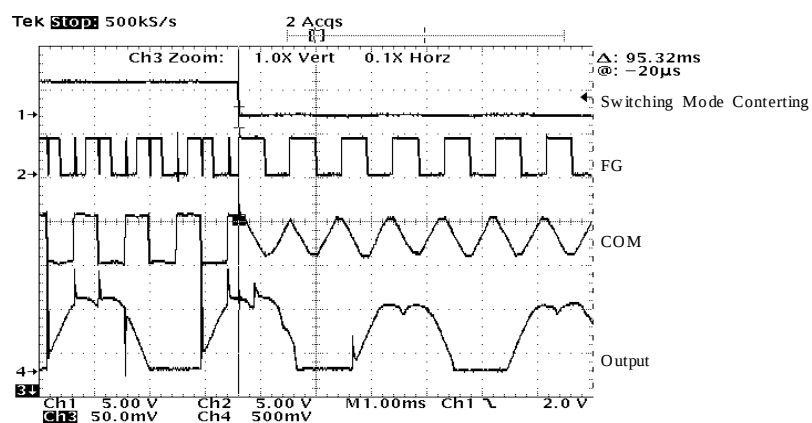


Figure 13. Switching mode converting

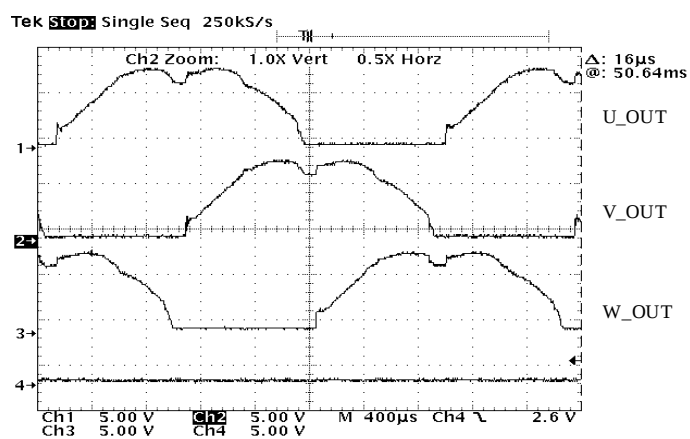
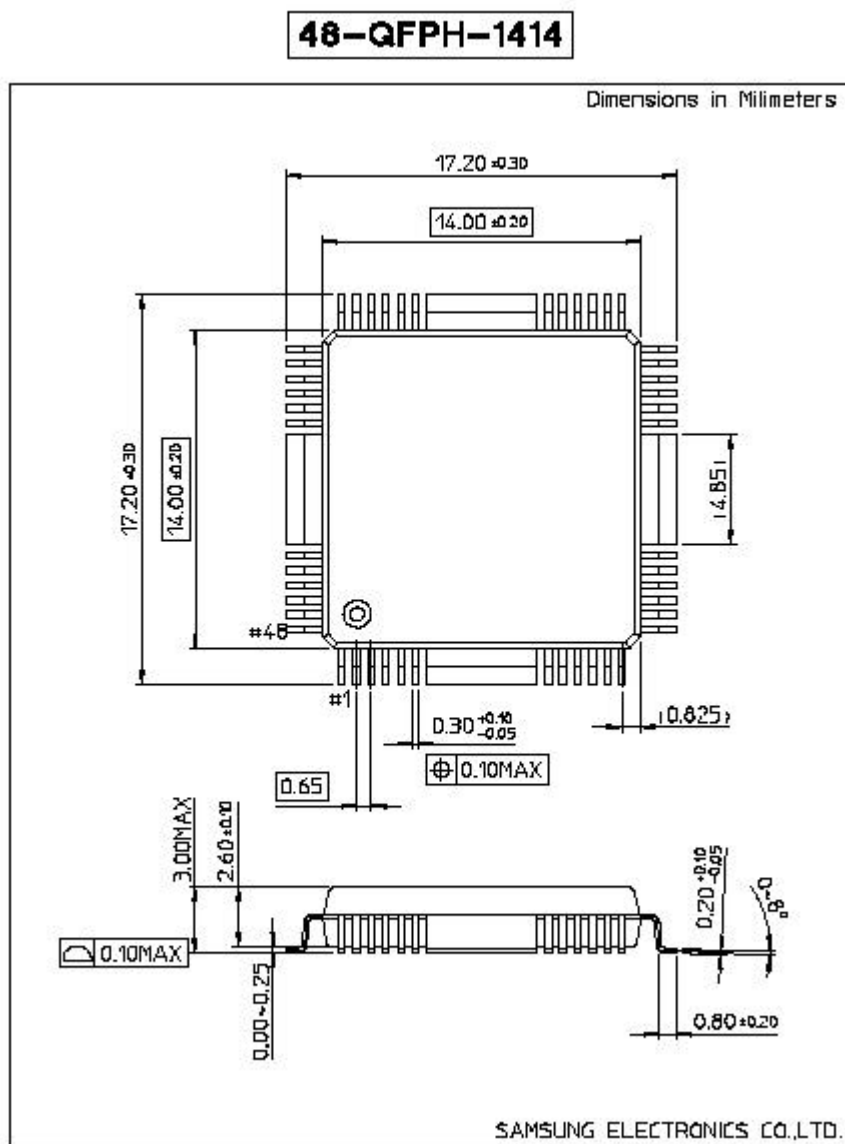


Figure 14. Soft-switching mode

PACKAGE DIMENSION



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