3-PHASE DRUM MOTOR DRIVER

KA3081D is a bipolar integrated circuit and used to drive 3-phase brushless DC motor in full wave mode using 1-hall sensor.
KA3081D uses 1-hall for commutation and PG generation. It is a special circuit for soft switching using 1-hall reduces the EMI and eliminates snubber. The FG is generated by BEMF.

20-SOP-300

FEATURES

- Commutation FG, PG is executed by 1-hall
- Soft switching at output terminal reduces switching impulse
- 3-phase full wave
- Voltage reference (Uses band gap circuit)
- Built-in thermal shut-down (TSD) circuit

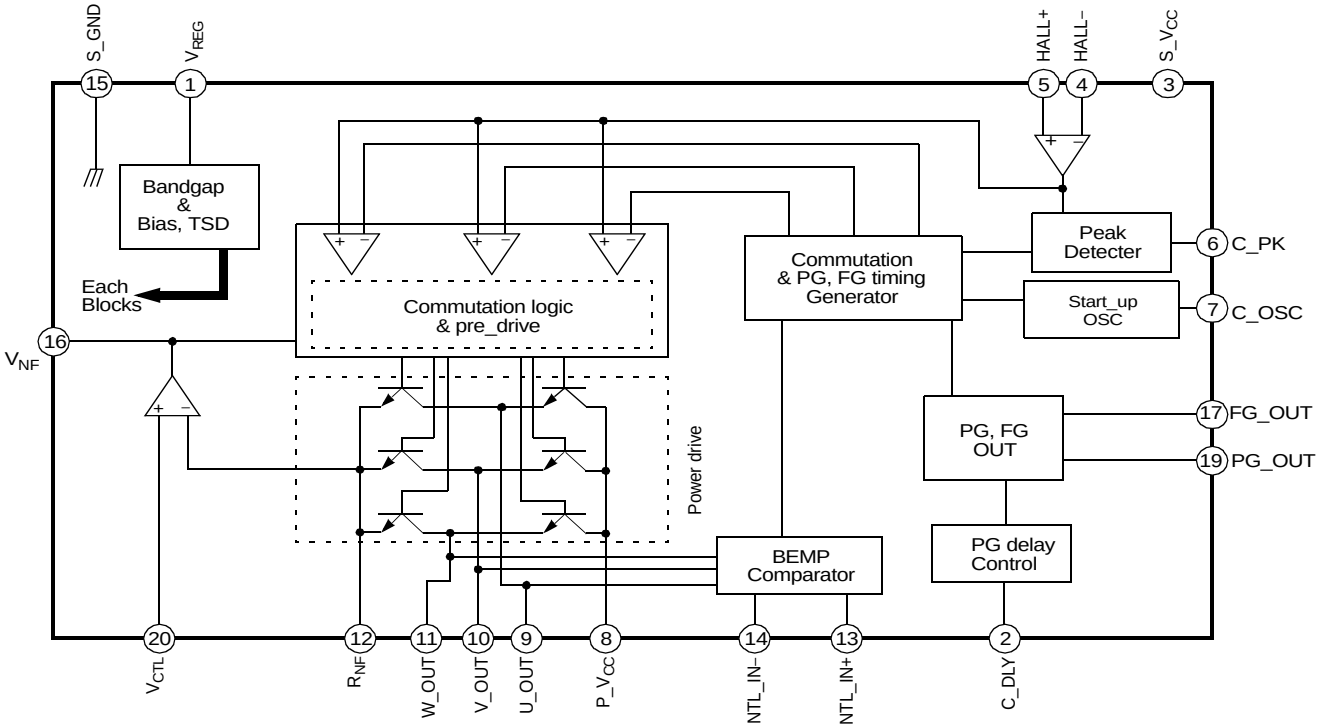
ORDERING INFORMATION

Device	Package	Operating Temperature
KA3081D	20-SOP-300	–25°C ~ +75°C

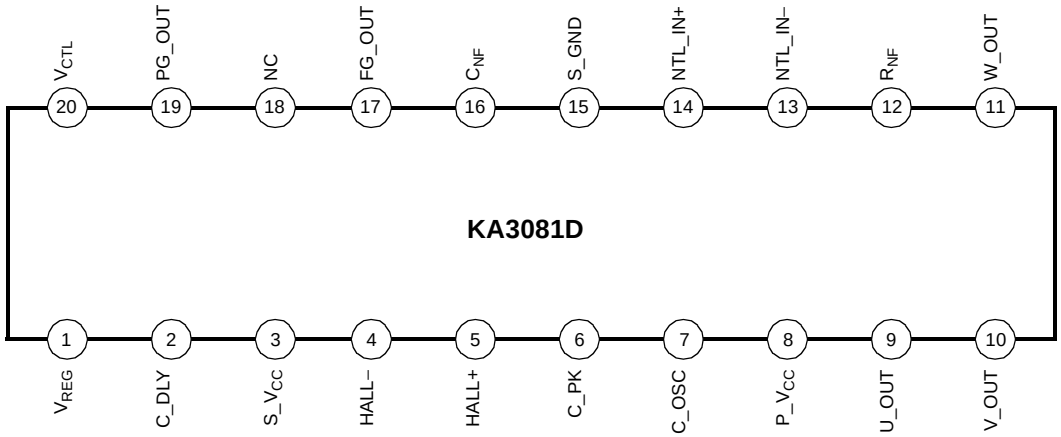
TARGET APPLICATION

- VCR drum motors

BLOCK DIAGRAM



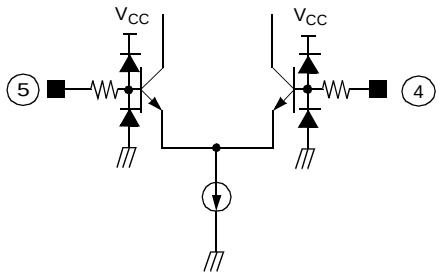
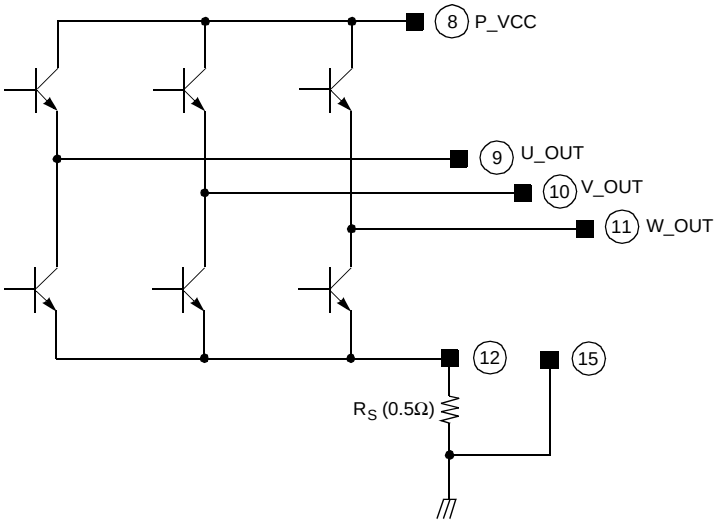
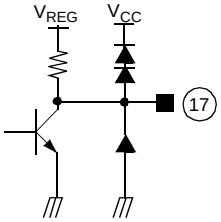
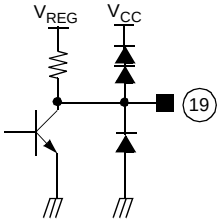
PIN CONFIGURATIONS



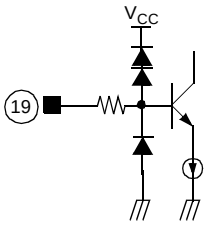
PIN DESCRIPTIONS

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	V_{REG}	Regurator output	11	W_OUT	W-phase output
2	C_DLY	PG. delay	12	R_{NF}	Output current sensing
3	S_V_{CC}	Signal V_{CC}	13	NTL_IN–	Input from the neutral point of the motor coils.
4	HALL–	Hall- input	14	NTL_IN+	Input from the neutral point of the motor coils.
5	HALL+	Hall+ input	15	S_GND	Signal ground
6	C_PK	Peak detector of hall signal	16	C_{NF}	Phase compensation
7	C_OSC	Start-up oscillator	17	FG_OUT	FG. output
8	P_V_{CC}	Power V_{CC}	18	NC	–
9	U_OUT	U-phase output	19	PG_OUT	PG. output
10	V_OUT	V-phase output	20	V_{CTL}	Output current control

INTERNAL CIRCUIT

Description	Pin No.	Internal circuit
Hall input	5,4	
Output & Current detection	9,10,11 8,2	
FG Output	17	
PG Output	19	

INTERNAL CIRCUIT (Continued)

Description	Pin No.	Internal circuit
Voltage control reference	20	

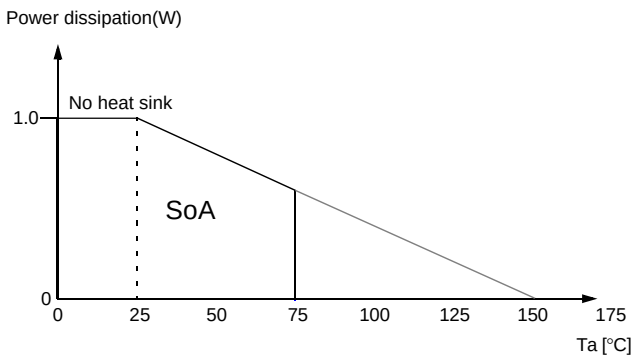
ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Characteristics	Symbol	Value	Unit	Remark
Supply voltage (Signal)	V_{CCmax}	20	V	–
Maxium Output current	I_{Omax}	1.0 note1	A / Phase	
Regulator output current	I_{REGmax}	10	mA	
Power dissipation	P_d	1.0 note2	W	No heat sink
Junction temperature	T_J	150	°C	–
Operating temperature	T_{OPR}	–20 ~ +75	°C	Ambient temperature (Ta)
Storage temperature	T_{STG}	–40 ~ +155	°C	

NOTES:

1. Duty 1 / 100, pulse width 500μs
2. 1) When mounted on glass epoxy PCB (76.2 × 114 × 1.57mm)
   2) Power dissipation reduces 9.6mW / °C for using above Ta=25°C.
   3) Do not exceed Pd and SOA.

PD GRAPH

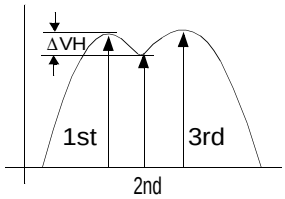


RECOMMENED OPERATING CONDITIONS

Characteristics	Symbol	Min.	Typ.	Max	Unit
Operating supply voltage(Signal)	S_V_{CC}	4.5	5.0	5.5	V
Operating supply voltage(Power)	P_V_{CC}	8	12	18	V

ELECTRICAL CHARACTERISTICS

(Measured in test circuit, P_V_{CC}=12V, Ta=25°C)

Characteristic	Symbol	Test conditions	Spec.			Unit
			Min.	Typ.	max.	
TOTAL						
Supply voltage	V_{CC}	–	8.0	–	18	V
Supply current (1)	I_{CC1}	P_V_{CC}=12V, V_{REG}=open, V_{CTL}=0V	–	11.2	17	mA
Supply current (2)	I_{CC2}	P_V_{CC}=12V, V_{REG}=open, V_{CTL}=0V	–	11.5	17	mA
REGURATOR						
V_{REG} output voltage (2)	V_{REG2}	P_V_{CC}=12V, I_{REG}=0mA	4.7	5.0	5.3	V
V_{REG} output voltage (5)	V_{REG5}	P_V_{CC}=12V, I_{REG}=10mA	4.7	5.0	5.3	V
START-UP OSCILLATOR						
C_OSC operation frequency	OSC_FEQ	C_OSC=47nF	6	8	10	Hz
C_OSC charging current	OSC_ICH	C_OSC=47nF	–0.5	–2	–3.5	µA
C_OSC discharging current	OSC_IDC	C_OSC=47nF	1	3	5	µA
C_OSC low threshold voltage	OSC_THL	C_OSC=47nF	0.2	0.5	0.8	V
C_OSC high threshold voltage	OSC_THH	C_OSC=47nF	2.7	3.0	3.3	V
VOLTAGE CONTROL						
V_{CTL} start voltage	V_{CTL_ST}	V_{CTL}=0~2V When I_O=25mA	1.01	1.26	1.51	V
V_{CTL} input voltage range	V_{CTL_IN}	V_{REG}	0	–	V_{REF}	V
V_{CTL} input bias current	V_{CTL_BI}	V_{CTL}=2.0V	–	1.0	1.5	µA
Gain	GM	R_{NF}=0.47Ω, V_{CTL}=0~2V	0.38	0.45	0.52	A
HALL INPUT						
Input hall signal Min. voltage note	V_{H_MIN}		300	–	–	mVp-p
PG hall 1'st Min. voltage note	V_{H_P1}		60	–	–	mVo-p
PG hall 2'nd Min. voltage note	V_{H_P2}		55	–	–	mVo-p
PG hall 3'rd Min. voltage note	V_{H_P3}		75	–	–	mVo-p
PG hall 1'st-2'nd level note	ΔV_H		5	–	–	mVo-p
FG (FREQUENCY GENERATOR), PG (PHASE GENERATOR)						
FG, PG high level	FG_PG_H	–	4.5	–	–	V
FG, PG low level	FG_PG_L	–	–	–	0.5	V

NOTE: The note in the chart means items calculated and approved in design not the items proven by actual test results.

ELECTRICAL CHARACTERISTICS (Continued)

(Measured in test circuit, P_V_{CC}=12V, Ta=25°C)

Characteristic	Symbol	Test conditions	Spec.			Unit
			Min.	Typ.	max.	
TSD						
Temp. threshold note	TSD_T	–	130	150	-	°C
Temp. hysteresis note	TSD_H	–	20	30	-	°C
OUTPUT						
Output saturation voltage (Upper)	V_{SU1}	V_{CTL}=4V, I_O=600mA, R_{NF}=0.47Ω, R_L=10Ω	-	1.0	1.5	V
Output saturation voltage (Under)	V_{SD1}		-	0.4	0.7	V
NTL_IN- input voltage range	V_{NTL_IN-}	–	0	-	V_{CC}	V
C_{NF} voltage	V_{CNF}	V_{CTL}=2V	1	-	-	V
C_PK frequency	CPK_FRQ	C_PK=100Ω + 0.1μF	0.8	1	1.2	kHz
C_CK voltage level	CPK_V	C_PK=100Ω + 0.1μF HALL– =0.25V	0.4	-	-	Vp-p
C_DLY						
C_DLY charging current	I_{C_DLY}	C_DLY=4nF	-20	-30	-40	μA

NOTE: The note in the chart means items calculated and approved in design not the items proven by actual test results.

APPLICATION INFORMATION

1. ORGANIZATION OF SYSTEM

The figure 1-1 shows concept of soft switching for 3-phase output with a hall sensor.

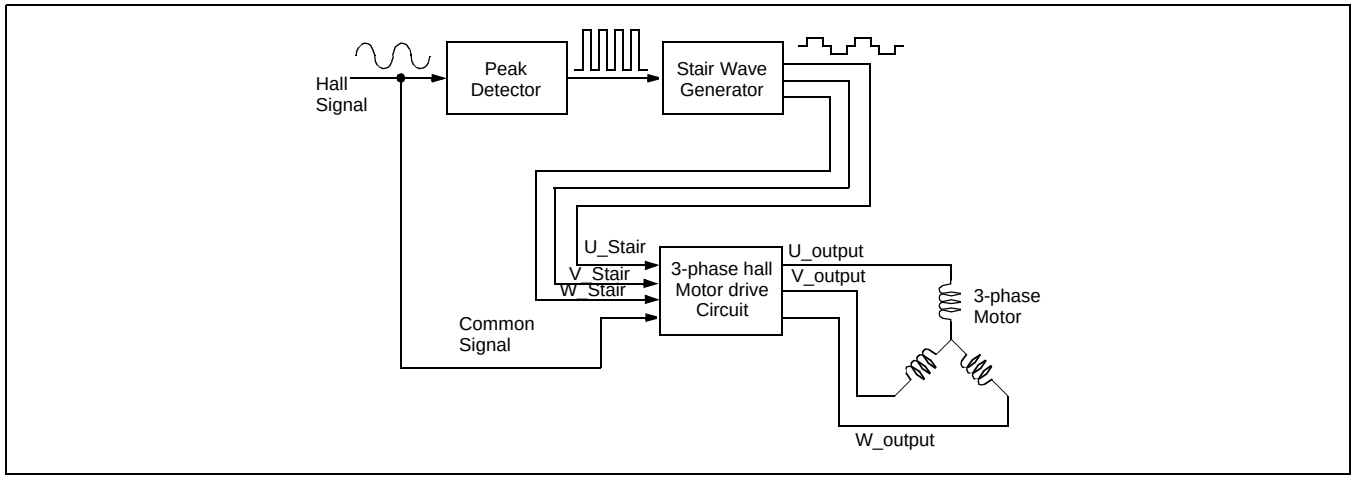


Figure 1-1.

- Peak detector
  Gets hall signals from hall sensor and generates clock pulses from the peak points of the hall signal.
- Stair wave generator
  Generates 3 stair wave signals with 120 degree different wave angles out of the clock pulses made from the peak detector.
- 3-phase motor drive circuit
  Controls output currents to operate 3-phase motor using the voltage difference between the 3 stair wave signals and FG hall signal. It's circuit for switching.

2. STRUCTURE OF BLDC MOTOR

Sub-magnet takes hall signal and go the through 6 gradual wave filtering steps purifying in order to operate 3-phase motor with one hall. For wave purification, the ratio between main-magnet and sub-magnet should maintain 1 main versus 3 subs as shown in the figure 2-1.

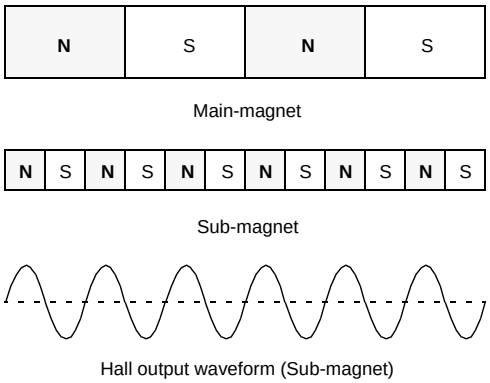
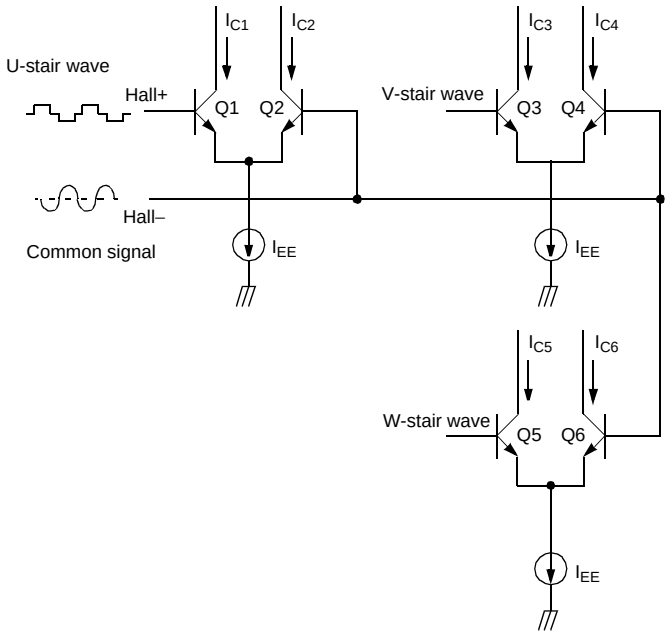


Figure 2-1.

3. PRINCIPLE OF OPERATION

Input circuit of 3-phase motor drive with soft-switching function is shown as the figure 3-1.



Hall–: Hall common signal taken from sub-magnet.
Hall+: Stairwave signal with 120 degree wave angle difference from one signal.

Figure 3-1.

Next the figure 3-2 shows common signal (Hall signal) and each individual stairwave at its own position.

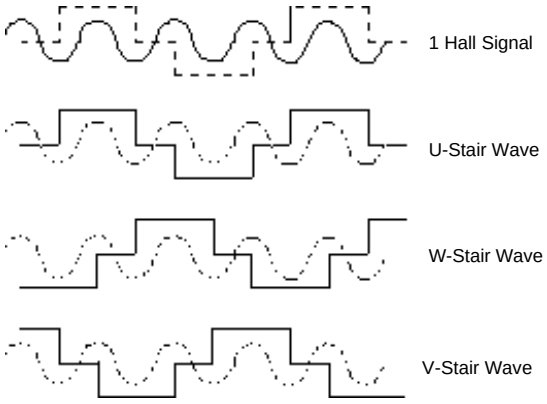
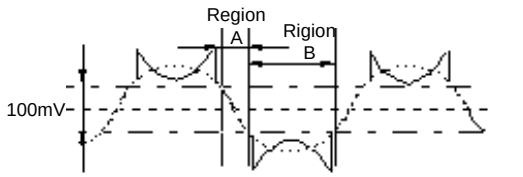
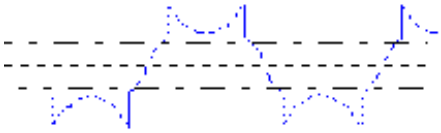


Figure 3-2.

And the figure 3-3 shows hall signal and the difference of each stairwave at its position. The section where the difference between hall signal and stairwave is within 100mV referring to hall bias shows the same as 3-phase motor drive with 3 halls in the figure 3-3. The other sections keep constant state regardless of hall signal size because output current is controlled by current source in input terminal the figure 3-1.



(a) The difference between 1 hall signal and U-stair wave



(b) The difference between 1 hall signal and V-stair wave

(c) The difference between 1 hall signal and W-stair wave

Figure 3-3.

4. PEAK DETECTOR

The signals used to operate motor are hall signals and stairwave made from peak detectors's output.
The peak detector is constructed with the following circuit (The figure 4-1)

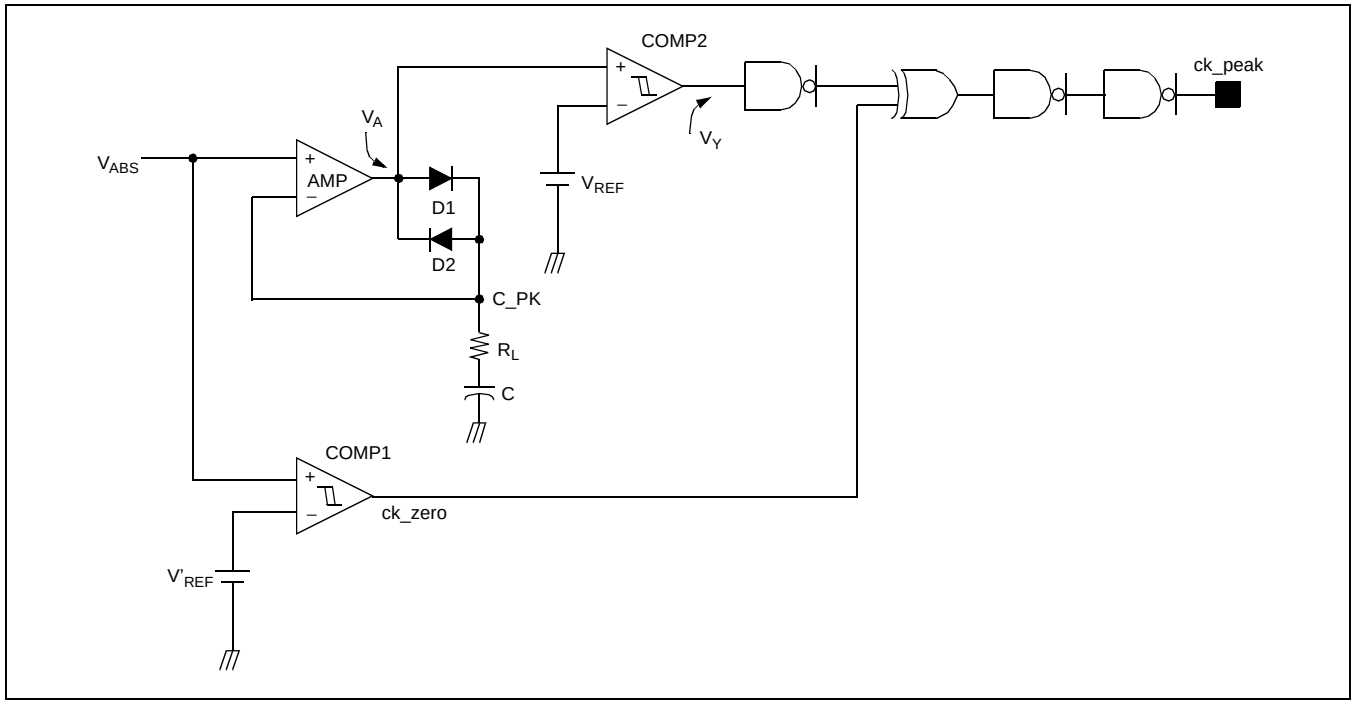


Figure 4.

V_{ABS} in the figure 4-1 is a signal from twice amplified hall signal and hall bias at 2.5 volt as standard voltage as you see in the figure 4-2.

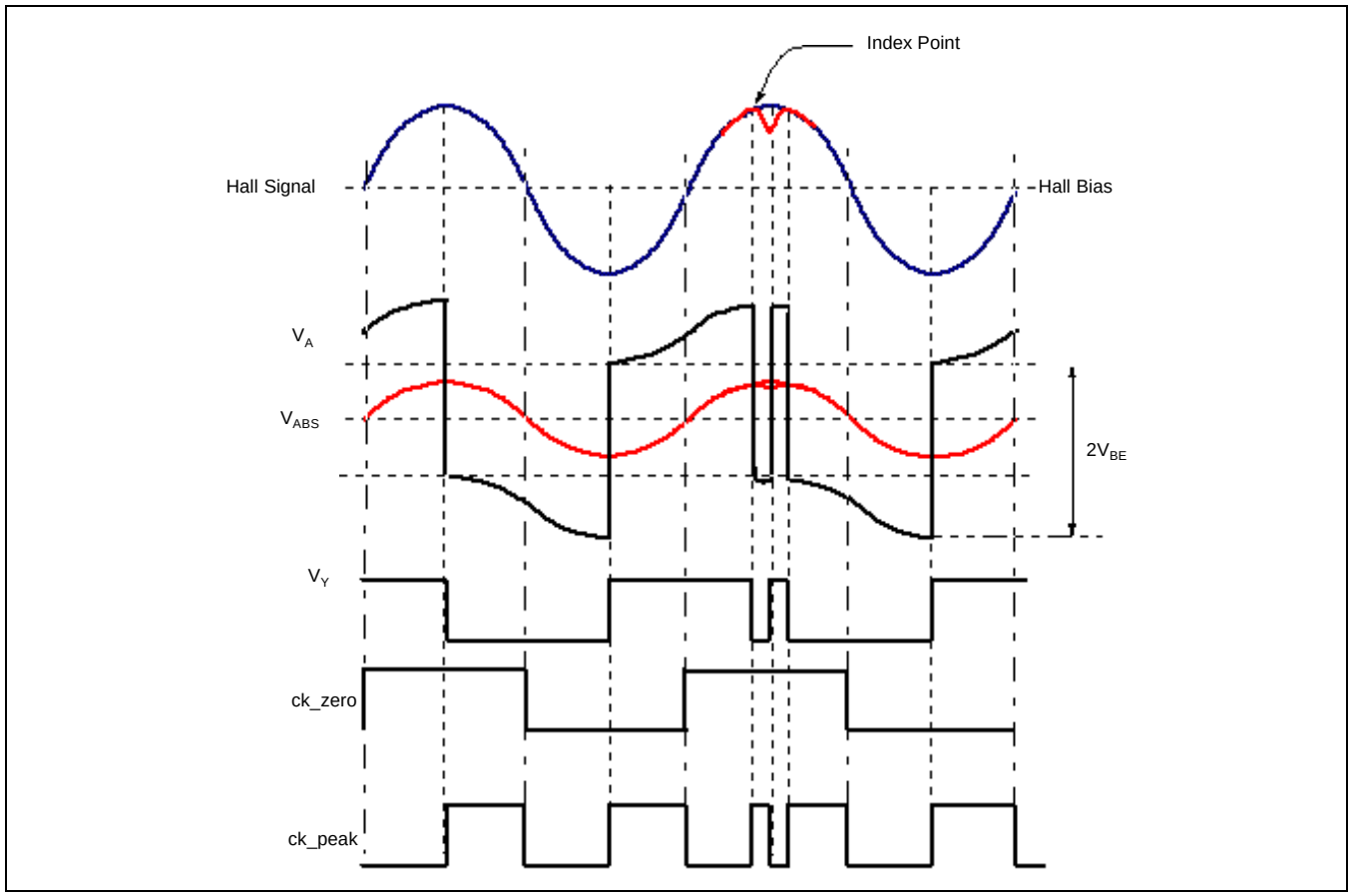


Figure 5.

V_{ABS} goes into COMP1 and AMP after that. Zero-crossing is done to the V_{ABS} signal into COMP1 to output ck_zero wave seen in the figure 4-2. And V_{ABS} signals into AMP comes out as V_A signal by following muchanism (1), (2) and (3).

1. When V_{ABS} increases from the lowest point to highest point.
   C_PK follows V_{ABS}'s shape by R_L and C and become charged. AMP outputs the same way.

2. When V_{ABS} decreases from the highest points.
   C_PK remains maximum status with no discharge path is available while D1 and D2 are off until the voltage difference with V_{ABS} is more than offset of AMP. Then, V_A which is output of AMP become deceased. When there is voltage difference more than 0.7V between Va and C_PK, D2 will be on to decease C_PK through emission from C as the same way as V_{ABS} signal. That time, V_A has the shape of V_{ABS} and outputs.

3. When V_{ABS} increases from the lower to highest point.
   C_PK remains its minimum status while V_{ABS} is increasing due to D1 is off. When the voltage difference between C_PK and V_{ABS} is bigger than offset of AMP, V_A which is output of AMP increases. When the voltage difference between V_A and C_PK is more than 0.7V, D1 will be on and discharge from C increases C_PK which will follow the same shape as VABS. That time VA with the same shape as VABS outputs.
   The final output ck_peak signal is made by outputs of COMP1 and COMP2.

5. CHECKING THE INDEX SIGN

Reversed embodied magnet (magnet with opposite polaris) is needed for sub-magnet to detect motor's index point as the hall signal shown in the figure 4-2.
The peak detector output from compounded magnet generates 2 clock pulses in half cycle.
The first clock pulse is used for filter motor's pulse wave and the other is used as index signal.
The index signal checks commutation of motor once for each rotation and offer reference point for data checking.

6. DRIVE OUTPUT

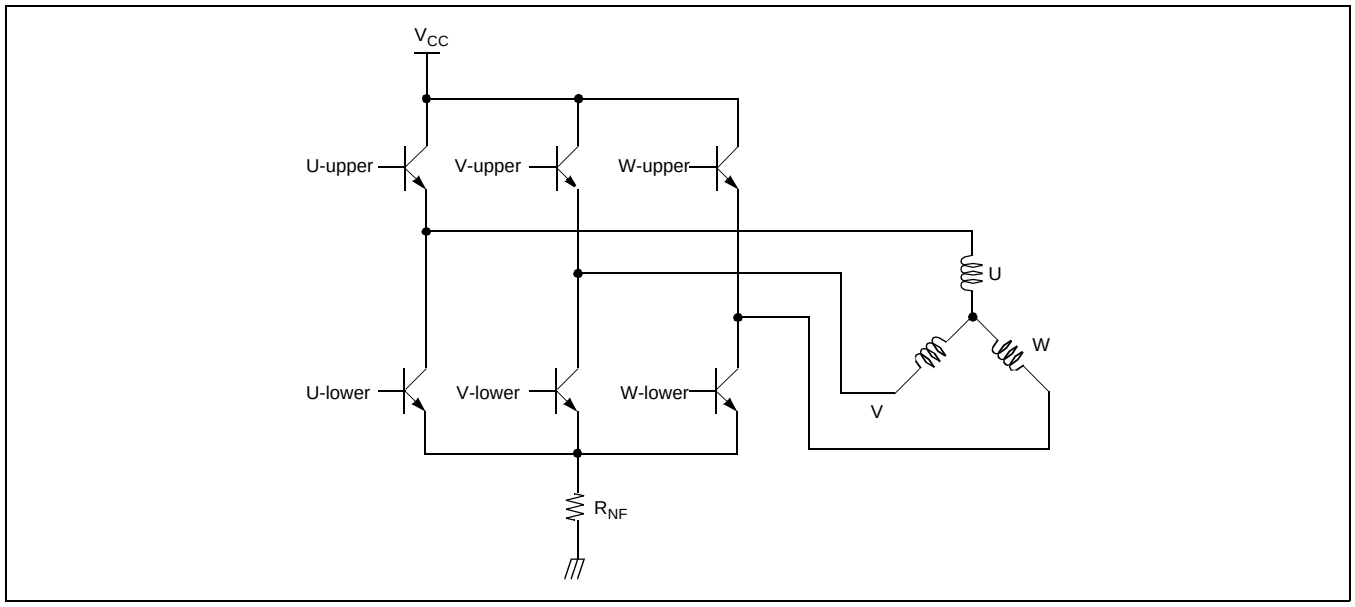


Figure 6-1.

The figure 6-1 shows the 3-phase mechanism. When one phase of upper power TR is on, 1 phase of the other lower TR becomes on and the rest power TR becomes off. This is the way to continuing commutation to right direction to operate motor.

The upper power TRs in output group operate in linear area and the lower group work in saturation area.

7. VOLTAGE CONTROL & CURRENT SENSING

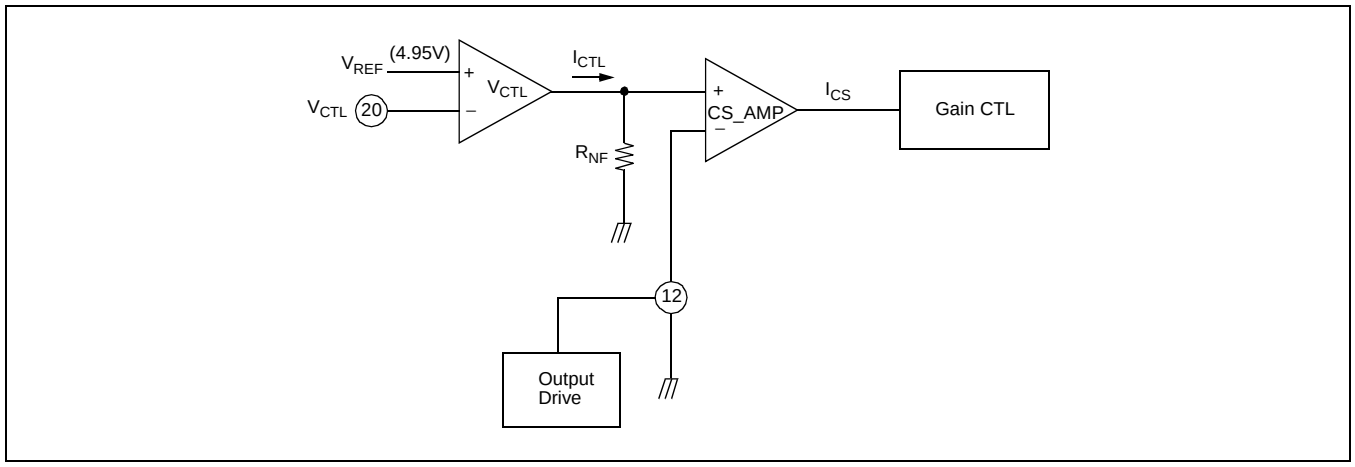


Figure 7-1.

The circuit in the figure 7-1 is to outputting I_{CTL} current when V_{CTL} (Control voltage from servo) becomes bigger than the value of V_{REF}. The V-I characteristic of this circuit is shown in the figure 7-2.

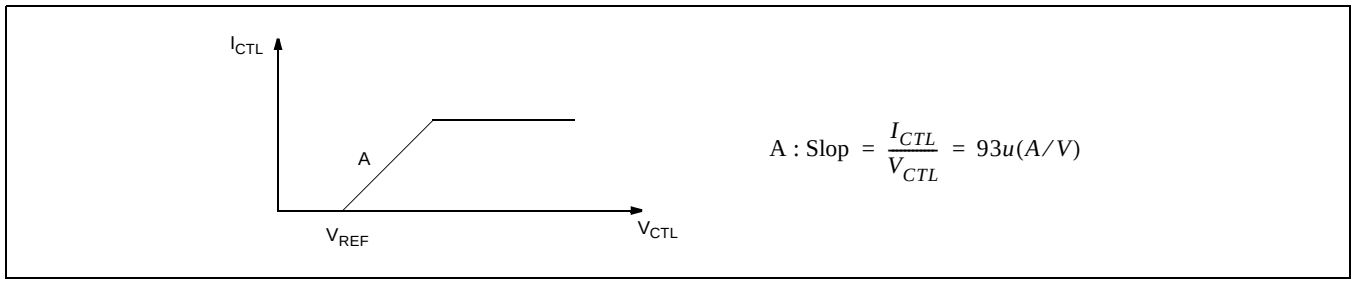


Figure 7-2.

The CS-AMP terminal amplifies by getting inputs from output terminal getting I_{CTL} and R_{NF} voltages.

R_{NF} resistance feedbacks the current in output terminal.

8. SHIFTOR

The function of this circuit is to delay PG signal generated by FG, PG generator using pin 2 (C_DLY) as shown in the figure 8-1.

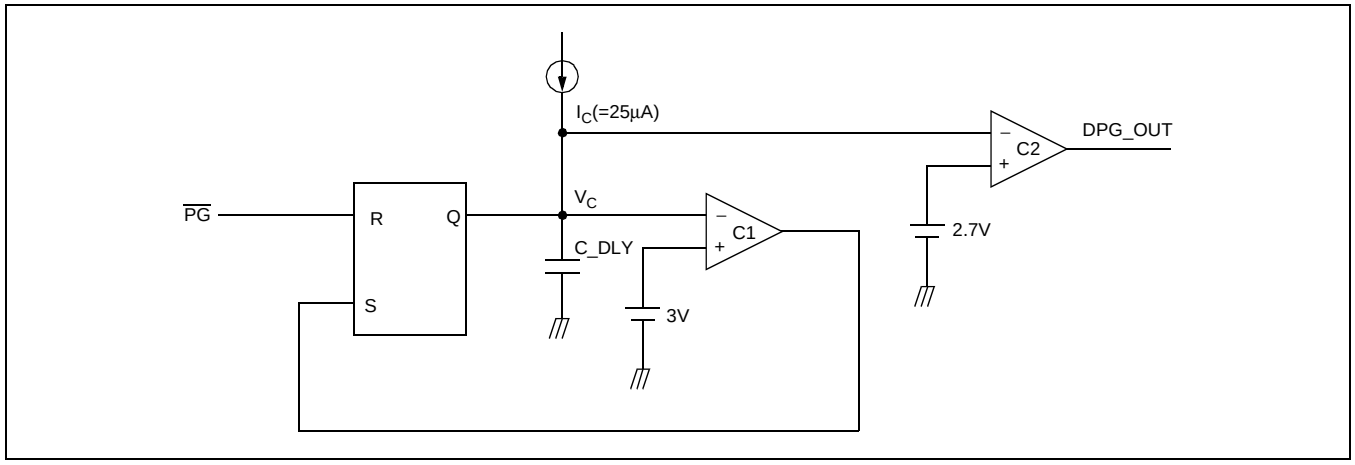


Figure 8-1.

The figure 8-2 shows the output wave shapes in each block of the circuit in figure 8-1.

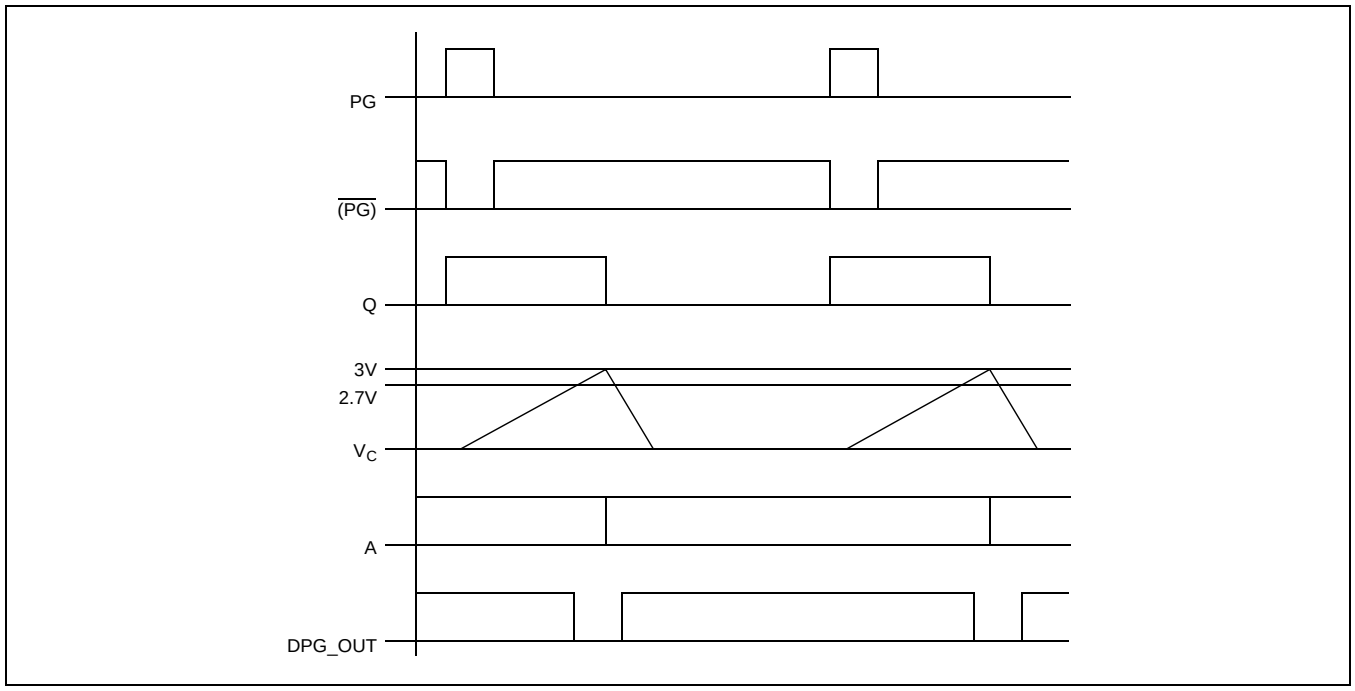
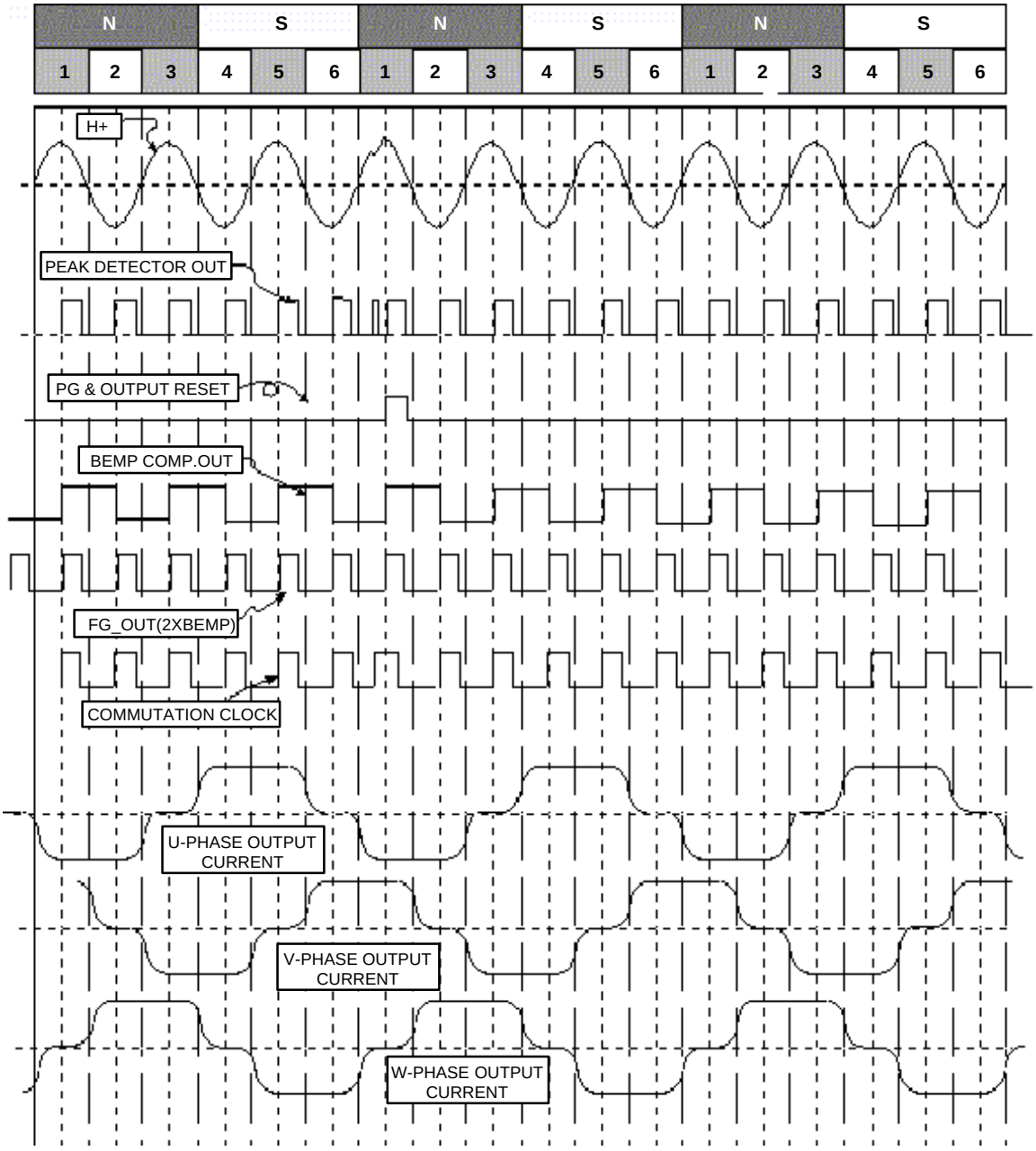
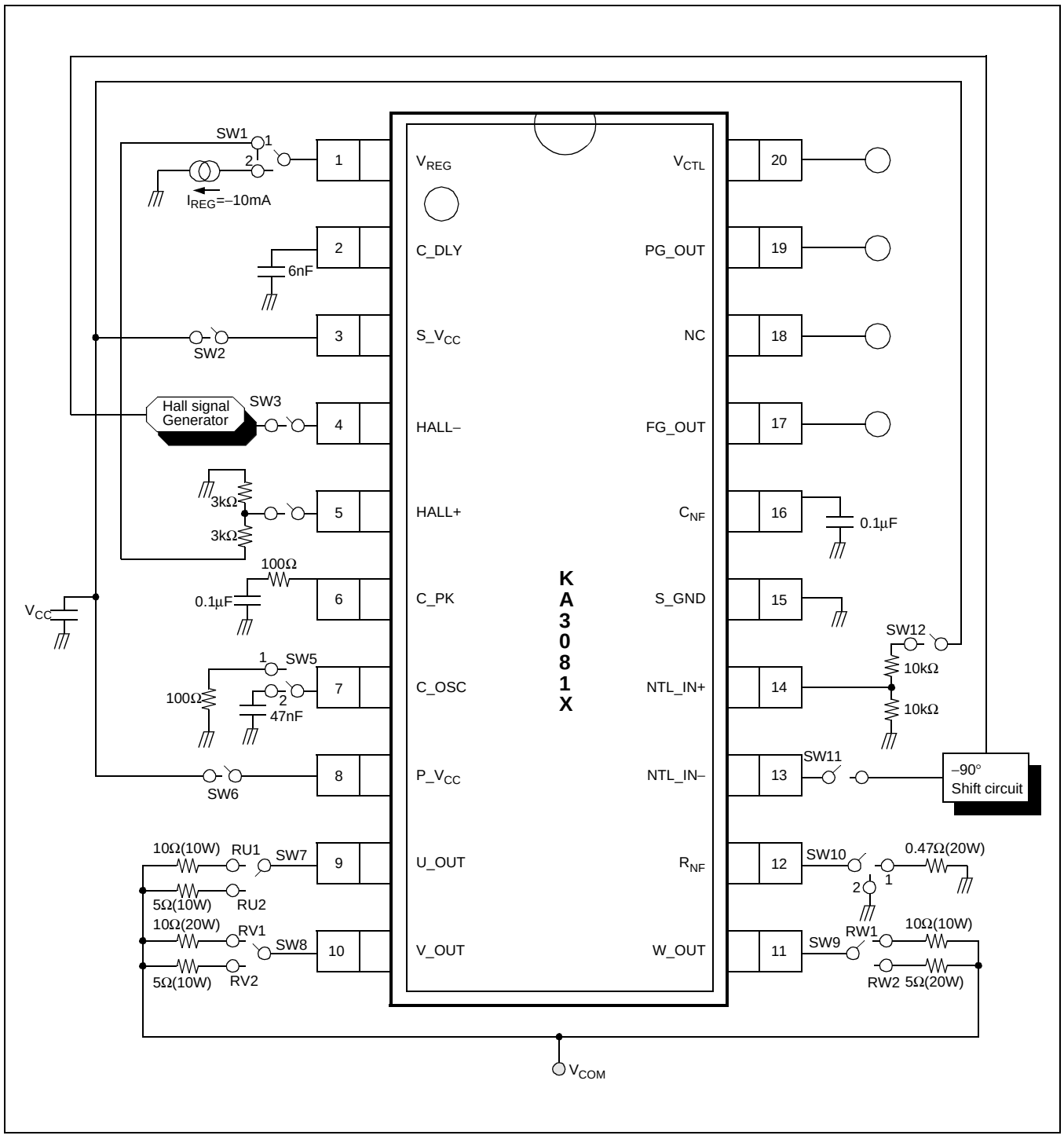


Figure 8-2.

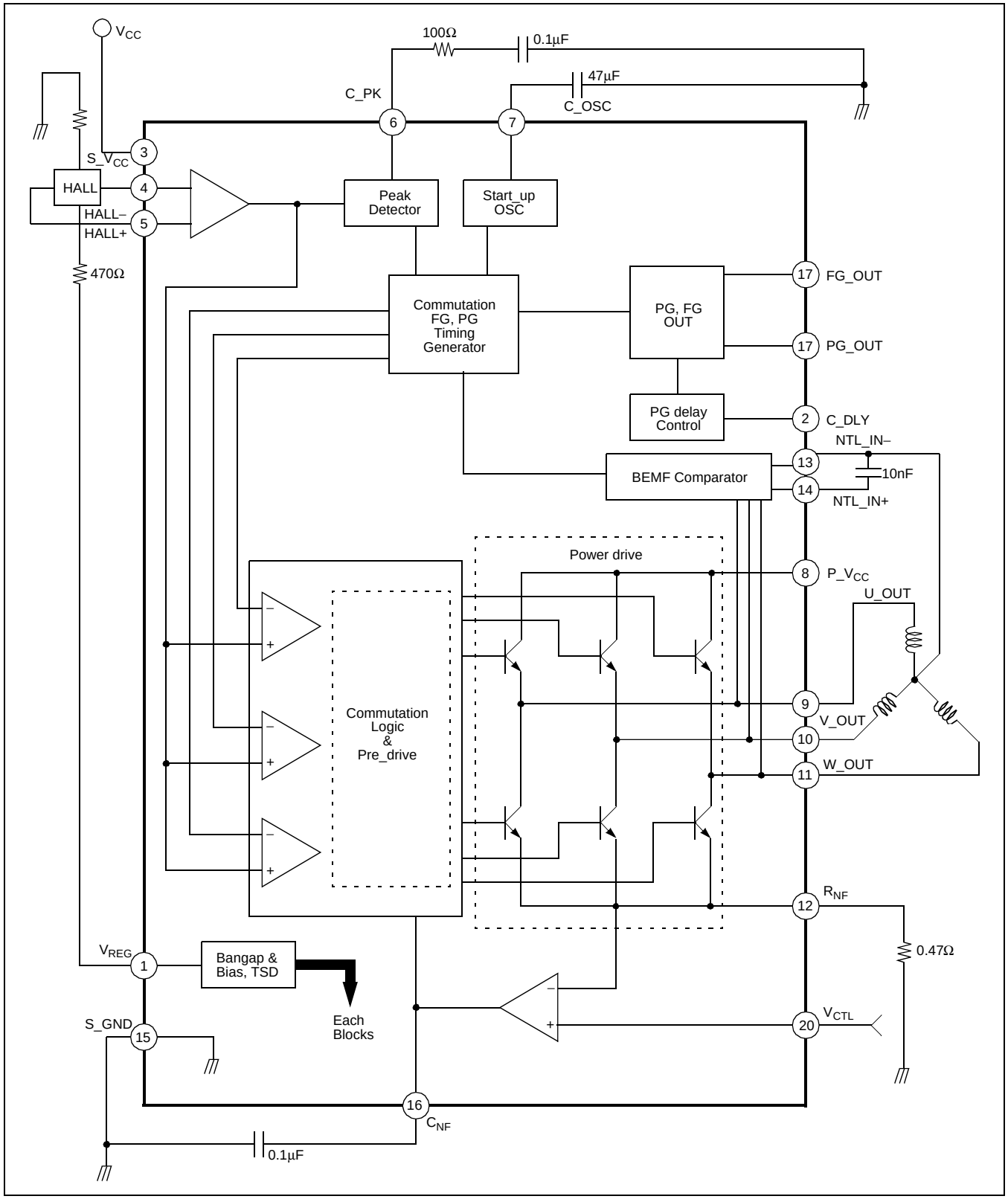
TIMING CHART



TEST CIRCUITS



TYPICAL APPLICATIONS



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No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
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