

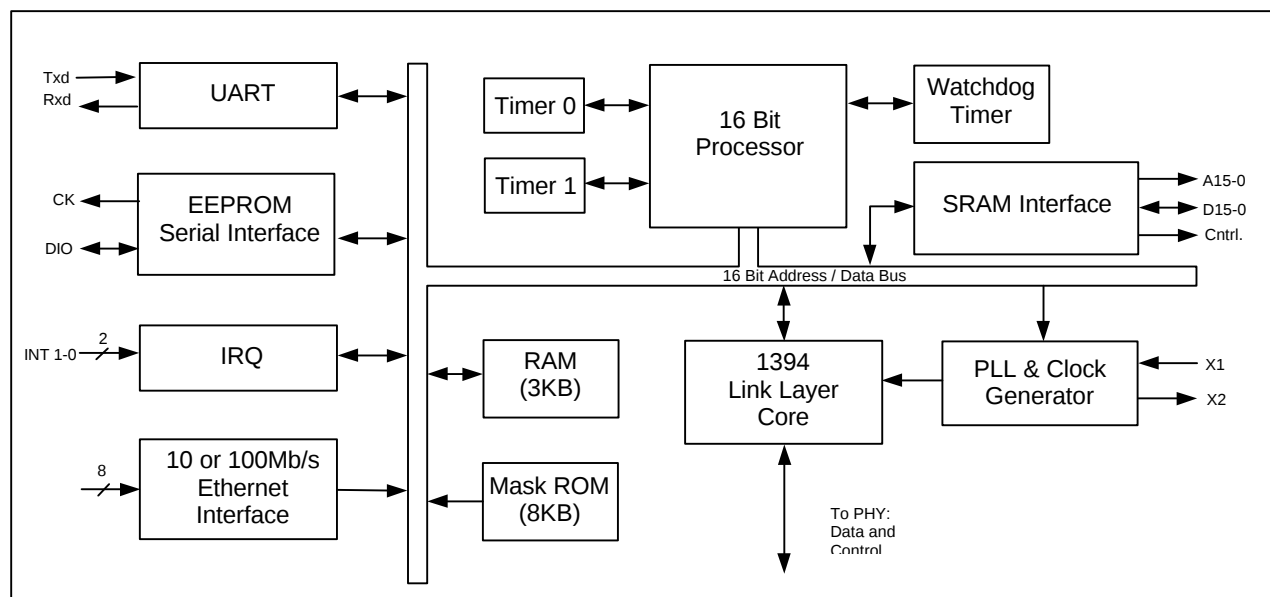
General Description

The Kawasaki Firewire to Ethernet Controller is a unique single chip solution to interface the 1394 Firewire and Ethernet. The controller has been specifically designed to provide a simple solution to communicate with Ethernet applications. This has been accomplished by its highly integrated functionality. The Firewire 1394 controller consists of a central 16-bit processor, mask ROM, RAM buffer, clock generator, Ethernet interface, UART, IRQ, Watchdog Timer, Serial interface, External Memory Interface and SPORT Interface. The Firewire interface is fully compatible with the 1394 specifications. This Firewire to Ethernet controller is ideal for LAN (Local Area Network), Cable Modem, or Mobile Networking applications.

Features

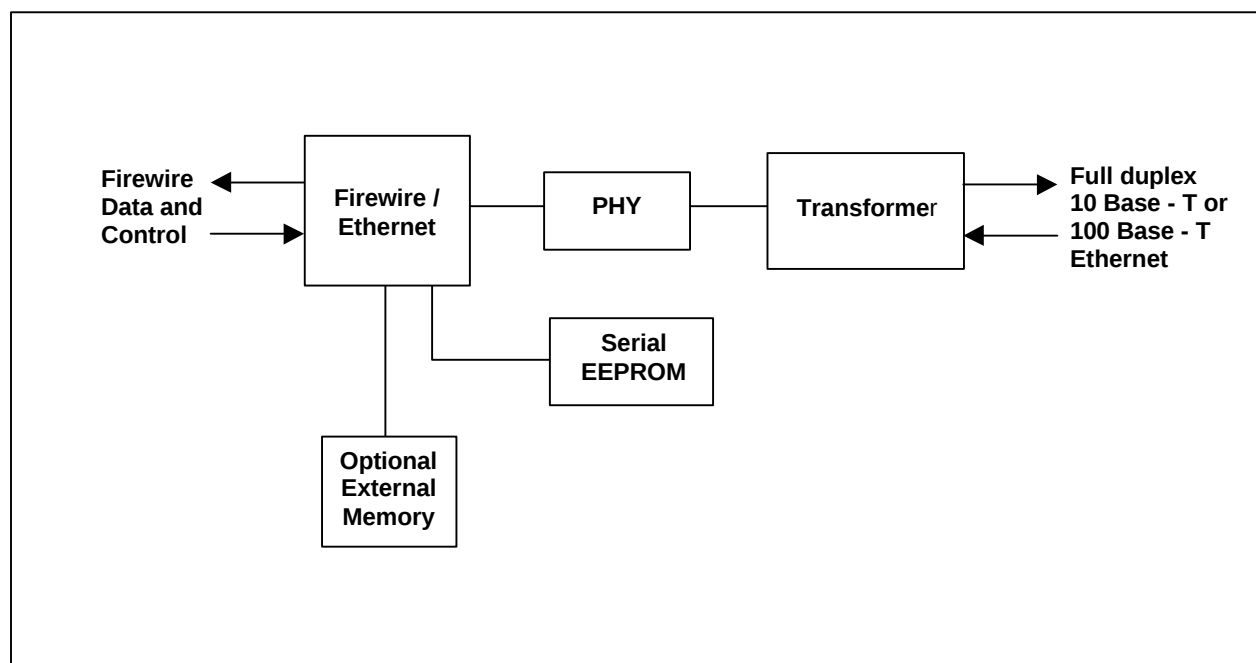
- Advanced 16 Bit processor for 1394 transaction processing and control data processing
- IEEE 802.3 Ethernet Standard
- 1394 Link Layer Core - IEEE P1394 compliant
- Internal Clock Generation
- Utilizes low cost external crystal circuitry
- 2K x 32 Internal RAM buffer
- Serial Interface for external EEPROM
- Watchdog timer
- Fully IEEE 802.3 compliant 10/100 Mbit/sec Ethernet MAC Layer. Interfaces serially of an external ENDEC PHY.
- Debug UART supports 900 baud to 115.2K baud.
- External memory interface
- 100 pin LQFP package

Block Diagram



PRELIMINARY

Application Block Diagram



Pin Description - Preliminary

Pin Number	Direction	Pin Name	Description
16	IN	PHTXCLK	Transmit clock from E-NET PHY
17	IN	PHRXCLK	Receive clock from E-NET PHY
18	IN	PHCRS	Carrier Sense from E-NET PHY
19	IN	PHCOL	Collision Detect from E-NET PHY
20	IN	PHRXDV	Receive Data Valid from E-NET PHY
21	IN	PHRXER	Receive Data Error from E-NET PHY
22	OUT	PHTXEN	E-NET PHY Transmit Enable
23	OUT	PH_TXD1	E-NET PHY Serial Transmit Data
24	IN/OUT	TXD	UART TXD
36	IN/OUT	RXD	UART RXD
37	IN	IRQ0	Edge sens. Interrupt
38	IN	IRQ1	Edge sens. Interrupt
39	IN	PH_RXD1	E-NET PHY Serial Receive Data
40	OUT	PH_TXD2	E-NET PHY Serial Transmit Data
41	IN	PH_RXD2	E-NET PHY Serial Receive Data
42	OUT	PH_TXD3	E-NET PHY Serial Transmit Data

PRELIMINARY

Pin Number	Direction	Pin Name	Description
43	IN	PH_RXD3	E-NET PHY Serial Receive Data
44	OUT	A15	Optional Extended Add. Bits
45	OUT	A14	Optional Extended Add. Bits
46	OUT	A0	Optional Extended Add. Bits
47	OUT	nXBHE	External Byte High Enable (active LO)
51	OUT	nXRAMSEL	External RAM CS (active LO)
54	IN/OUT	GPIO0	GPIO0
55	IN/OUT	GPIO1	GPIO1
56	IN/OUT	GPIO2	GPIO2
58	IN/OUT	GPIO3	GPIO3
59	IN/OUT	GPIO4	GPIO4
60	IN/OUT	GPIO5	GPIO5
61	IN/OUT	GPIO6	GPIO6
62	IN/OUT	GPIO7	GPIO7
63	IN/OUT	GPIO8	GPIO8
64	IN/OUT	GPIO9	GPIO9
13	IN/OUT	GPIO10	GPIO10
12	IN/OUT	GPIO11	GPIO11
11	IN/OUT	GPIO12	GPIO12
10	IN/OUT	GPIO13	GPIO13
9	IN/OUT	GPIO14	GPIO14
8	IN/OUT	GPIO15	GPIO15
7	OUT	LPS	1394
6	IN	SCLK	1394
26	OUT	LREQ	1394
27	IN/OUT	C1	1394
29	IN/OUT	C0	1394
30	IN/OUT	D7	1394
31	IN/OUT	D6	1394
32	IN/OUT	D5	1394
33	IN/OUT	D4	1394
34	IN/OUT	D3	1394
35	IN/OUT	D2	1394
49	IN/OUT	D1	1394
50	IN/OUT	D0	1394
66	OUT	PHTXER	E-NET PHY Transmit Error
67	OUT	PH_TXD0	E-NET PHY Serial Transmit Data
68	IN	PH_RXD0	E-NET PHY Serial Receive Data

PRELIMINARY

Pin Number	Direction	Pin Name	Description
69	IN/OUT	X_PCLK	External PCLK
70	IN	CLK	50MHz Clock/Crystal Input
71	OUT	X2	50MHz Crystal Output
72	OUT	nXRD	External Memory Read (active LO)
73	OUT	nXWR	External Memory Write (active LO)
74	OUT	nXROMSEL	External ROM CS (active LO)
75	IN	nRESET	Reset Pin
76	IN	nTST	Test Pin, N/C for Normal Operation
77	OUT	XA_1	External Address Pins
78	OUT	XA_2	External Address Pins
79	OUT	XA_3	External Address Pins
80	OUT	XA_4	External Address Pins
81	OUT	XA_5	External Address Pins
82	OUT	XA_6	External Address Pins
83	OUT	XA_7	External Address Pins
84	OUT	XA_8	External Address Pins
85	OUT	XA_9	External Address Pins
86	OUT	XA_10	External Address Pins
87	OUT	XA_11	External Address Pins
88	OUT	XA_12	External Address Pins
89	OUT	XA_13	External Address Pins
90	IN/OUT	XD_0	External Data Pins
91	IN/OUT	XD_1	External Data Pins
92	IN/OUT	XD_2	External Data Pins
93	IN/OUT	XD_3	External Data Pins
94	IN/OUT	XD_4	External Data Pins
95	IN/OUT	XD_5	External Data Pins
97	IN/OUT	XD_6	External Data Pins
98	IN/OUT	XD_7	External Data Pins
100	IN/OUT	XD_8	External Data Pins
1	IN/OUT	XD_9	External Data Pins
3	IN/OUT	XD_10	External Data Pins
4	IN/OUT	XD_11	External Data Pins
5	IN/OUT	XD_12	External Data Pins
14	IN/OUT	XD_13	External Data Pins
15	IN/OUT	XD_14	External Data Pins
25	IN/OUT	XD_15	External Data Pins
28	IN	GND	GND

PRELIMINARY

Pin Number	Direction	Pin Name	Description
31	IN	GND	GND
34	IN	GND	GND
48	IN	GND	GND
52	IN	VDD	VDD
53	IN	VDD	VDD
57	IN	VDD	VDD

Function Description

16 Bit Processor

The integrated 16-bit processor serves as a micro controller for 1394 peripherals. The processor can execute approximately five million instructions per second. With this processing power it allows the design of intelligent peripherals that can process data prior to passing it on to the host PC, thus improving overall performance of the system. The masked ROM (8K X 32) in the KLSI device or external memory contains a specialized instruction set that has been designed for highly efficient coding of processing algorithms and 1394 transaction processing.

The 16-bit processor is designed for efficient data execution by having direct access to the RAM Buffer, external memory, I/O interfaces, and all the control and status registers. The divide/multiply feature expands the capability of 1394 peripherals.

The processor supports prioritized vectored hardware interrupts. In addition, as many as 240 software interrupt vectors are available.

The processor provides six addressing modes, supporting memory-to-memory, memory-to-register, register-to-register, immediate-to-register or immediate-to-memory operations. Register, direct, immediate, indirect and indirect indexed addressing modes are supported. In addition, there is an auto-increment mode in which a register, used as an address pointer is automatically incremented after each use, making repetitive operations more efficient both from a programming and a performance standpoint.

The processor features a full set of program control, logical, and integer arithmetic instructions. All instructions are sixteen bits wide, although some instructions require operands, which may occupy another one or two words. Several special "short immediate" instructions are available, so that certain frequently used operations with small constant operand will fit into a 16-bit instruction.

PRELIMINARY

The Processor – Divide/Multiply function

The processor's divide/multiply function contains all the instructions of the base processor that additionally includes integer divide and multiply instructions. A signed multiply instruction takes two 16-bit operands and returns a 32-bit result. A signed divide instruction divides a 32-bit operand by a 16-bit operand.

RAM Buffer

The EFIRE Controller contains a 8K byte internal SRAM memory, organized as 2K X 32. The memory is used to buffer data, Ethernet and 1394 packets and is accessed by the 16 Bit processor, the Ethernet and 1394 DMA controllers.

Ethernet and 1394 transactions are routed to the memory buffer through 6 separate DMA controllers. The 16-bit processor has the ability to set up pointers and block sizes in buffer memory for Ethernet and 1394 transactions. Data is read from the interfaces and is processed and packetized by the 16-bit I/O processor.

PLL Clock Generator

The PLL circuitry is provided to generate the internal clock requirements. This circuitry is designed to allow use of low cost external. If an external clock is available in the application, it may be used in lieu of the crystal circuit.

1394 Interface

The EFIRE Link Layer Core controller meets the IEEE P1394 Serial Bus Specification. The EFIRE controller interfaces to an external PHY 1394 Transceiver chip.

10/100 Mb/s Ethernet Interface

The EFIRE Controller has a built in 10/100 Mbit/second Ethernet MAC Layer that is fully compliant with the IEEE 802.3 Ethernet standard. The EFIRE connects externally to a 10/100-Base-T ENDEC PHY. The EFIRE Controller 16 bit processor has direct access to the registers of the ENET MAC.

UART Interface

Supports a transfer rate of 900 to 115.2K bauds.

PRELIMINARY**Serial EEPROM Support**

The EFIRE Controller serial interface can be used to provide access to external EEPROM's. The interface is implemented using General Purpose I/O signals and can support a variety of serial EEPROM formats.

SRAM Interface

An address port and 16-bit data port has been provided to interface to an external SRAM.

General Purpose I/O

Up to 16 general purpose I/O signals are available. However, most GPIO may be configured for special purpose functions such as UART, Digital Input. etc.

RAM/ROM Interface

A multiplexed address port and 16-bit data port has been provided to interface to an external RAM or ROM.

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