1Mx36 & 2Mx18-Bit Synchronous Burst SRAM

FEATURES

- Synchronous Operation.
- On-Chip Address Counter.
- Self-Timed Write Cycle.
- On-Chip Address and Control Registers.
- 3.3V+0.165V/-0.165V Power Supply.
- I/O Supply Voltage 3.3V+0.165V/-0.165V for 3.3V I/O or 2.5V+0.4V/-0.125V for 2.5V I/O
- 5V Tolerant Inputs Except I/O Pins.
- Byte Writable Function.
- Global Write Enable Controls a full bus-width write.
- Power Down State via ZZ Signal.
- $\overline{LBO}$ Pin allows a choice of either a interleaved burst or a linear burst.
- Three Chip Enables for simple depth expansion with No Data Contention only for TQFP.
- Asynchronous Output Enable Control.
- $\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$ Burst Control Pins.
- TTL-Level Three-State Output.
- 100-TQFP-1420A /119BGA(7x17 Ball Grid Array Package)

FAST ACCESS TIMES

PARAMETER	Symbol	-65	-75	-85	-90	Unit
Cycle Time	t_{CYC}	7.5	8.5	10	10	ns
Clock Access Time	t_{CD}	6.5	7.5	8.5	9.0	ns
Output Enable Access Time	t_{OE}	3.5	3.5	4.0	4.0	ns

GENERAL DESCRIPTION

The K7B323625M and K7B321825M are 37,748,736-bit Synchronous Static Random Access Memory designed for high performance second level cache of Pentium and Power PC based System.

It is organized as 1M(2M) words of 36(18) bits and integrates address and control registers, a 2-bit burst address counter and added some new functions for high performance cache RAM applications; $\overline{GW}$, $\overline{BW}$, $\overline{LBO}$, ZZ. Write cycles are internally self-timed and synchronous.

Full bus-width write is done by $\overline{GW}$, and each byte write is performed by the combination of $\overline{WE}x$ and $\overline{BW}$ when $\overline{GW}$ is high. And with $\overline{CS_1}$ high, $\overline{ADSP}$ is blocked to control signals.

Burst cycle can be initiated with either the address status processor($\overline{ADSP}$) or address status cache controller($\overline{ADSC}$) inputs. Subsequent burst addresses are generated internally in the system's burst sequence and are controlled by the burst address advance($\overline{ADV}$) input.

$\overline{LBO}$ pin is DC operated and determines burst sequence(linear or interleaved).

ZZ pin controls Power Down State and reduces Stand-by current regardless of CLK.

The K7B323625M and K7B321825M are fabricated using SAMSUNG's high performance CMOS technology and is available in a 100pin TQFP and 119BGA package. Multiple power and ground pins are utilized to minimize ground bounce.

LOGIC BLOCK DIAGRAM