Document Title

512Kx36 & 1Mx18-Bit Synchronous Pipelined Burst SRAM

Revision History

Rev. No.	History	Draft Date	Remark
0.0	1. Initial draft	Feb. 23. 2001	Preliminary
0.1	1. Add JTAG Scan Order	May. 10. 2001	Preliminary

16Mb SB/SPB Synchronous SRAM Ordering Information

Org.	Part Number	Mode	VDD	Speed SB ; Access Time(ns) SPB ; Cycle Time(MHz)	PKG	Temp
1Mx18	K7B161825A-Q(H)C65/75/85/90	SB	3.3	6.5/7.5/8.5/9.0ns	Q : 100TQFP H : 119BGA	C (Commercial Temperature Range)
	K7A161800A-Q(H)C16/15/14	SPB(2E1D)	3.3	167/150/138MHz		
	K7A161809A-Q(H)C25/22/20	SPB(2E1D)	3.3	250/225/200MHz		
	K7A161801A-QC16/15/14	SPB(2E2D)	3.3	167/150/138MHz		
	K7A161808A-QC25/22/20	SPB(2E2D)	3.3	250/225/200MHz		
512Kx36	K7B163625A-Q(H)C65/75/85/90	SB	3.3	6.5/7.5/8.5/9.0ns		
	K7A163600A-Q(H)C16/15/14	SPB(2E1D)	3.3	167/150/138MHz		
	K7A163609A-Q(H)C25/22/20	SPB(2E1D)	3.3	250/225/200MHz		
	K7A163601A-QC16/15/14	SPB(2E2D)	3.3	167/150/138MHz		
	K7A163608A-QC25/22/20	SPB(2E2D)	3.3	250/225/200MHz		

512Kx36 & 1Mx18-Bit Synchronous Pipelined Burst SRAM

FEATURES

- Synchronous Operation.
- 2 Stage Pipelined operation with 4 Burst.
- On-Chip Address Counter.
- Self-Timed Write Cycle.
- On-Chip Address and Control Registers.
- V_{DD} = 3.3V +0.165V/-0.165V Power Supply.
- I/O Supply Voltage 3.3V +0.165V/-0.165V for 3.3V I/O or 2.5V+0.4V/-0.125V for 2.5V I/O.
- 5V Tolerant Inputs Except I/O Pins.
- Byte Writable Function.
- Global Write Enable Controls a full bus-width write.
- Power Down State via ZZ Signal.
- $\overline{LBO}$ Pin allows a choice of either a interleaved burst or a linear burst.
- Three Chip Enables for simple depth expansion with No Data Contention only for TQFP ; 2cycle Enable, 1cycle Disable.
- Asynchronous Output Enable Control.
- $\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$ Burst Control Pins.
- TTL-Level Three-State Output.
- 100-TQFP-1420A / 119BGA(7x17 Ball Grid Array Package)

FAST ACCESS TIMES

PARAMETER	Symbol	-25	-22	-20	Unit
Cycle Time	tCYC	4.0	4.4	5.0	ns
Clock Access Time	tCD	2.6	2.8	3.1	ns
Output Enable Access Time	tOE	2.6	2.8	3.1	ns

GENERAL DESCRIPTION

The K7A163609A and K7A161809A are 18,874,368-bit Synchronous Static Random Access Memory designed for high performance second level cache of Pentium and Power PC based System.

It is organized as 512K(1M) words of 36(18) bits and integrates address and control registers, a 2-bit burst address counter and added some new functions for high performance cache RAM applications; $\overline{GW}$, $\overline{BW}$, $\overline{LBO}$, ZZ. Write cycles are internally self-timed and synchronous.

Full bus-width write is done by $\overline{GW}$, and each byte write is performed by the combination of $\overline{WE}$x and $\overline{BW}$ when $\overline{GW}$ is high. And with $\overline{CS}_1$ high, $\overline{ADSP}$ is blocked to control signals.

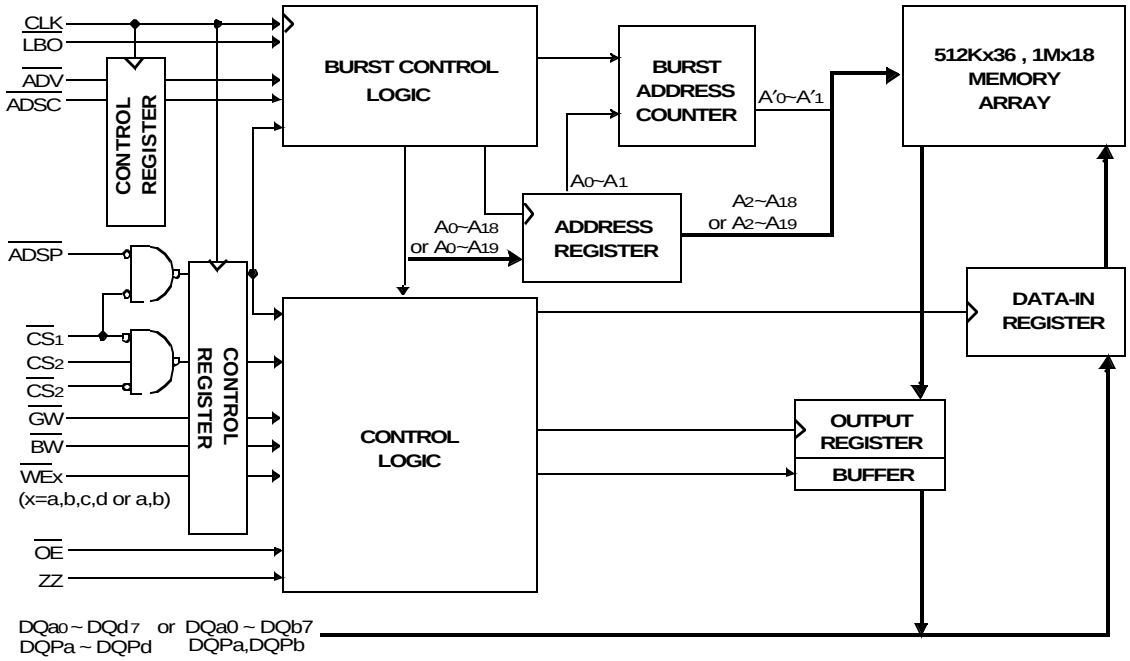
Burst cycle can be initiated with either the address status processor($\overline{ADSP}$) or address status cache controller($\overline{ADSC}$) inputs. Subsequent burst addresses are generated internally in the system's burst sequence and are controlled by the burst address advance($\overline{ADV}$) input.

$\overline{LBO}$ pin is DC operated and determines burst sequence(linear or interleaved).

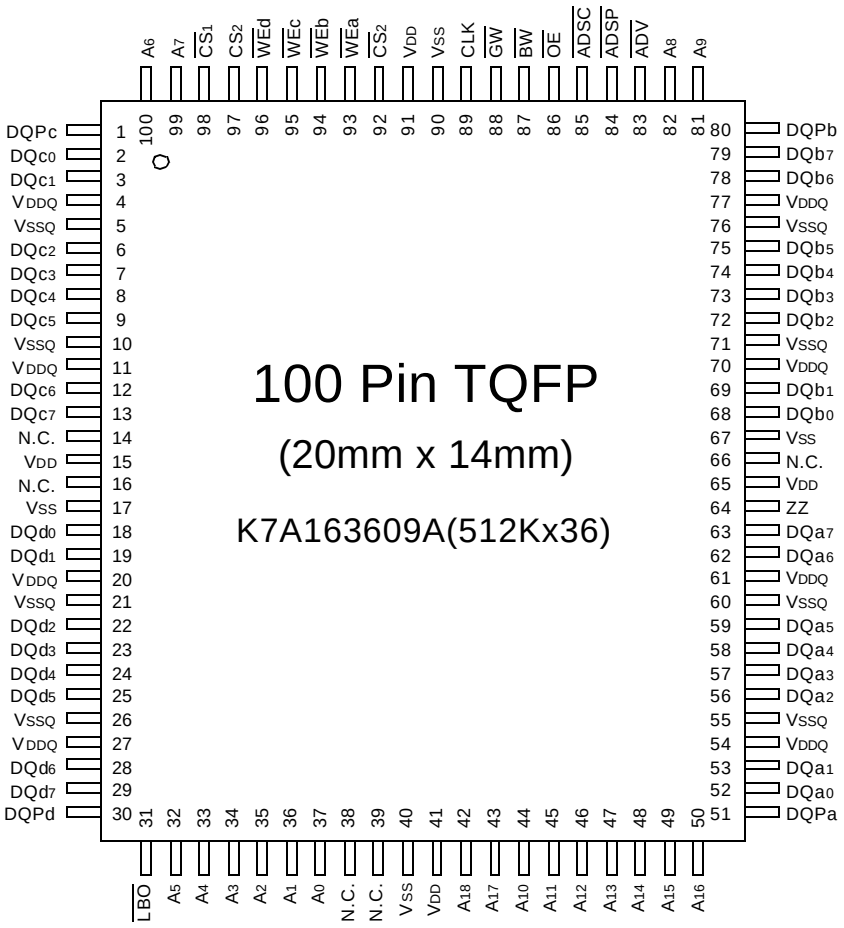
ZZ pin controls Power Down State and reduces Stand-by current regardless of CLK.

The K7A163609A and K7A161809A are fabricated using SAMSUNG's high performance CMOS technology and is available in a 100pin TQFP and 119BGA package. Multiple power and ground pins are utilized to minimize ground bounce.

LOGIC BLOCK DIAGRAM



PIN CONFIGURATION(TOP VIEW)

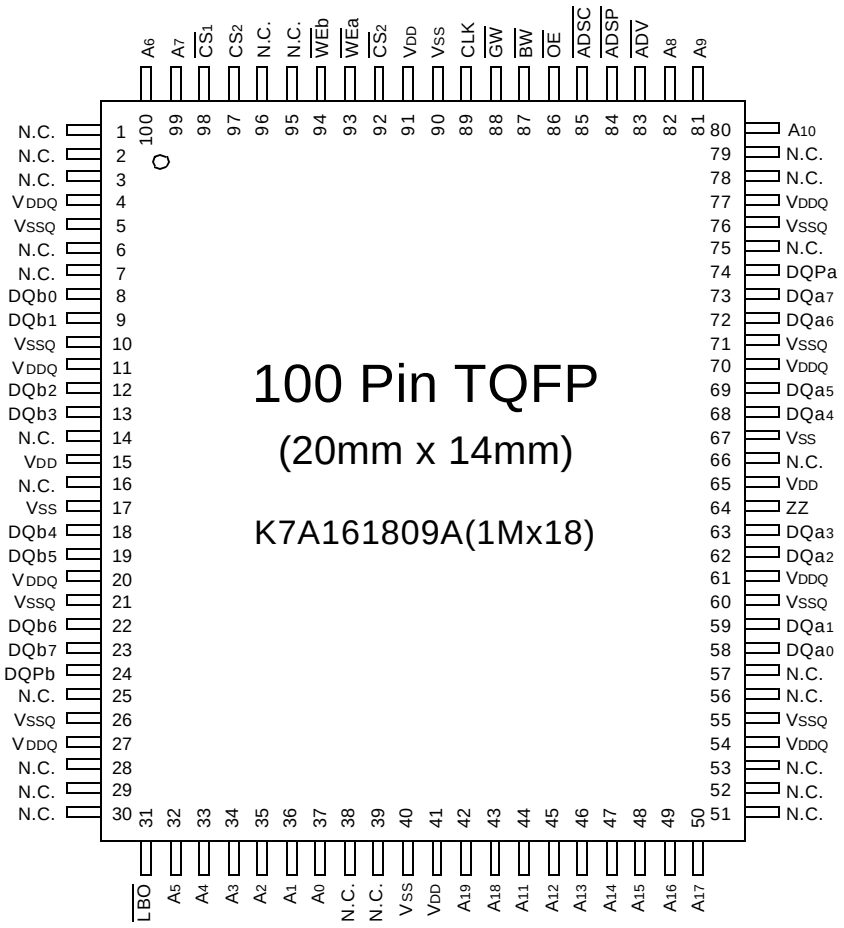


PIN NAME

SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A_0 - A_{18}	Address Inputs	32,33,34,35,36,37,42 43,44,45,46,47,48,49 50,81,82,99,100	V_{DD}	Power Supply(+3.3V)	15,41,65,91
			V_{SS}	Ground	17,40,67,90
$\overline{ADV}$	Burst Address Advance	83	N.C.	No Connect	14,16,38,39,66
$\overline{ADSP}$	Address Status Processor	84			
$\overline{ADSC}$	Address Status Controller	85	$DQa_{0\sim7}$	Data Inputs/Outputs	52,53,56,57,58,59,62,63
CLK	Clock	89	$DQb_{0\sim7}$		68,69,72,73,74,75,78,79
$\overline{CS_1}$	Chip Select	98	$DQc_{0\sim7}$		2,3,6,7,8,9,12,13
CS_2	Chip Select	97	$DQd_{0\sim7}$		18,19,22,23,24,25,28,29
$\overline{CS_2}$	Chip Select	92	$DQPa\sim Pd$		51,80,1,30
$\overline{WEx}$(x=a,b,c,d)	Byte Write Inputs	93,94,95,96			
$\overline{OE}$	Output Enable	86	V_{DDQ}	Output Power Supply (3.3V or 2.5V)	4,11,20,27,54,61,70,77
$\overline{GW}$	Global Write Enable	88			
$\overline{BW}$	Byte Write Enable	87	V_{SSQ}	Output Ground	5,10,21,26,55,60,71,76
$\overline{ZZ}$	Power Down Input	64			
$\overline{LBO}$	Burst Mode Control	31			

Note : 1. A0 and A1 are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

PIN CONFIGURATION (TOP VIEW)



PIN NAME

SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A_0 - A_{19}	Address Inputs	32,33,34,35,36,37,42 43,44,45,46,47,48,49 50 80,81,82,99,100	V_{DD}	Power Supply(+3.3V)	15,41,65,91
			V_{SS}	Ground	17,40,67,90
$\overline{ADV}$	Burst Address Advance	83	N.C.	No Connect	1,2,3,6,7,14,16,25,28,29 30,38,39,51,52,53,56,57 66,75,78,79,95,96
$\overline{ADSP}$	Address Status Processor	84			
$\overline{ADSC}$	Address Status Controller	85			
CLK	Clock	89			
$\overline{CS_1}$	Chip Select	98	DQa_0 ~ a_7	Data Inputs/Outputs	58,59,62,63,68,69,72,73
CS_2	Chip Select	97	DQb_0 ~ b_7		8,9,12,13,18,19,22,23
$\overline{CS_2}$	Chip Select	92	DQPa, Pb		74,24
$\overline{WE}$x(x=a,b)	Byte Write Inputs	93,94			
$\overline{OE}$	Output Enable	86	V_{DDQ}	Output Power Supply (3.3V or 2.5V)	4,11,20,27,54,61,70,77
$\overline{GW}$	Global Write Enable	88			
$\overline{BW}$	Byte Write Enable	87	V_{SSQ}	Output Ground	5,10,21,26,55,60,71,76
$\overline{ZZ}$	Power Down Input	64			
LBO	Burst Mode Control	31			

Note : 1. A_0 and A_1 are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

119BGA PACKAGE PIN CONFIGURATIONS(TOP VIEW)

K7A163609A(512Kx36)

	1	2	3	4	5	6	7
A	V_{DDQ}	A	A	$\overline{ADSP}$	A	A	V_{DDQ}
B	NC	A	A	$\overline{ADSC}$	A	A	NC
C	NC	A	A	V_{DD}	A	A	NC
D	DQc	DQPc	V_{SS}	NC	V_{SS}	DQPb	DQb
E	DQc	DQc	V_{SS}	$\overline{CS_1}$	V_{SS}	DQb	DQb
F	V_{DDQ}	DQc	V_{SS}	$\overline{OE}$	V_{SS}	DQb	V_{DDQ}
G	DQc	DQc	$\overline{WE}$c	$\overline{ADV}$	$\overline{WE}$b	DQb	DQb
H	DQc	DQc	V_{SS}	$\overline{GW}$	V_{SS}	DQb	DQb
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	DQd	DQd	V_{SS}	CLK	V_{SS}	DQa	DQa
L	DQd	DQd	$\overline{WE}$d	NC	$\overline{WE}$a	DQa	DQa
M	V_{DDQ}	DQd	V_{SS}	$\overline{BW}$	V_{SS}	DQa	V_{DDQ}
N	DQd	DQd	V_{SS}	A_1*	V_{SS}	DQa	DQa
P	DQd	DQPd	V_{SS}	A_0*	V_{SS}	DQPa	DQa
R	NC	A	$\overline{LBO}$	V_{DD}	NC	A	NC
T	NC	NC	A	A	A	NC	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

Note : * A_0 and A_1 are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

PIN NAME

SYMBOL	PIN NAME	SYMBOL	PIN NAME
A	Address Inputs	V_{DD}	Power Supply(+3.3V)
A_0, A_1	Burst Count Address	V_{SS}	Ground
$\overline{ADV}$	Burst Address Advance	N.C.	No Connect
$\overline{ADSP}$	Address Status Processor		
$\overline{ADSC}$	Address Status Controller	DQa	Data Inputs/Outputs
CLK	Clock	DQb	Data Inputs/Outputs
$\overline{CS_1}$	Chip Select	DQc	Data Inputs/Outputs
$\overline{WE}$x	Byte Write Inputs	DQd	Data Inputs/Outputs
(x=a,b,c,d)		DQPa~Pd	Data Inputs/Outpus
$\overline{OE}$	Output Enable	V_{DDQ}	Output Power Supply
$\overline{GW}$	Global Write Enable		(2.5V or 3.3V)
$\overline{BW}$	Byte Write Enable		
$\overline{ZZ}$	Power Down Input		
$\overline{LBO}$	Burst Mode Control		
TCK	JTAG Test Clock		
TMS	JTAG Test Mode Select		
TDI	JTAG Test Data Input		
TDO	JTAG Test Data Output		

119BGA PACKAGE PIN CONFIGURATIONS(TOP VIEW)

K7A161809A(1Mx18)

	1	2	3	4	5	6	7
A	V_{DDQ}	A	A	$\overline{ADSP}$	A	A	V_{DDQ}
B	NC	A	A	$\overline{ADSC}$	A	A	NC
C	NC	A	A	V_{DD}	A	A	NC
D	DQb	NC	V_{SS}	NC	V_{SS}	DQPa	NC
E	NC	DQb	V_{SS}	$\overline{CS_1}$	V_{SS}	NC	DQa
F	V_{DDQ}	NC	V_{SS}	$\overline{OE}$	V_{SS}	DQa	V_{DDQ}
G	NC	DQb	$\overline{WE}$b	$\overline{ADV}$	V_{SS}	NC	DQa
H	DQb	NC	V_{SS}	$\overline{GW}$	V_{SS}	DQa	NC
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	NC	DQb	V_{SS}	CLK	V_{SS}	NC	DQa
L	DQb	NC	V_{SS}	NC	$\overline{WE}$a	DQa	NC
M	V_{DDQ}	DQb	V_{SS}	$\overline{BW}$	V_{SS}	NC	V_{DDQ}
N	DQb	NC	V_{SS}	A_1*	V_{SS}	DQa	NC
P	NC	DQPb	V_{SS}	A_0*	V_{SS}	NC	DQa
R	NC	A	$\overline{LBO}$	V_{DD}	NC	A	NC
T	NC	A	A	NC	A	A	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

Note : * A_0 and A_1 are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

PIN NAME

SYMBOL	PIN NAME	SYMBOL	PIN NAME
A	Address Inputs	V_{DD}	Power Supply(+3.3V)
A_0,A_1	Burst Count Address	V_{SS}	Ground
$\overline{ADV}$	Burst Address Advance	N.C.	No Connect
$\overline{ADSP}$	Address Status Processor		
$\overline{ADSC}$	Address Status Controller	DQa	Data Inputs/Outputs
CLK	Clock	DQb	Data Inputs/Outputs
$\overline{CS_1}$	Chip Select	DQPa~Pb	Data Inputs/Outpus
$\overline{WE}$x	Byte Write Inputs		
(x=a,b)		V_{DDQ}	Output Power Supply
			(2.5V or 3.3V)
$\overline{OE}$	Output Enable		
$\overline{GW}$	Global Write Enable		
$\overline{BW}$	Byte Write Enable		
$\overline{ZZ}$	Power Down Input		
$\overline{LBO}$	Burst Mode Control		
TCK	JTAG Test Clock		
TMS	JTAG Test Mode Select		
TDI	JTAG Test Data Input		
TDO	JTAG Test Data Output		

FUNCTION DESCRIPTION

The K7A163609A and K7A161809A are synchronous SRAM designed to support the burst address accessing sequence of the Power PC based microprocessor. All inputs (with the exception of $\overline{OE}$, $\overline{LBO}$ and ZZ) are sampled on rising clock edges. The start and duration of the burst access is controlled by $\overline{ADSC}$, $\overline{ADSP}$ and $\overline{ADV}$ and chip select pins.

The accesses are enabled with the chip select signals and output enabled signals. Wait states are inserted into the access with $\overline{ADV}$.

When ZZ is pulled high, the SRAM will enter a Power Down State. At this time, internal state of the SRAM is preserved. When ZZ returns to low, the SRAM normally operates after 2cycles of wake up time. ZZ pin is pulled down internally.

Read cycles are initiated with $\overline{ADSP}$(regardless of $\overline{WE}$x and $\overline{ADSC}$)using the new external address clocked into the on-chip address register whenever $\overline{ADSP}$ is sampled low, the chip selects are sampled active, and the output buffer is enabled with $\overline{OE}$. In read operation the data of cell array accessed by the current address, registered in the Data-out registers by the positive edge of CLK, are carried to the Data-out buffer by the next positive edge of CLK. The data, registered in the Data-out buffer, are projected to the output pins. $\overline{ADV}$ is ignored on the clock edge that samples $\overline{ADSP}$ asserted, but is sampled on the subsequent clock edges. The address increases internally for the next access of the burst when $\overline{WE}$x are sampled High and $\overline{ADV}$ is sampled low. And $\overline{ADSP}$ is blocked to control signals by disabling $\overline{CS}_1$.

All byte write is done by $\overline{GW}$(regaedless of $\overline{BW}$ and $\overline{WE}$x.), and each byte write is performed by the combination of $\overline{BW}$ and $\overline{WE}$x when $\overline{GW}$ is high.

Write cycles are performed by disabling the output buffers with $\overline{OE}$ and asserting $\overline{WE}$x. $\overline{WE}$x are ignored on the clock edge that samples $\overline{ADSP}$ low, but are sampled on the subsequent clock edges. The output buffers are disabled when $\overline{WE}$x are sampled Low(regaedless of $\overline{OE}$). Data is clocked into the data input register when $\overline{WE}$x sampled Low. The address increases internally to the next address of burst, if both $\overline{WE}$x and $\overline{ADV}$ are sampled Low. Individual byte write cycles are performed by any one or more byte write enable signals($\overline{WE}$a, $\overline{WE}$b, $\overline{WE}$c or $\overline{WE}$d) sampled low. The $\overline{WE}$a control DQa_0 ~ DQa_7 and DQPa, $\overline{WE}$b controls DQb_0 ~ DQb_7 and DQPb, $\overline{WE}$c controls DQc_0 ~ DQc_7 and DQPc, and $\overline{WE}$d control DQd_0 ~ DQd_7 and DQPd. Read or write cycle may also be initiated with $\overline{ADSC}$, instead of $\overline{ADSP}$. The differences between cycles initiated with $\overline{ADSC}$ and $\overline{ADSP}$ as are follows;

$\overline{ADSP}$ must be sampled high when $\overline{ADSC}$ is sampled low to initiate a cycle with $\overline{ADSC}$.

$\overline{WE}$x are sampled on the same clock edge that sampled $\overline{ADSC}$ low(and $\overline{ADSP}$ high).

Addresses are generated for the burst access as shown below, The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion. The burst sequence is determined by the state of the $\overline{LBO}$ pin. When this pin is Low, linear burst sequence is selected. When this pin is High, Interleaved burst sequence is selected.

BURST SEQUENCE TABLE

(Interleaved Burst)

$\overline{LBO}$ PIN	HIGH	Case 1		Case 2		Case 3		Case 4	
		A_1	A_0	A_1	A_0	A_1	A_0	A_1	A_0
First Address		0	0	0	1	1	0	1	1
↓		0	1	0	0	1	1	1	0
		1	0	1	1	0	0	0	1
Fourth Address		1	1	1	0	0	1	0	0

(Linear Burst)

$\overline{LBO}$ PIN	LOW	Case 1		Case 2		Case 3		Case 4	
		A_1	A_0	A_1	A_0	A_1	A_0	A_1	A_0
First Address		0	0	0	1	1	0	1	1
↓		0	1	1	0	1	1	0	0
		1	0	1	1	0	0	0	1
Fourth Address		1	1	0	0	0	1	1	0

Note : 1. $\overline{LBO}$ pin must be tied to High or Low, and Floating State must not be allowed.

ASYNCHRONOUS TRUTH TABLE

Operation	ZZ	$\overline{OE}$	I/O STATUS
Sleep Mode	H	X	High-Z
Read	L	L	DQ
	L	H	High-Z
Write	L	X	Din, High-Z
Deselected	L	X	High-Z

Notes

1. X means "Don't Care".
2. ZZ pin is pulled down internally
3. For write cycles that following read cycles, the output buffers must be disabled with $\overline{OE}$, otherwise data bus contention will occur.
4. Sleep Mode means power down state of which stand-by current does not depend on cycle time.
5. Deselected means power down state of which stand-by current depends on cycle time.

TRUTH TABLES

SYNCHRONOUS TRUTH TABLE

$\overline{CS_1}$	CS_2	$\overline{CS_2}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	CLK	ADDRESS ACCESSED	OPERATION
H	X	X	X	L	X	X	↑	N/A	Not Selected
L	L	X	L	X	X	X	↑	N/A	Not Selected
L	X	H	L	X	X	X	↑	N/A	Not Selected
L	L	X	X	L	X	X	↑	N/A	Not Selected
L	X	H	X	L	X	X	↑	N/A	Not Selected
L	H	L	L	X	X	X	↑	External Address	Begin Burst Read Cycle
L	H	L	H	L	X	L	↑	External Address	Begin Burst Write Cycle
L	H	L	H	L	X	H	↑	External Address	Begin Burst Read Cycle
X	X	X	H	H	L	H	↑	Next Address	Continue Burst Read Cycle
H	X	X	X	H	L	H	↑	Next Address	Continue Burst Read Cycle
X	X	X	H	H	L	L	↑	Next Address	Continue Burst Write Cycle
H	X	X	X	H	L	L	↑	Next Address	Continue Burst Write Cycle
X	X	X	H	H	H	H	↑	Current Address	Suspend Burst Read Cycle
H	X	X	X	H	H	H	↑	Current Address	Suspend Burst Read Cycle
X	X	X	H	H	H	L	↑	Current Address	Suspend Burst Write Cycle
H	X	X	X	H	H	L	↑	Current Address	Suspend Burst Write Cycle

Notes : 1. X means "Don't Care". 2. The rising edge of clock is symbolized by ↑.

3. $\overline{WRITE}$ = L means Write operation in WRITE TRUTH TABLE.
   $\overline{WRITE}$ = H means Read operation in WRITE TRUTH TABLE.
4. Operation finally depends on status of asynchronous input pins(ZZ and $\overline{OE}$).

WRITE TRUTH TABLE(x36)

$\overline{GW}$	$\overline{BW}$	$\overline{WE}a$	$\overline{WE}b$	$\overline{WE}c$	$\overline{WE}d$	OPERATION
H	H	X	X	X	X	READ
H	L	H	H	H	H	READ
H	L	L	H	H	H	WRITE BYTE a
H	L	H	L	H	H	WRITE BYTE b
H	L	H	H	L	L	WRITE BYTE c and d
H	L	L	L	L	L	WRITE ALL BYTEs
L	X	X	X	X	X	WRITE ALL BYTEs

Notes : 1. X means "Don't Care".

2. All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).

WRITE TRUTH TABLE(x18)

$\overline{GW}$	$\overline{BW}$	$\overline{WE}a$	$\overline{WE}b$	OPERATION
H	H	X	X	READ
H	L	H	H	READ
H	L	L	H	WRITE BYTE a
H	L	H	L	WRITE BYTE b
H	L	L	L	WRITE ALL BYTEs
L	X	X	X	WRITE ALL BYTEs

Notes : 1. X means "Don't Care".

2. All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).

PASS-THROUGH TRUTH TABLE

PREVIOUS CYCLE		PRESENT CYCLE				NEXT CYCLE
OPERATION	$\overline{WRITE}$	OPERATION	$\overline{CS_1}$	$\overline{WRITE}$	$\overline{OE}$	
Write Cycle, All bytes Address=An-1, Data=Dn-1	All L	Initiate Read Cycle Address=An Data=Qn-1 for all bytes	L	H	L	Read Cycle Data=Qn
Write Cycle, All bytes Address=An-1, Data=Dn-1	All L	No new cycle Data=Qn-1 for all bytes	H	H	L	No carryover from previous cycle
Write Cycle, All bytes Address=An-1, Data=Dn-1	All L	No new cycle Data=High-Z	H	H	H	No carryover from previous cycle
Write Cycle, One byte Address=An-1, Data=Dn-1	One L	Initiate Read Cycle Address=An Data=Qn-1 for one byte	L	H	L	Read Cycle Data=Qn
Write Cycle, One byte Address=An-1, Data=Dn-1	One L	No new cycle Data=Qn-1 for one byte	H	H	L	No carryover from previous cycle

Note : 1. This operation makes written data immediately available at output during a read cycle preceded by a write cycle.

ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Voltage on V_{DD} Supply Relative to V_{SS}	V_{DD}	-0.3 to 4.6	V
Voltage on V_{DDQ} Supply Relative to V_{SS}	V_{DDQ}	V_{DD}	V
Voltage on Input Pin Relative to V_{SS}	V_{IN}	-0.3 to V_{DD}+0.3	V
Voltage on I/O Pin Relative to V_{SS}	V_{IO}	-0.3 to V_{DDQ}+0.3	V
Power Dissipation	P_D	1.6	W
Storage Temperature	T_{STG}	-65 to 150	°C
Operating Temperature	T_{OPR}	0 to 70	°C
Storage Temperature Range Under Bias	T_{BIAS}	-10 to 85	°C

***Note :** Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING CONDITIONS at 3.3V I/O(0°C ≤ T_A ≤ 70°C)

PARAMETER	SYMBOL	MIN	Typ.	MAX	UNIT
Supply Voltage	V_{DD}	3.135	3.3	3.465	V
	V_{DDQ}	3.135	3.3	3.465	V
Ground	V_{SS}	0	0	0	V

OPERATING CONDITIONS at 2.5V I/O(0°C ≤ T_A ≤ 70°C)

PARAMETER	SYMBOL	MIN	Typ.	MAX	UNIT
Supply Voltage	V_{DD}	3.135	3.3	3.465	V
	V_{DDQ}	2.375	2.5	2.9	V
Ground	V_{SS}	0	0	0	V

CAPACITANCE*(T_A=25°C, f=1MHz)

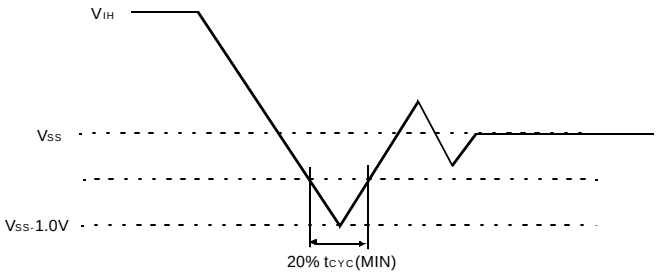
PARAMETER	SYMBOL	TEST CONDITION	MIN	MAX	UNIT
Input Capacitance	C_{IN}	V_{IN}=0V	-	5	pF
Output Capacitance	C_{OUT}	V_{OUT}=0V	-	7	pF

***Note :** Sampled not 100% tested.

DC ELECTRICAL CHARACTERISTICS(V_{DD}=3.3V+0.165V/-0.165V, T_A=0°C to +70°C)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	MAX	UNIT	NOTES
Input Leakage Current(except ZZ)	I_{IL}	V_{DD} = Max ; V_{IN}=V_{SS} to V_{DD}		-2	+2	µA	
Output Leakage Current	I_{OL}	Output Disabled, V_{OUT}=V_{SS} to V_{DDQ}		-2	+2	µA	
Operating Current	I_{CC}	Device Selected, I_{OUT}=0mA, ZZ≤V_{IL}, Cycle Time ≥ t_{CYC} Min	-25	-	TBD	mA	1,2
			-22	-	TBD		
			-20	-	TBD		
Standby Current	I_{SB}	Device deselected, I_{OUT}=0mA, ZZ≤V_{IL}, f=Max, All Inputs≤0.2V or ≥ V_{DD}-0.2V	-25	-	TBD	mA	
			-22	-	TBD		
			-20	-	TBD		
	I_{SB1}	Device deselected, I_{OUT}=0mA, ZZ≤0.2V, f = 0, All Inputs=fixed (V_{DD}-0.2V or 0.2V)		-	TBD	mA	
	I_{SB2}	Device deselected, I_{OUT}=0mA, ZZ≥V_{DD}-0.2V, f=Max, All Inputs≤V_{IL} or ≥V_{IH}		-	TBD	mA	
Output Low Voltage(3.3V I/O)	V_{OL}	I_{OL}=8.0mA		-	0.4	V	
Output High Voltage(3.3V I/O)	V_{OH}	I_{OH}=-4.0mA		2.4	-	V	
Output Low Voltage(2.5V I/O)	V_{OL}	I_{OL}=1.0mA		-	0.4	V	
Output High Voltage(2.5V I/O)	V_{OH}	I_{OH}=-1.0mA		2.0	-	V	
Input Low Voltage(3.3V I/O)	V_{IL}			-0.3*	0.8	V	
Input High Voltage(3.3V I/O)	V_{IH}			2.0	V_{DD}+0.3**	V	3
Input Low Voltage(2.5V I/O)	V_{IL}			-0.3*	0.7	V	
Input High Voltage(2.5V I/O)	V_{IH}			1.7	V_{DD}+0.3**	V	3

Notes : 1. Reference AC Operating Conditions and Characteristics for input and timing.
2. Data states are all zero.
3. In Case of I/O Pins, the Max. V_{IH}=V_{DDQ}+0.3V.

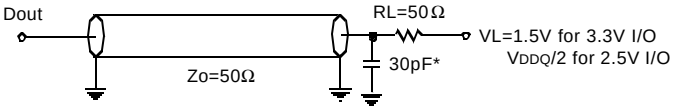


TEST CONDITIONS

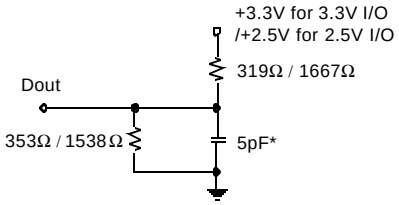
(V_{DD}=3.3V+0.165V/-0.165V,V_{DDQ}=3.3V+0.165/-0.165V or V_{DD}=3.3V+0.165V/-0.165V,V_{DDQ}=2.5V+0.4V/-0.125V, T_A=0to70°C)

PARAMETER	VALUE
Input Pulse Level(for 3.3V I/O)	0 to 3.0V
Input Pulse Level(for 2.5V I/O)	0 to 2.5V
Input Rise and Fall Time(Measured at 20% to 80% for 3.3V I/O)	1.0V/ns
Input Rise and Fall Time(Measured at 20% to 80% for 2.5V I/O)	1.0V/ns
Input and Output Timing Reference Levels for 3.3V I/O	1.5V
Input and Output Timing Reference Levels for 2.5V I/O	V_{DDQ}/2
Output Load	See Fig. 1

Output Load(A)



Output Load(B),
(for tLZC, tLZOE, tHZOE & tHZC)



* Including Scope and Jig Capacitance

Fig. 1

AC TIMING CHARACTERISTICS(VDD=3.3V+0.165V/-0.165V, TA=0°C to +70°C)

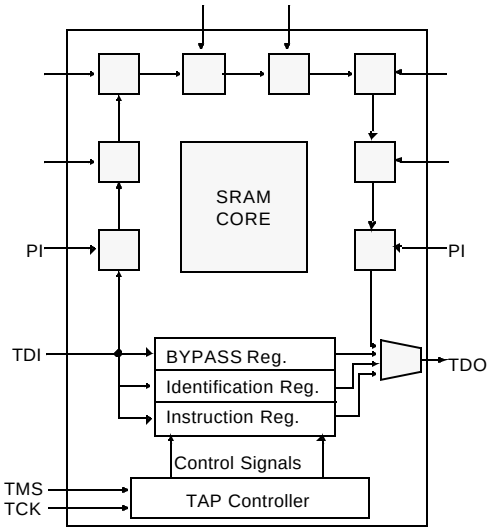
PARAMETER	Symbol	-25		-22		-20		UNIT
		MIN	MAX	Min	Max	MIN	MAX	
Cycle Time	tCYC	4.0	-	4.4	-	5.0	-	ns
Clock Access Time	tCD	-	2.6	-	2.8	-	3.1	ns
Output Enable to Data Valid	tOE	-	2.6	-	2.8	-	3.1	ns
Clock High to Output Low-Z	tLZC	0	-	0	-	0	-	ns
Output Hold from Clock High	tOH	0.8	-	1.0	-	1.0	-	ns
Output Enable Low to Output Low-Z	tLZOE	0	-	0	-	0	-	ns
Output Enable High to Output High-Z	tHZOE	-	2.6	-	2.8	-	3.0	ns
Clock High to Output High-Z	tHZC	0.8	2.6	1.0	2.8	1.0	3.0	ns
Clock High Pulse Width	tCH	1.7	-	1.8	-	2.0	-	ns
Clock Low Pulse Width	tCL	1.7	-	1.8	-	2.0	-	ns
Address Setup to Clock High	tAS	1.2	-	1.4	-	1.4	-	ns
Address Status Setup to Clock High	tSS	1.2	-	1.4	-	1.4	-	ns
Data Setup to Clock High	tDS	1.2	-	1.4	-	1.4	-	ns
Write Setup to Clock High ($\overline{GW}$, $\overline{BW}$, $\overline{WE}$x)	tWS	1.2	-	1.4	-	1.4	-	ns
Address Advance Setup to Clock High	tADVS	1.2	-	1.4	-	1.4	-	ns
Chip Select Setup to Clock High	tCSS	1.2	-	1.4	-	1.4	-	ns
Address Hold from Clock High	tAH	0.3	-	0.4	-	0.4	-	ns
Address Status Hold from Clock High	tSH	0.3	-	0.4	-	0.4	-	ns
Data Hold from Clock High	tDH	0.3	-	0.4	-	0.4	-	ns
Write Hold from Clock High ($\overline{GW}$, $\overline{BW}$, $\overline{WE}$x)	tWH	0.3	-	0.4	-	0.4	-	ns
Address Advance Hold from Clock High	tADVH	0.3	-	0.4	-	0.4	-	ns
Chip Select Hold from Clock High	tCSH	0.3	-	0.4	-	0.4	-	ns
ZZ High to Power Down	tPDS	2	-	2	-	2	-	cycle
ZZ Low to Power Up	tPUS	2	-	2	-	2	-	cycle

Notes : 1. All address inputs must meet the specified setup and hold times for all rising clock edges whenever $\overline{ADSC}$ and/or $\overline{ADSP}$ is sampled low and CS is sampled low. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.
2. Both chip selects must be active whenever ADSC or ADSP is sampled low in order for the this device to remain enabled.
3. ADSC or ADSP must not be asserted for at least 2 Clock after leaving ZZ state.

IEEE 1149.1 TEST ACCESS PORT AND BOUNDARY SCAN-JTAG

This part contains an IEEE standard 1149.1 Compatible Teat Access Port(TAP). The package pads are monitored by the Serial Scan circuitry when in test mode. This is to support connectivity testing during manufacturing and system diagnostics. Internal data is not driven out of the SRAM under JTAG control. In conformance with IEEE 1149.1, the SRAM contains a TAP controller, Instruction Register, Bypass Register and ID register. The TAP controller has a standard 16-state machine that resets internally upon power-up, therefore, TRST signal is not required. It is possible to use this device without utilizing the TAP. To disable the TAP controller without interfacing with normal operation of the SRAM, TCK must be tied to V_{SS} to preclude mid level input. TMS and TDI are designed so an undriven input will produce a response identical to the application of a logic 1, and may be left unconnected. But they may also be tied to V_{DD} through a resistor. TDO should be left unconnected.

JTAG Block Diagram



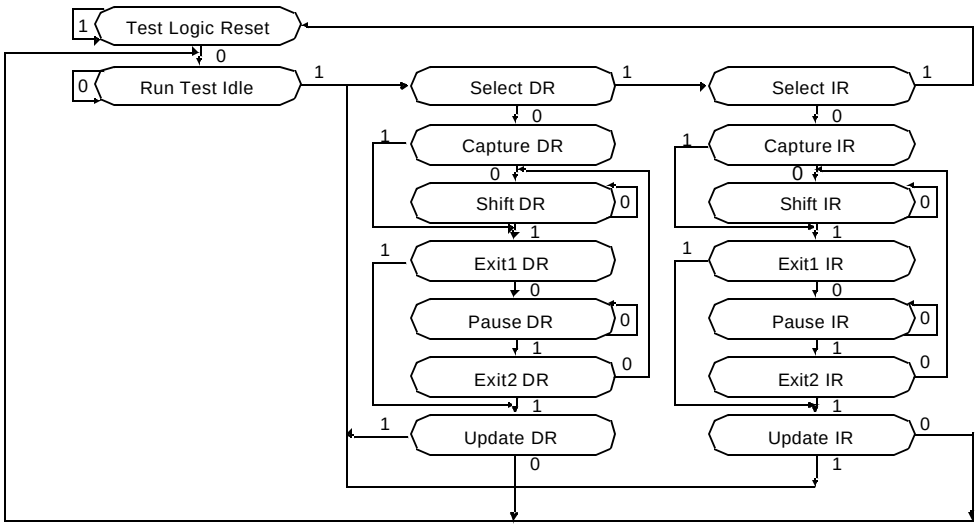
JTAG Instruction Coding

IR2	IR1	IR0	Instruction	TDO Output	Notes
0	0	0	SAMPLE-Z	Boundary Scan Register	1
0	0	1	IDCODE	Identification Register	2
0	1	0	SAMPLE-Z	Boundary Scan Register	1
0	1	1	BYPASS	Bypass Register	3
1	0	0	SAMPLE	Boundary Scan Register	4
1	0	1	BYPASS	Bypass Register	3
1	1	0	BYPASS	Bypass Register	3
1	1	1	BYPASS	Bypass Register	3

NOTE :

1. Places DQs in Hi-Z in order to sample all input data regardless of other SRAM inputs.
2. TDI is sampled as an input to the first ID register to allow for the serial shift of the external TDI data.
3. Bypass register is initiated to V_{SS} when BYPASS instruction is invoked. The Bypass Register also holds serially loaded TDI when exiting the Shift DR states.
4. SAMPLE instruction dose not places DQs in Hi-Z.

TAP Controller State Diagram



SCAN REGISTER DEFINITION

Part	Instruction Register	Bypass Register	ID Register	Boundary Scan
512Kx36	3 bits	1 bits	32 bits	75 bits
1Mx18	3 bits	1 bits	32 bits	75 bits

ID REGISTER DEFINITION

Part	Revision Number (31:28)	Part Configuration (27:18)	Vendor Definition (17:12)	Samsung JEDEC Code (11: 1)	Start Bit(0)
512Kx36	0000	00111 00100	XXXXXX	00001001110	1
1Mx18	0000	01000 00011	XXXXXX	00001001110	1

119BGA BOUNDARY SCAN EXIT ORDER(x36)

1	2T	NC		CLK	4K	39
2	1R	NC		$\overline{ADV}$	4G	40
3	4T	A		$\overline{ADSC}$	4B	41
4	4H	$\overline{GW}$		$\overline{ADSP}$	4A	42
5	5R	NC		$\overline{BW}$	4M	43
6	5T	A		$\overline{WE}$c	3G	44
7	5L	$\overline{WE}$a		A	3B	45
8	7R	NC		A	3A	46
9	6R	A		A	2B	47
10	7T	ZZ		$\overline{CS}$1	4E	48
11	6P	DQPa		A	3C	49
12	7N	DQa		A	2C	50
13	6M	DQa		A	2A	51
14	7L	DQa		DQPc	2D	52
15	6K	DQa		DQc	1E	53
16	7P	DQa		DQc	2F	54
17	6N	DQa		DQc	1G	55
18	6L	DQa		DQc	2H	56
19	7K	DQa		DQc	1D	57
20	5J	NC		DQc	2E	58
21	6H	DQb		DQc	2G	59
22	7G	DQb		DQc	1H	60
23	6F	DQb		DQd	2K	61
24	7E	DQb		DQd	1L	62
25	7D	DQb		DQd	2M	63
26	7H	DQb		DQd	1N	64
27	6G	DQb		DQd	1P	65
28	6E	DQb		DQd	1K	66
29	6D	DQPb		DQd	2L	67
30	7B	NC		DQd	2N	68
31	6C	A		DQPd	2P	69
32	5C	A		$\overline{WE}$d	3L	70
33	6A	A		$\overline{LBO}$	3R	71
34	5B	A		A	2R	72
35	5A	A		A	3T	73
36	4F	$\overline{OE}$		A1	4N	74
37	5G	$\overline{WE}$b		A0	4P	75
38	6B	A				

119BGA BOUNDARY SCAN EXIT ORDER(x18)

1	2T	A		CLK	4K	39
2	1R	NC		$\overline{ADV}$	4G	40
3	6T	A		$\overline{ADSC}$	4B	41
4	4H	$\overline{GW}$		$\overline{ADSP}$	4A	42
5	5R	NC		$\overline{BW}$	4M	43
6	5T	A		$\overline{WE}$b	3G	44
7	5L	$\overline{WE}$a		A	3B	45
8	7R	NC		A	3A	46
9	6R	A		A	2B	47
10	7T	ZZ		$\overline{CS}$1	4E	48
11	6P	NC		A	3C	49
12	7N	NC		A	2C	50
13	6M	NC		A	2A	51
14	7L	NC		NC	2D	52
15	6K	NC		NC	1E	53
16	7P	DQa		NC	2F	54
17	6N	DQa		NC	1G	55
18	6L	DQa		NC	2H	56
19	7K	DQa		DQb	1D	57
20	5J	NC		DQb	2E	58
21	6H	DQa		DQb	2G	59
22	7G	DQa		DQb	1H	60
23	6F	DQa		DQb	2K	61
24	7E	DQa		DQb	1L	62
25	6D	DQPa		DQb	2M	63
26	7H	NC		DQb	1N	64
27	6G	NC		DQPb	2P	65
28	6E	NC		NC	1K	66
29	7D	NC		NC	2L	67
30	7B	NC		NC	2N	68
31	6C	A		NC	1P	69
32	5C	A		NC	3L	70
33	6A	A		$\overline{LBO}$	3R	71
34	5B	A		A	2R	72
35	5A	A		A	3T	73
36	4F	$\overline{OE}$		A1	4N	74
37	5G	NC		A0	4P	75
38	6B	A				

NOTE, NC ; Don't Care

JTAG DC OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Note
Power Supply Voltage	V_{DD}	3.135	3.3	3.465	V	
Input High Level (3.3V I/O / 2.5V I/O)	V_{IH}	2.0 / 1.7	-	V_{DD}+0.3	V	
Input Low Level (3.3V I/O / 2.5V I/O)	V_{IL}	-0.3	-	0.8 / 0.7	V	
Output High Voltage(3.3V I/O / 2.5V I/O)	V_{OH}	2.4 / 2.0	-	-	V	
Output Low Voltage(3.3V I/O / 2.5V I/O)	V_{OL}	-	-	0.4 / 0.4	V	

NOTE : The input level of SRAM pin is to follow the SRAM DC specification.

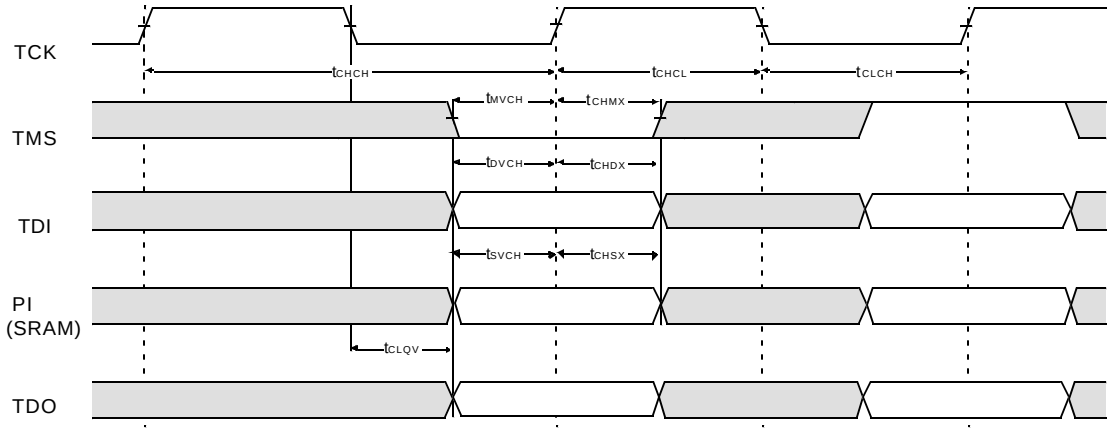
JTAG AC TEST CONDITIONS

Parameter	Symbol	Min	Unit	Note
Input High/Low Level(3.3V I/O , 2.5V I/O)	V_{IH}/V_{IL}	3.0/0 , 2.5/0	V	
Input Rise/Fall Time(3.3V I/O , 2.5V I/O)	TR/TF	1.0/1.0 , 1.0/1.0	ns	
Input and Output Timing Reference Level		$V_{DDQ}/2$	V	

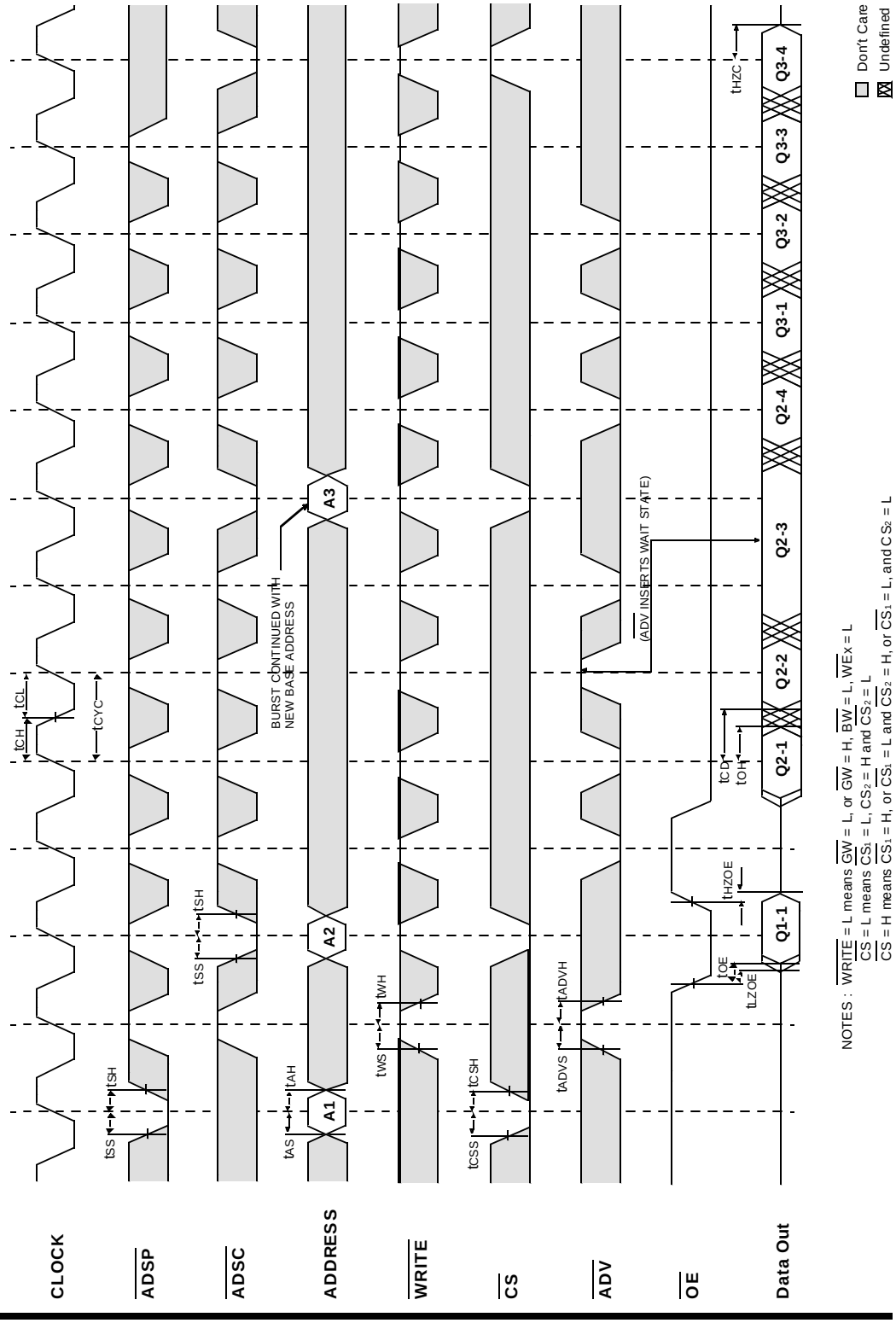
JTAG AC Characteristics

Parameter	Symbol	Min	Max	Unit	Note
TCK Cycle Time	t_{CHCH}	50	-	ns	
TCK High Pulse Width	t_{CHCL}	20	-	ns	
TCK Low Pulse Width	t_{CLCH}	20	-	ns	
TMS Input Setup Time	t_{MVCH}	5	-	ns	
TMS Input Hold Time	t_{CHMX}	5	-	ns	
TDI Input Setup Time	t_{DVCH}	5	-	ns	
TDI Input Hold Time	t_{CHDX}	5	-	ns	
SRAM Input Setup Time	t_{SVCH}	5	-	ns	
SRAM Input Hold Time	t_{CHSX}	5	-	ns	
Clock Low to Output Valid	t_{CLQV}	0	10	ns	

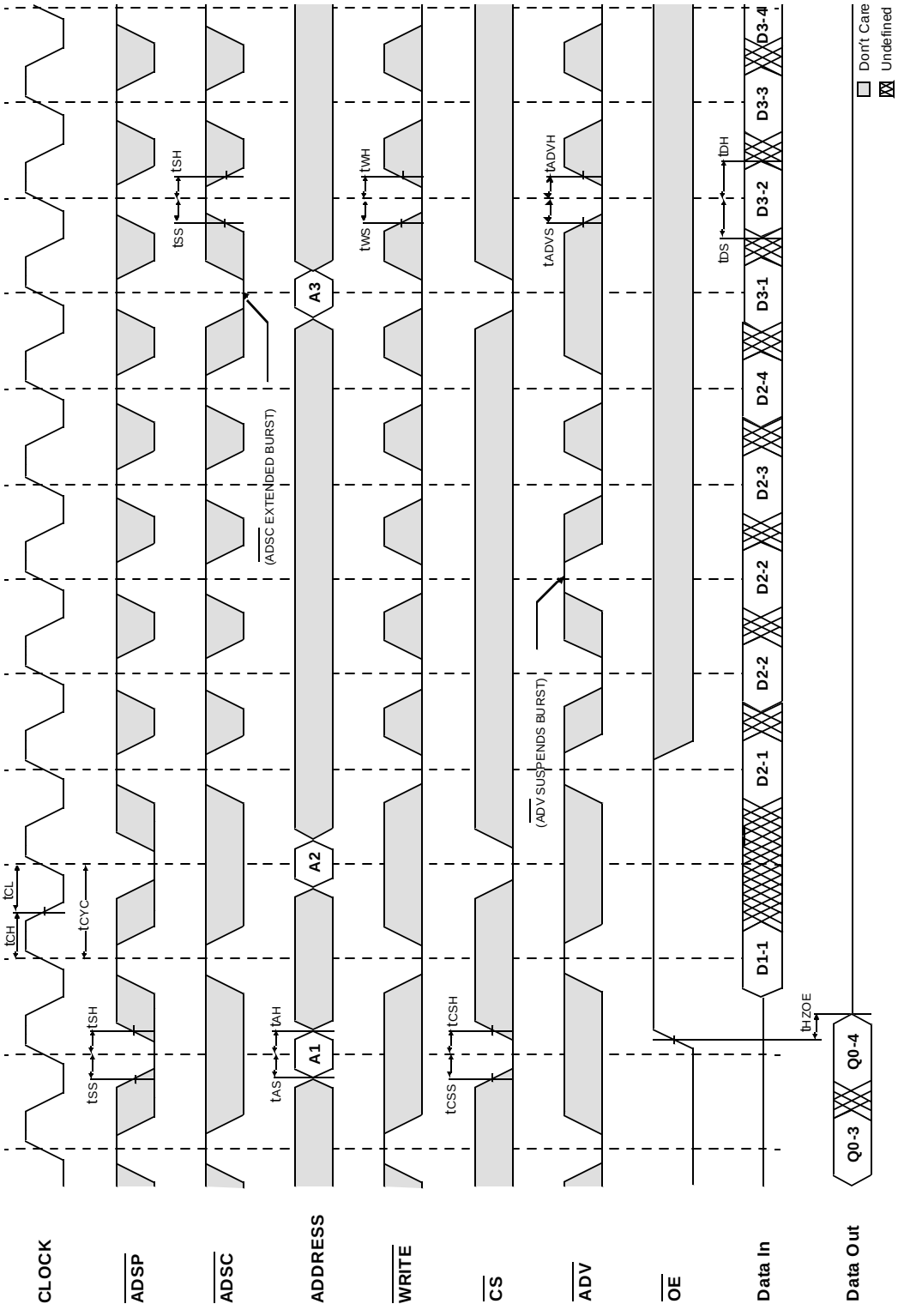
JTAG TIMING DIAGRAM



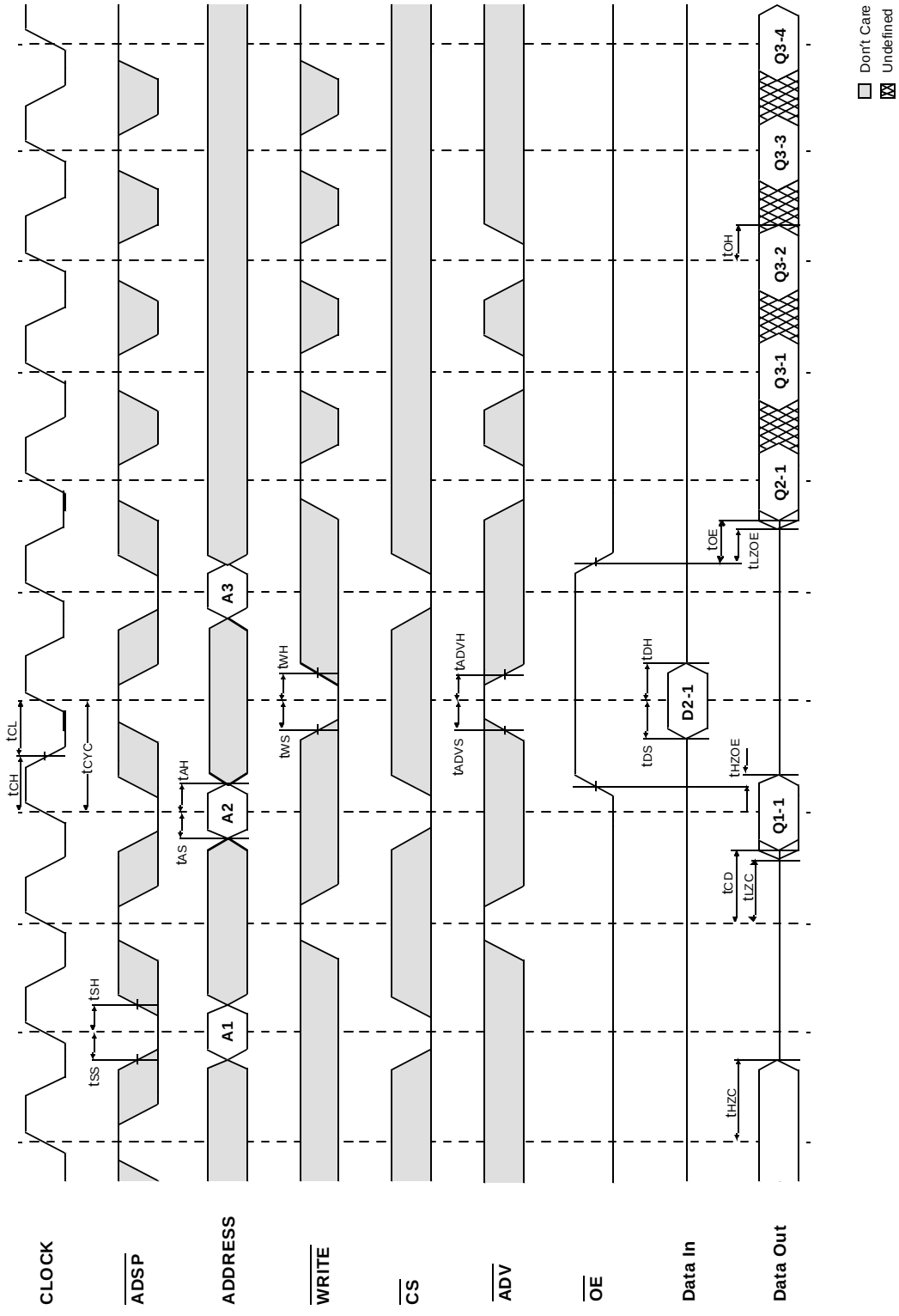
TIMING WAVEFORM OF READ CYCLE



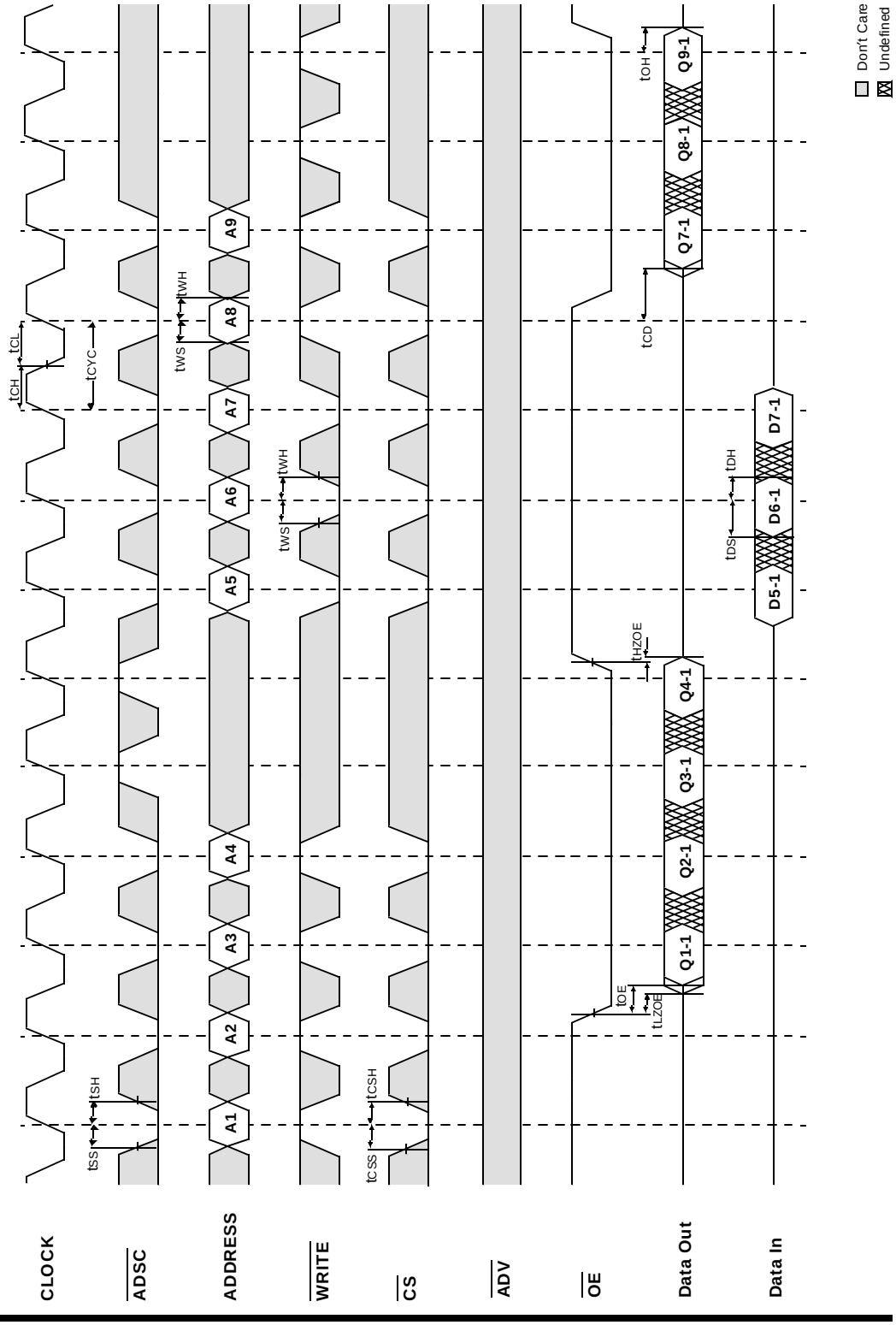
TIMING WAVEFORM OF WRTE CYCLE



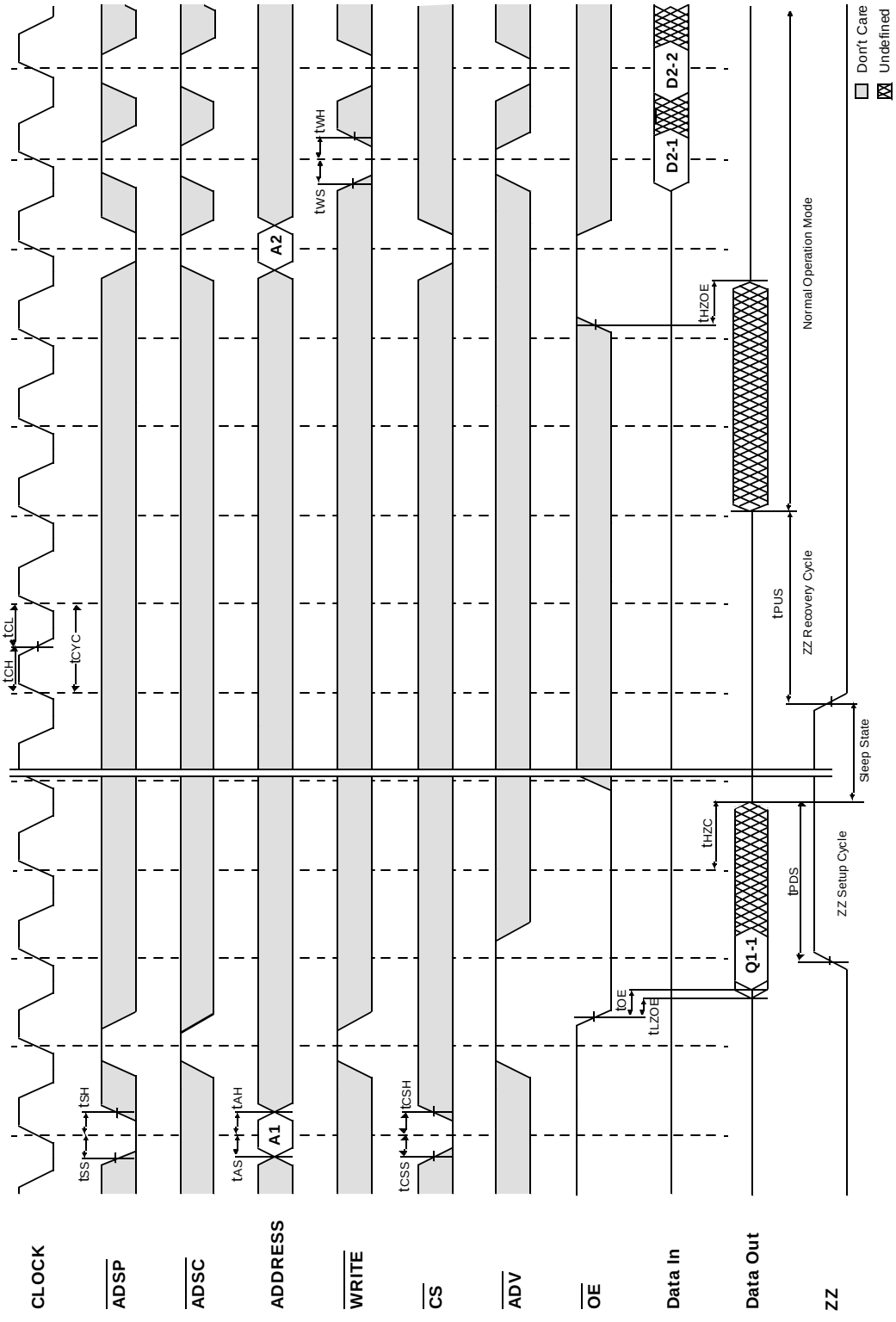
TIMING WAVEFORM OF COMBINATION READ/WRTE CYCLE(ADSP CONTROLLED , ADSC=HIGH)



TIMING WAVEFORM OF SINGLE READ/WRITE CYCLE(ADSC CONTROLLED , ADSP=HIGH)



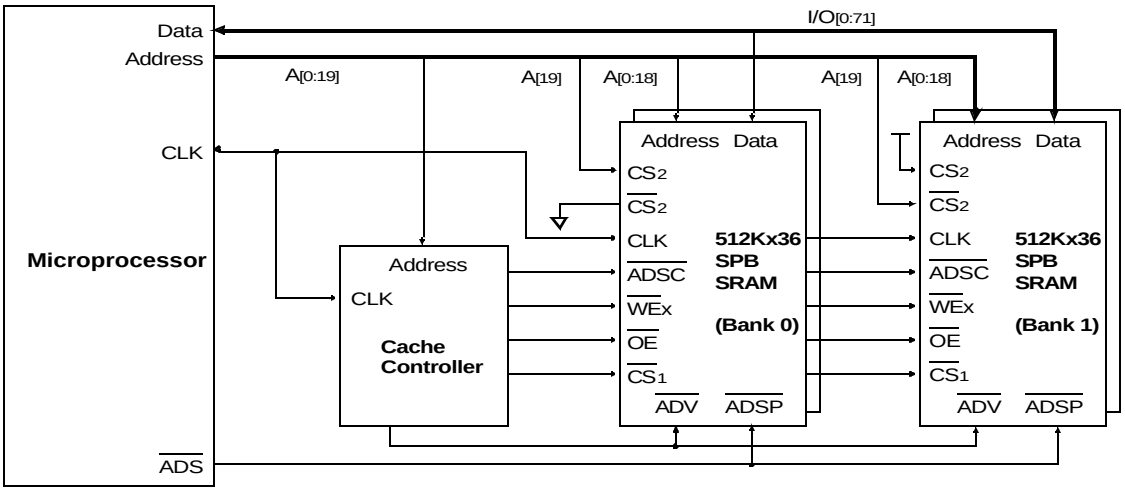
TIMING WAVEFORM OF POWER DOWN CYCLE



APPLICATION INFORMATION

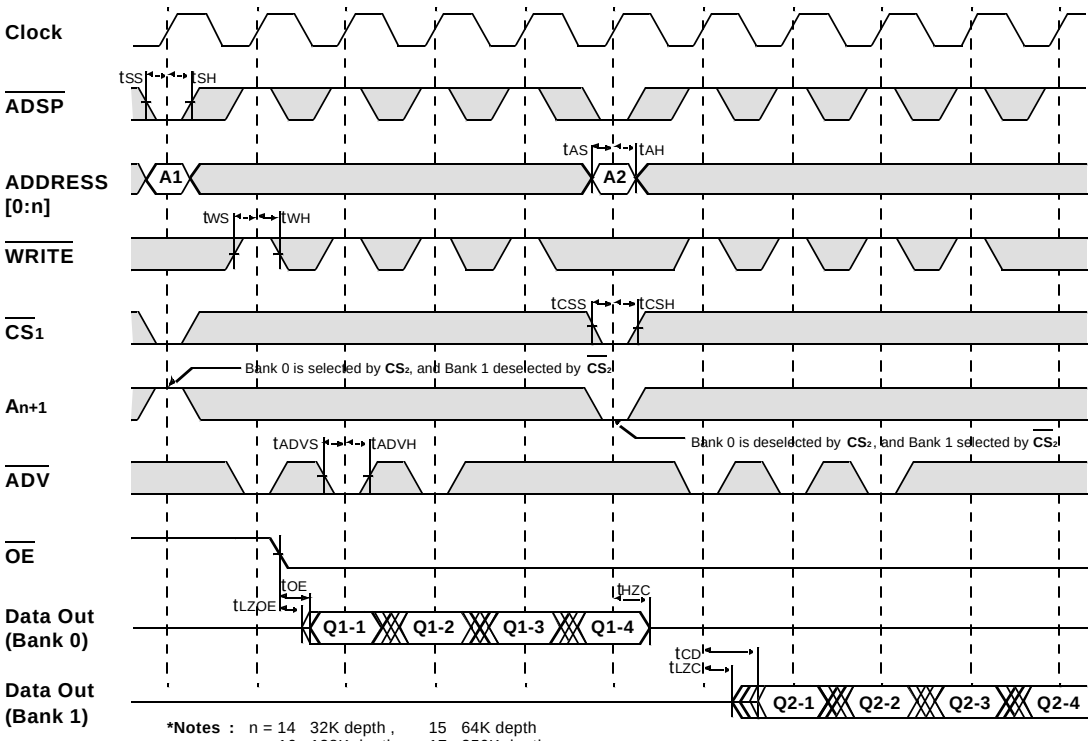
DEPTH EXPANSION

The Samsung 512Kx36 Synchronous Pipelined Burst SRAM has two additional chip selects for simple depth expansion. This permits easy secondary cache upgrades from 512K depth to 1M depth without extra logic.



INTERLEAVE READ TIMING (Refer to non-interleave write timing for interleave write timing)

($\overline{ADSP}$ CONTROLLED , $\overline{ADSC}$=HIGH)



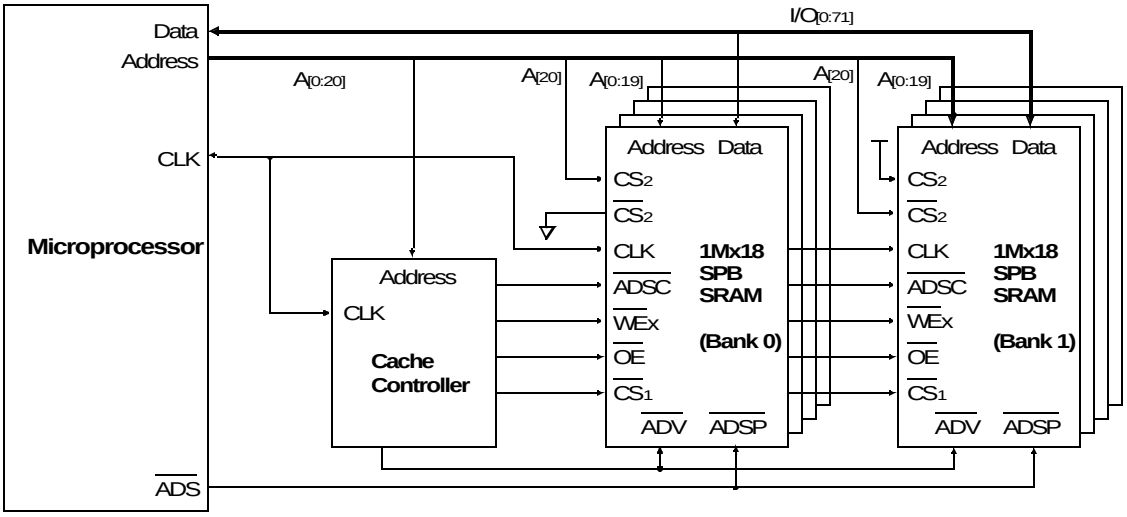
***Notes :** n = 14 32K depth , 15 64K depth
16 128K depth , 17 256K depth
18 512K depth , 19 1M depth

Don't Care Undefined

APPLICATION INFORMATION

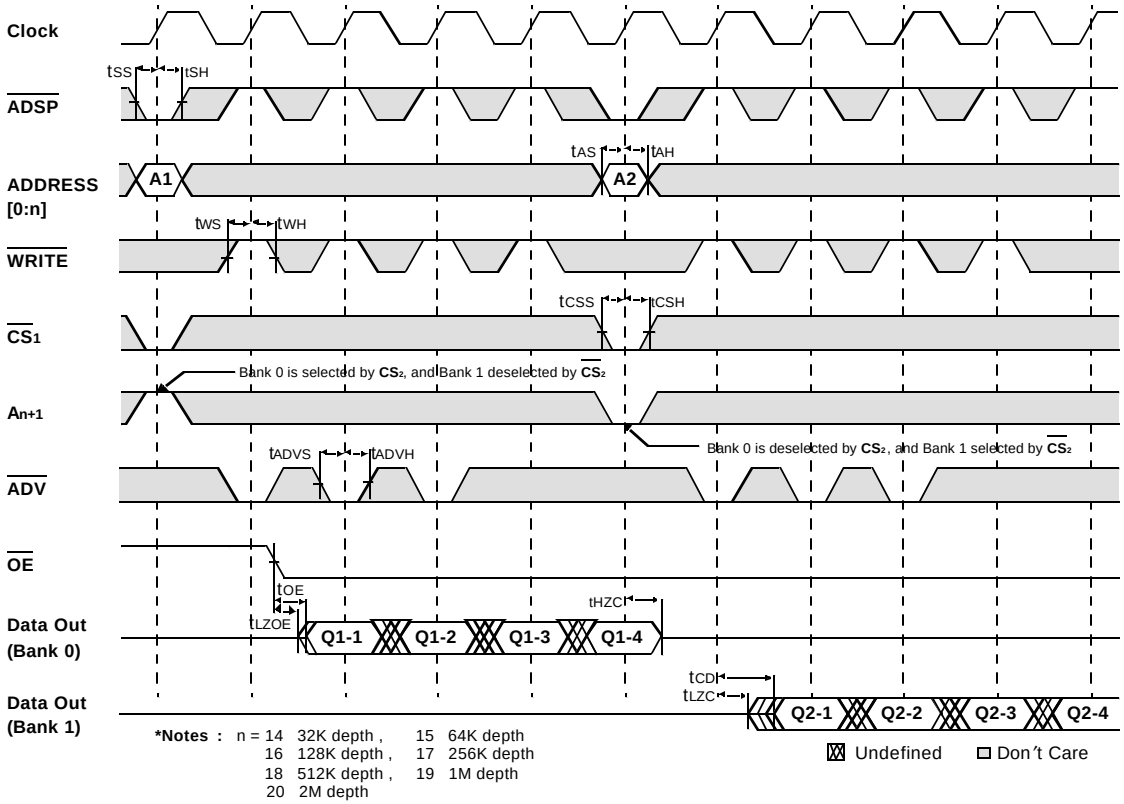
DEPTH EXPANSION

The Samsung 1Mx18 Synchronous Pipelined Burst SRAM has two additional chip selects for simple depth expansion. This permits easy secondary cache upgrades from 1M depth to 2M depth without extra logic.



INTERLEAVE READ TIMING (Refer to non-interleave write timing for interleave write timing)

(ADSP CONTROLLED , ADSC=HIGH)

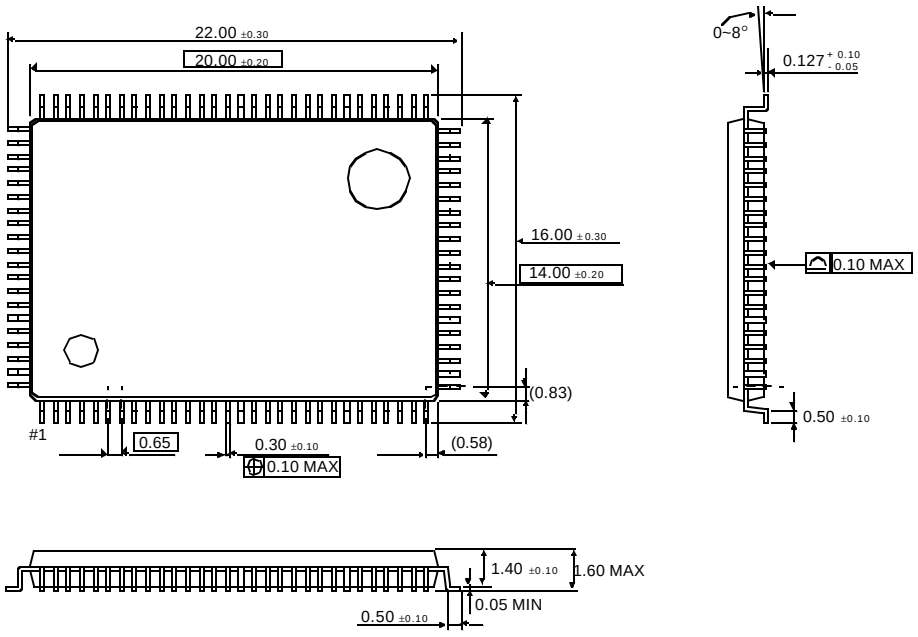


*Notes : n = 14 32K depth , 15 64K depth
16 128K depth , 17 256K depth
18 512K depth , 19 1M depth
20 2M depth

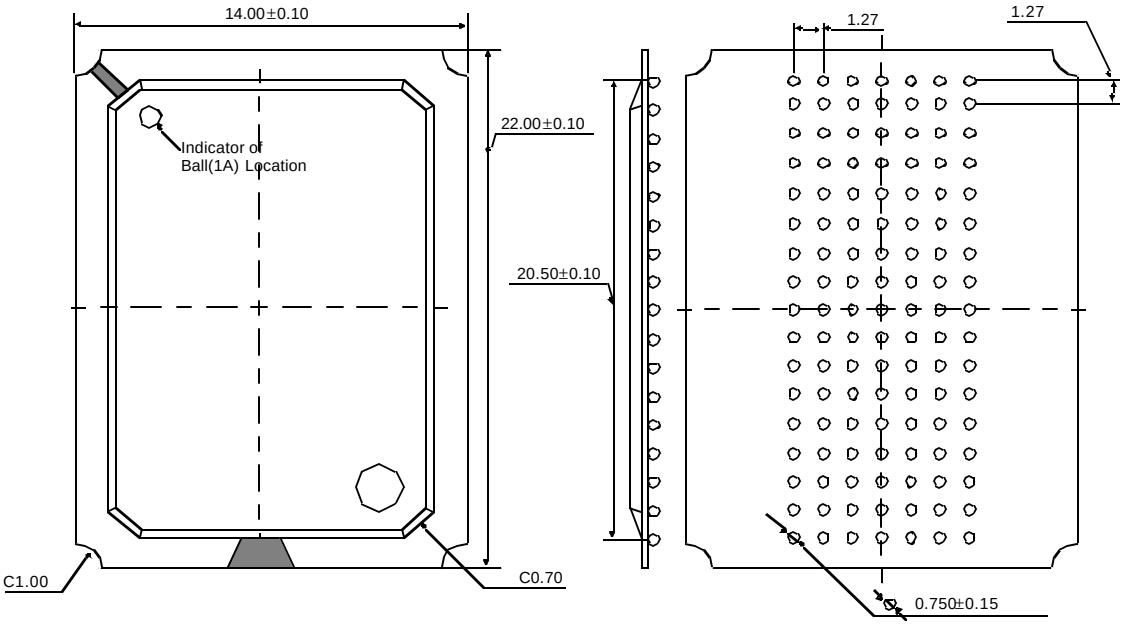
PACKAGE DIMENSIONS

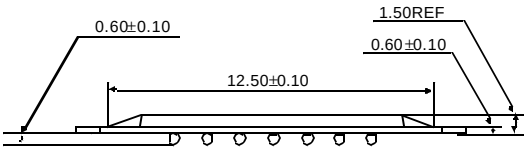
100-TQFP-1420A

Units ; millimeters/Inches



119 BGA PACKAGE DIMENSIONS





NOTE :

1. All Dimensions are in Millimeters.
2. Solder Ball to PCB Offset : 0.10 MAX.
3. PCB to Cavity Offset : 0.10 MAX.