512Kx36 & 1Mx18-Bit Synchronous Pipelined Burst SRAM

FEATURES

- Synchronous Operation.
- 2 Stage Pipelined operation with 4 Burst.
- On-Chip Address Counter.
- Self-Timed Write Cycle.
- On-Chip Address and Control Registers.
- V_{DD} = 3.3V +0.165V/-0.165V Power Supply.
- I/O Supply Voltage 3.3V +0.165V/-0.165V for 3.3V I/O or 2.5V+0.4V/-0.125V for 2.5V I/O.
- 5V Tolerant Inputs Except I/O Pins.
- Byte Writable Function.
- Global Write Enable Controls a full bus-width write.
- Power Down State via ZZ Signal.
- $\overline{LBO}$ Pin allows a choice of either a interleaved burst or a linear burst.
- Three Chip Enables for simple depth expansion with No Data Contention only for TQFP ; 2cycle Enable, 1cycle Disable.
- Asynchronous Output Enable Control.
- $\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$ Burst Control Pins.
- TTL-Level Three-State Output.
- 100-TQFP-1420A / 119BGA(7x17 Ball Grid Array Package)

FAST ACCESS TIMES

PARAMETER	Symbol	-25	-22	-20	Unit
Cycle Time	tCYC	4.0	4.4	5.0	ns
Clock Access Time	tCD	2.6	2.8	3.1	ns
Output Enable Access Time	tOE	2.6	2.8	3.1	ns

GENERAL DESCRIPTION

The K7A163609A and K7A161809A are 18,874,368-bit Synchronous Static Random Access Memory designed for high performance second level cache of Pentium and Power PC based System.

It is organized as 512K(1M) words of 36(18) bits and integrates address and control registers, a 2-bit burst address counter and added some new functions for high performance cache RAM applications; $\overline{GW}$, $\overline{BW}$, $\overline{LBO}$, ZZ. Write cycles are internally self-timed and synchronous.

Full bus-width write is done by $\overline{GW}$, and each byte write is performed by the combination of $\overline{WE}$x and $\overline{BW}$ when $\overline{GW}$ is high. And with $\overline{CS}_1$ high, $\overline{ADSP}$ is blocked to control signals.

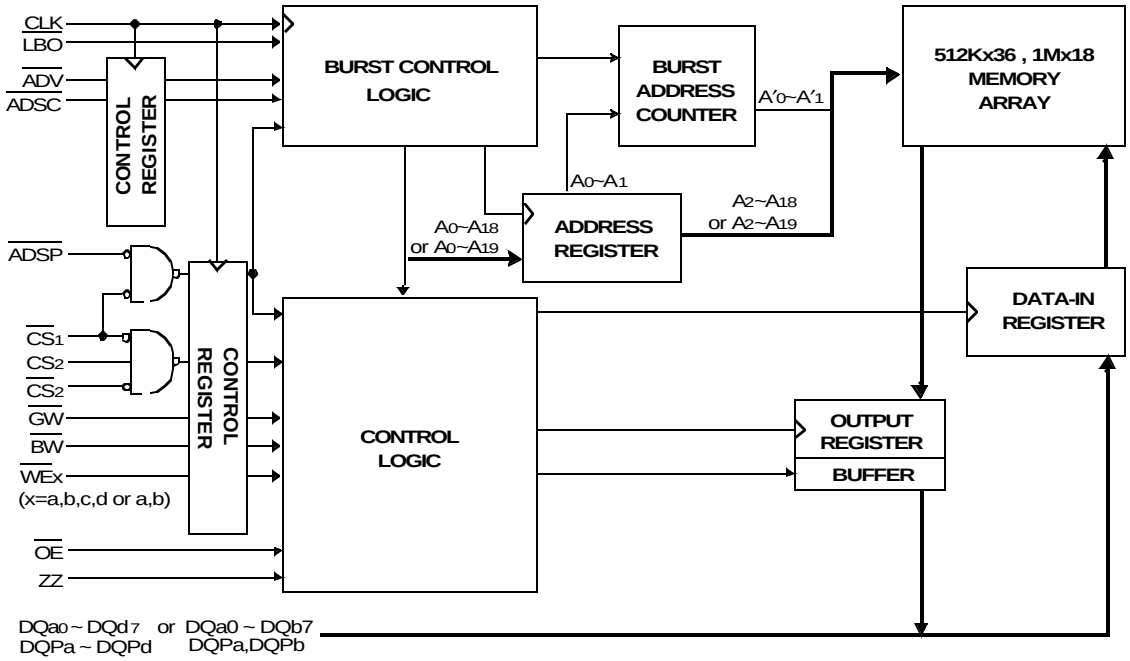
Burst cycle can be initiated with either the address status processor($\overline{ADSP}$) or address status cache controller($\overline{ADSC}$) inputs. Subsequent burst addresses are generated internally in the system's burst sequence and are controlled by the burst address advance($\overline{ADV}$) input.

$\overline{LBO}$ pin is DC operated and determines burst sequence(linear or interleaved).

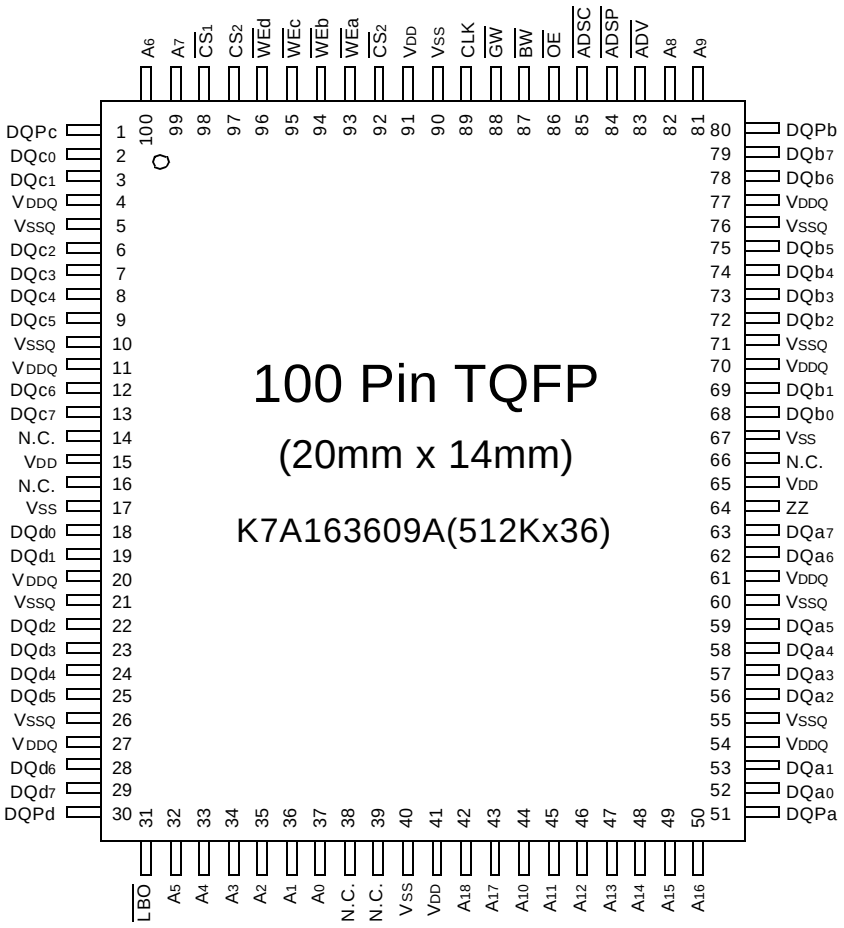
ZZ pin controls Power Down State and reduces Stand-by current regardless of CLK.

The K7A163609A and K7A161809A are fabricated using SAMSUNG's high performance CMOS technology and is available in a 100pin TQFP and 119BGA package. Multiple power and ground pins are utilized to minimize ground bounce.

LOGIC BLOCK DIAGRAM



PIN CONFIGURATION(TOP VIEW)

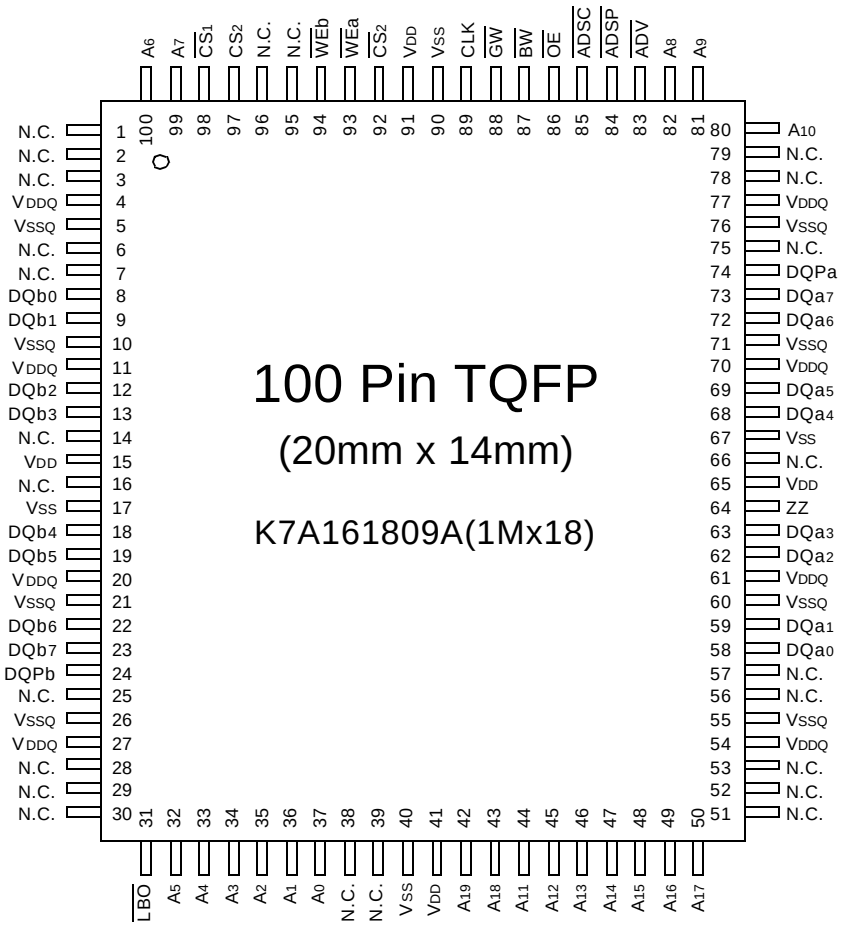


PIN NAME

SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A_0 - A_{18}	Address Inputs	32,33,34,35,36,37,42 43,44,45,46,47,48,49 50,81,82,99,100	V_{DD}	Power Supply(+3.3V)	15,41,65,91
			V_{SS}	Ground	17,40,67,90
$\overline{ADV}$	Burst Address Advance	83	N.C.	No Connect	14,16,38,39,66
$\overline{ADSP}$	Address Status Processor	84			
$\overline{ADSC}$	Address Status Controller	85	$DQa_{0\sim7}$	Data Inputs/Outputs	52,53,56,57,58,59,62,63
CLK	Clock	89	$DQb_{0\sim7}$		68,69,72,73,74,75,78,79
$\overline{CS_1}$	Chip Select	98	$DQc_{0\sim7}$		2,3,6,7,8,9,12,13
CS_2	Chip Select	97	$DQd_{0\sim7}$		18,19,22,23,24,25,28,29
$\overline{CS_2}$	Chip Select	92	$DQPa\sim Pd$		51,80,1,30
$\overline{WEx}$(x=a,b,c,d)	Byte Write Inputs	93,94,95,96			
$\overline{OE}$	Output Enable	86	V_{DDQ}	Output Power Supply (3.3V or 2.5V)	4,11,20,27,54,61,70,77
$\overline{GW}$	Global Write Enable	88			
$\overline{BW}$	Byte Write Enable	87	V_{SSQ}	Output Ground	5,10,21,26,55,60,71,76
$\overline{ZZ}$	Power Down Input	64			
$\overline{LBO}$	Burst Mode Control	31			

Note : 1. A0 and A1 are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

PIN CONFIGURATION (TOP VIEW)



100 Pin TQFP

(20mm x 14mm)

K7A161809A(1Mx18)

PIN NAME

SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A_0 - A_{19}	Address Inputs	32,33,34,35,36,37,42 43,44,45,46,47,48,49 50 80,81,82,99,100	V_{DD}	Power Supply(+3.3V)	15,41,65,91
			V_{SS}	Ground	17,40,67,90
$\overline{ADV}$	Burst Address Advance	83	N.C.	No Connect	1,2,3,6,7,14,16,25,28,29 30,38,39,51,52,53,56,57 66,75,78,79,95,96
$\overline{ADSP}$	Address Status Processor	84			
$\overline{ADSC}$	Address Status Controller	85			
CLK	Clock	89			
$\overline{CS_1}$	Chip Select	98	DQa_0 ~ a_7	Data Inputs/Outputs	58,59,62,63,68,69,72,73
CS_2	Chip Select	97	DQb_0 ~ b_7		8,9,12,13,18,19,22,23
$\overline{CS_2}$	Chip Select	92	DQPa, Pb		74,24
$\overline{WE}$x(x=a,b)	Byte Write Inputs	93,94			
$\overline{OE}$	Output Enable	86	V_{DDQ}	Output Power Supply (3.3V or 2.5V)	4,11,20,27,54,61,70,77
$\overline{GW}$	Global Write Enable	88			
$\overline{BW}$	Byte Write Enable	87	V_{SSQ}	Output Ground	5,10,21,26,55,60,71,76
$\overline{ZZ}$	Power Down Input	64			
LBO	Burst Mode Control	31			

Note : 1. A_0 and A_1 are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

119BGA PACKAGE PIN CONFIGURATIONS

K7A163609A(512Kx36)

	1		3	4		6	7
	VDDQ		A	$\overline{ADSP}$		A	V
B	NC		A	$\overline{ADSC}$		A	NC
	NC	A		VDD		A	NC
	DQc	DQPc	SS	NC	SS	DQPb	
E	DQc		VSS	$\overline{\quad}$1	V	DQb	DQb
	VDDQ		VSS	$\overline{\quad}$	VSS		VDDQ
	DQc	DQc	$\overline{\quad}$c	$\overline{ADV}$	$\overline{\quad}$b	DQb	
H	DQc		VSS	$\overline{\quad}$	VSS		DQb
J	DDQ	V	NC	V	NC	V	VDDQ
	DQd	DQd	SS	CLK	SS	DQa	
L	DQd		$\overline{WE}$d		$\overline{WE}$a		DQa
M	DDQ	DQd	SS	$\overline{BW}$	SS	DQa	DDQ
N		DQd	V	A1	VSS		DQa
P		DQPd	V	A0	VSS		DQa
R		A	$\overline{LBO}$	DD	NC		NC
T		NC	A		A	NC	
U	V	TMS	TDI		TDO	NC	DDQ

Note : 0 and A are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

PIN NAME

	PIN NAME	SYMBOL	
A A , A1	Burst Count Address	V VSS	Power Supply(+3.3V)
$\overline{\quad}$ $\overline{ADSP}$	Burst Address Advance		No Connect
$\overline{ADSC}$	Address Status Controller Clock	DQa DQb	Data Inputs/Outputs
$\overline{CS_1}$ x (x=a,b,c,d)	Byte Write Inputs	DQd DQPa~Pd	Data Inputs/Outputs Data Inputs/Outputs
$\overline{\quad}$ $\overline{GW}$ $\overline{BW}$	Output Enable Byte Write Enable Power Down Input	DDQ	Output Power Supply (2.5V or 3.3V)
$\overline{LBO}$ TCK TDI TDO	JTAG Test Clock JTAG Test Mode Select JTAG Test Data Output		

119BGA PACKAGE PIN CONFIGURATIONS(TOP VIEW)

K7A161809A(1Mx18)

	1	2	3	4	5	6	7
A	V_{DDQ}	A	A	$\overline{ADSP}$	A	A	V_{DDQ}
B	NC	A	A	$\overline{ADSC}$	A	A	NC
C	NC	A	A	V_{DD}	A	A	NC
D	DQb	NC	V_{SS}	NC	V_{SS}	DQPa	NC
E	NC	DQb	V_{SS}	$\overline{CS_1}$	V_{SS}	NC	DQa
F	V_{DDQ}	NC	V_{SS}	$\overline{OE}$	V_{SS}	DQa	V_{DDQ}
G	NC	DQb	$\overline{WE}$b	$\overline{ADV}$	V_{SS}	NC	DQa
H	DQb	NC	V_{SS}	$\overline{GW}$	V_{SS}	DQa	NC
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	NC	DQb	V_{SS}	CLK	V_{SS}	NC	DQa
L	DQb	NC	V_{SS}	NC	$\overline{WE}$a	DQa	NC
M	V_{DDQ}	DQb	V_{SS}	$\overline{BW}$	V_{SS}	NC	V_{DDQ}
N	DQb	NC	V_{SS}	A_1*	V_{SS}	DQa	NC
P	NC	DQPb	V_{SS}	A_0*	V_{SS}	NC	DQa
R	NC	A	$\overline{LBO}$	V_{DD}	NC	A	NC
T	NC	A	A	NC	A	A	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

Note : * A_0 and A_1 are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

PIN NAME

SYMBOL	PIN NAME	SYMBOL	PIN NAME
A	Address Inputs	V_{DD}	Power Supply(+3.3V)
A_0,A_1	Burst Count Address	V_{SS}	Ground
$\overline{ADV}$	Burst Address Advance	N.C.	No Connect
$\overline{ADSP}$	Address Status Processor		
$\overline{ADSC}$	Address Status Controller	DQa	Data Inputs/Outputs
CLK	Clock	DQb	Data Inputs/Outputs
$\overline{CS_1}$	Chip Select	DQPa~Pb	Data Inputs/Outpus
$\overline{WE}$x	Byte Write Inputs		
(x=a,b)		V_{DDQ}	Output Power Supply
			(2.5V or 3.3V)
$\overline{OE}$	Output Enable		
$\overline{GW}$	Global Write Enable		
$\overline{BW}$	Byte Write Enable		
$\overline{ZZ}$	Power Down Input		
$\overline{LBO}$	Burst Mode Control		
TCK	JTAG Test Clock		
TMS	JTAG Test Mode Select		
TDI	JTAG Test Data Input		
TDO	JTAG Test Data Output		