

512Kx36 & 1Mx18-Bit Synchronous Pipelined Burst SRAM

FEATURES

- Synchronous Operation.
- 2 Stage Pipelined operation with 4 Burst.
- On-Chip Address Counter.
- Self-Timed Write Cycle.
- On-Chip Address and Control Registers.
- $V_{DD} = 3.3V \pm 0.165V / -0.165V$ Power Supply.
- I/O Supply Voltage $3.3V \pm 0.165V / -0.165V$ for 3.3V I/O or $2.5V \pm 0.4V / -0.125V$ for 2.5V I/O.
- 5V Tolerant Inputs Except I/O Pins.
- Byte Writable Function.
- Global Write Enable Controls a full bus-width write.
- Power Down State via ZZ Signal.
- LBO Pin allows a choice of either a interleaved burst or a linear burst.
- Three Chip Enables for simple depth expansion with No Data Contention ; 2cycle Enable, 2cycle Disable.
- Asynchronous Output Enable Control.
- ADSP, ADSC, ADV Burst Control Pins.
- TTL-Level Three-State Output.
- 100-TQFP-1420A Package

FAST ACCESS TIMES

PARAMETER	Symbol	-25	-22	-20	Unit
Cycle Time	tCYC	4.0	4.4	5.0	ns
Clock Access Time	tCD	2.6	2.8	3.1	ns
Output Enable Access Time	tOE	2.6	2.8	3.1	ns

GENERAL DESCRIPTION

The K7A163608A and K7A161808A are 18,874,368-bit Synchronous Static Random Access Memory designed for high performance second level cache of Pentium and Power PC based System.

It is organized as 512K(1M) words of 36(18) bits and integrates address and control registers, a 2-bit burst address counter and added some new functions for high performance cache RAM applications; $\overline{GW}$, $\overline{BW}$, $\overline{LBO}$, ZZ. Write cycles are internally self-timed and synchronous.

Full bus-width write is done by $\overline{GW}$, and each byte write is performed by the combination of $\overline{WEx}$ and $\overline{BW}$ when $\overline{GW}$ is high. And with $\overline{CS}_1$ high, $\overline{ADSP}$ is blocked to control signals.

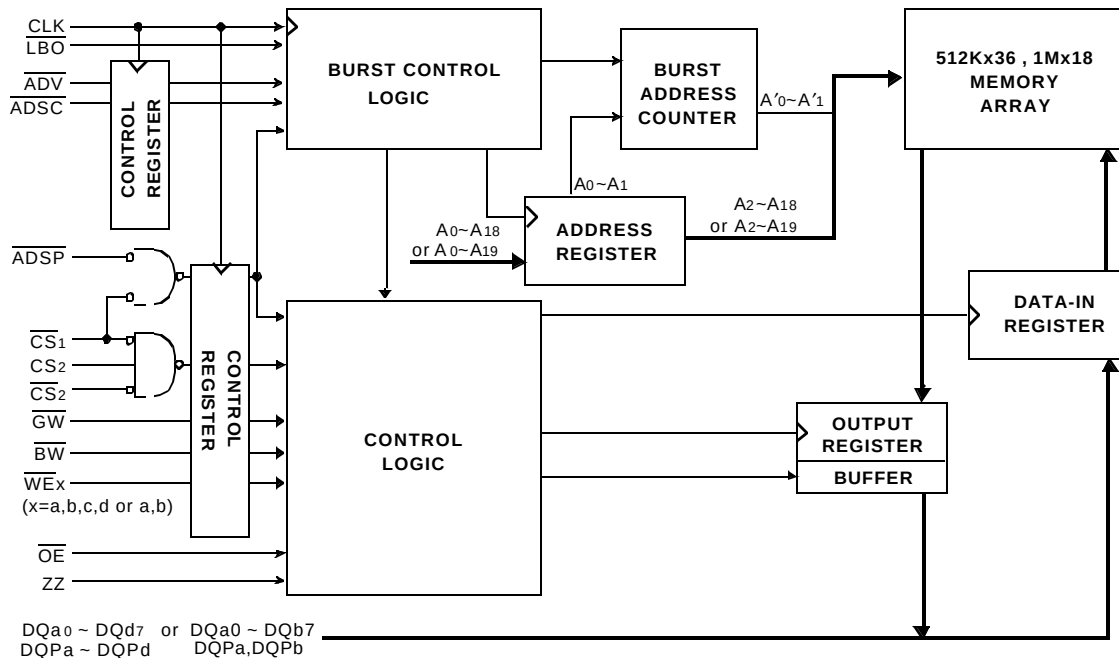
Burst cycle can be initiated with either the address status processor($\overline{ADSP}$) or address status cache controller($\overline{ADSC}$) inputs. Subsequent burst addresses are generated internally in the system's burst sequence and are controlled by the burst address advance($\overline{ADV}$) input.

$\overline{LBO}$ pin is DC operated and determines burst sequence(linear or interleaved).

ZZ pin controls Power Down State and reduces Stand-by current regardless of CLK.

The K7A163608A and K7A161808A are fabricated using SAMSUNG's high performance CMOS technology and is available in a 100pin TQFP package. Multiple power and ground pins are utilized to minimize ground bounce.

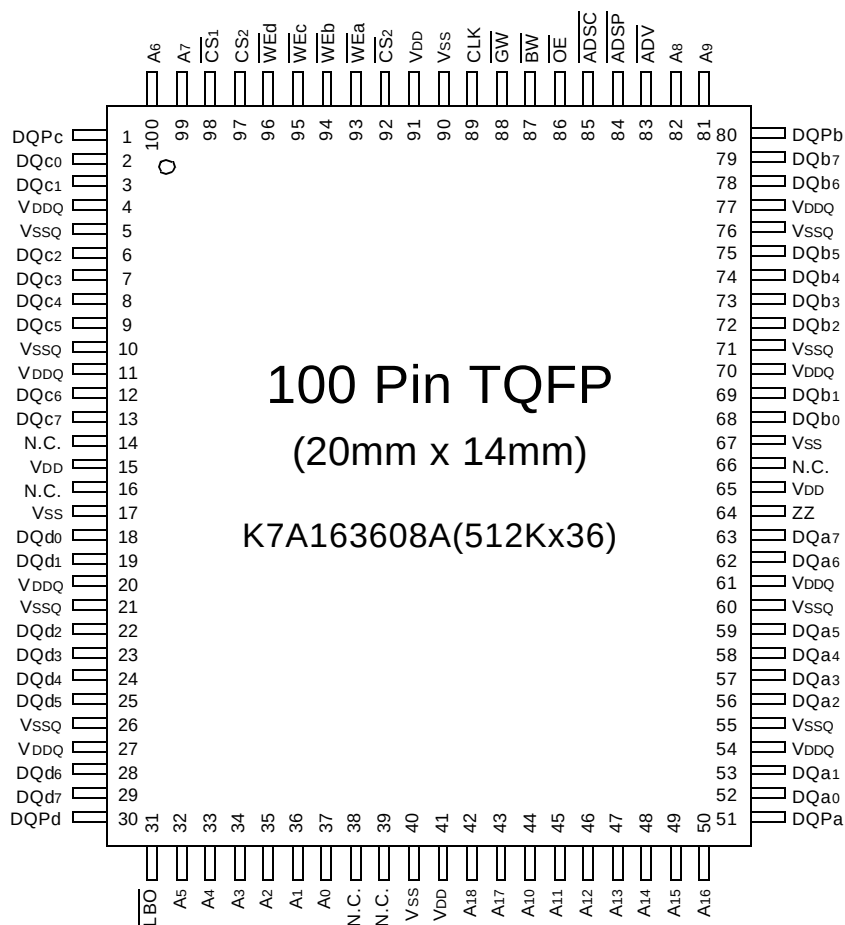
LOGIC BLOCK DIAGRAM



K7A163608A
K7A161808A

PRELIMINARY
512Kx36 & 1Mx18 Synchronous SRAM

PIN CONFIGURATION(TOP VIEW)



PIN NAME

SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A0 - A18	Address Inputs	32,33,34,35,36,37,42,43,44,45,46,47,48,49,50,81,82,99,100	VDD	Power Supply(+3.3V)	15,41,65,91
			VSS	Ground	17,40,67,90
ADV	Burst Address Advance	83	N.C.	No Connect	14,16,38,39,66
ADSP	Address Status Processor	84			
ADSC	Address Status Controller	85	DQa0~a7	Data Inputs/Outputs	52,53,56,57,58,59,62,63
CLK	Clock	89	DQb0~b7		68,69,72,73,74,75,78,79
CS1	Chip Select	98	DQc0~c7		2,3,6,7,8,9,12,13
CS2	Chip Select	97	DQd0~d7		18,19,22,23,24,25,28,29
CS2	Chip Select	92	DQPa~Pd		51,80,1,30
WE _x (x=a,b,c,d)	Byte Write Inputs	93,94,95,96			
OE	Output Enable	86	VDDQ	Output Power Supply (3.3V or 2.5V)	4,11,20,27,54,61,70,77
GW	Global Write Enable	88	VSSQ	Output Ground	5,10,21,26,55,60,71,76
BW	Byte Write Enable	87			
ZZ	Power Down Input	64			
LBO	Burst Mode Control	31			

Note : 1. A₀ and A₁ are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.



ELECTRONICS

PRELIMINARY
512Kx36 & 1Mx18 Synchronous SRAM

[illegible]

SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A0 - A19	Address Inputs	32,33,34,35,36,37,42 43,44,45,46,47,48,49 50 80,81,82,99,100	VDD VSS	Power Supply(+3.3V) Ground	15,41,65,91 17,40,67,90
$\overline{\text{ADV}}$	Burst Address Advance	83	N.C.	No Connect	1,2,3,6,7,14,16,25,28,29
$\overline{\text{ADSP}}$	Address Status Processor	84			30,38,39,51,52,53,56,57
$\overline{\text{ADSC}}$	Address Status Controller	85			66,75,78,79,95,96
CLK	Clock	89			
CS ₁	Chip Select	98	DQa ₀ ~ a ₇	Data Inputs/Outputs	58,59,62,63,68,69,72,73
CS ₂	Chip Select	97	DQb ₀ ~ b ₇		8,9,12,13,18,19,22,23
CS ₂	Chip Select	92	DQPa, Pb		74,24
WE _x (x=a,b)	Byte Write Inputs	93,94			
$\overline{\text{OE}}$	Output Enable	86	VDDQ	Output Power Supply	4,11,20,27,54,61,70,77
$\overline{\text{GW}}$	Global Write Enable	88		(3.3V or 2.5V)	
BW	Byte Write Enable	87	VSSQ	Output Ground	5,10,21,26,55,60,71,76
ZZ	Power Down Input	64			
LBO	Burst Mode Control	31			

Note : 1. A_0 and A_1 are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.