# 512Kx36 & 1Mx18-Bit Synchronous Pipelined Burst SRAM

## FEATURES

- Synchronous Operation.
- 2 Stage Pipelined operation with 4 Burst.
- On-Chip Address Counter.
- Self-Timed Write Cycle.
- On-Chip Address and Control Registers.
- $V_{DD}$= 3.3V +0.165V/-0.165V Power Supply.
- I/O Supply Voltage 3.3V +0.165V/-0.165V for 3.3V I/O or 2.5V+0.4V/-0.125V for 2.5V I/O.
- 5V Tolerant Inputs Except I/O Pins.
- Byte Writable Function.
- Global Write Enable Controls a full bus-width write.
- Power Down State via ZZ Signal.
- $\overline{LBO}$ Pin allows a choice of either a interleaved burst or a linear burst.
- Three Chip Enables for simple depth expansion with No Data Contention ; 2cycle Enable, 2cycle Disable.
- Asynchronous Output Enable Control.
- $\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$ Burst Control Pins.
- TTL-Level Three-State Output.
- 100-TQFP-1420A Package

## FAST ACCESS TIMES

| PARAMETER | Symbol | -16 | -15 | -14 | Unit |
|---|---|---|---|---|---|
| Cycle Time | $t_{CYC}$ | 6.0 | 6.7 | 7.2 | ns |
| Clock Access Time | $t_{CD}$ | 3.5 | 3.8 | 4.0 | ns |
| Output Enable Access Time | $t_{OE}$ | 3.5 | 3.8 | 4.0 | ns |

## GENERAL DESCRIPTION

The K7A163601A and K7A161801A are 18,874,368-bit Synchronous Static Random Access Memory designed for high performance second level cache of Pentium and Power PC based System.

It is organized as 512K(1M) words of 36(18) bits and integrates address and control registers, a 2-bit burst address counter and added some new functions for high performance cache RAM applications; $\overline{GW}$, $\overline{BW}$, $\overline{LBO}$, ZZ. Write cycles are internally self-timed and synchronous.

Full bus-width write is done by $\overline{GW}$, and each byte write is performed by the combination of $\overline{WE}x$ and $\overline{BW}$ when $\overline{GW}$ is high. And with $\overline{CS}_1$ high, $\overline{ADSP}$ is blocked to control signals.

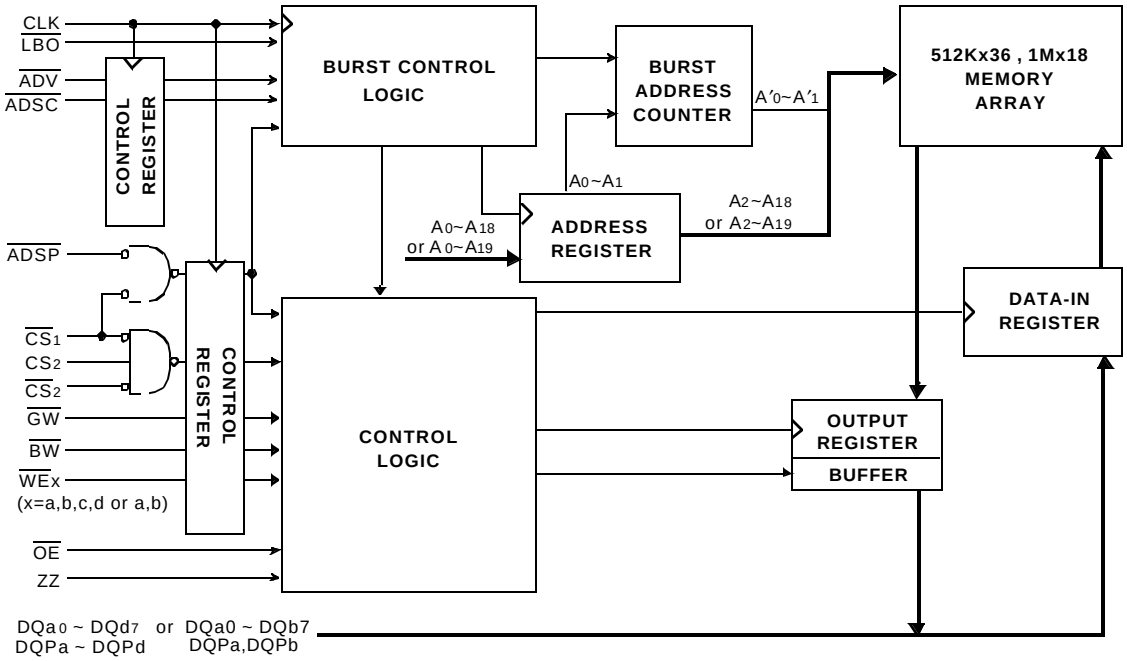
Burst cycle can be initiated with either the address status processor($\overline{ADSP}$) or address status cache controller($\overline{ADSC}$) inputs. Subsequent burst addresses are generated internally in the system's burst sequence and are controlled by the burst address advance($\overline{ADV}$) input.

$\overline{LBO}$ pin is DC operated and determines burst sequence(linear or interleaved).

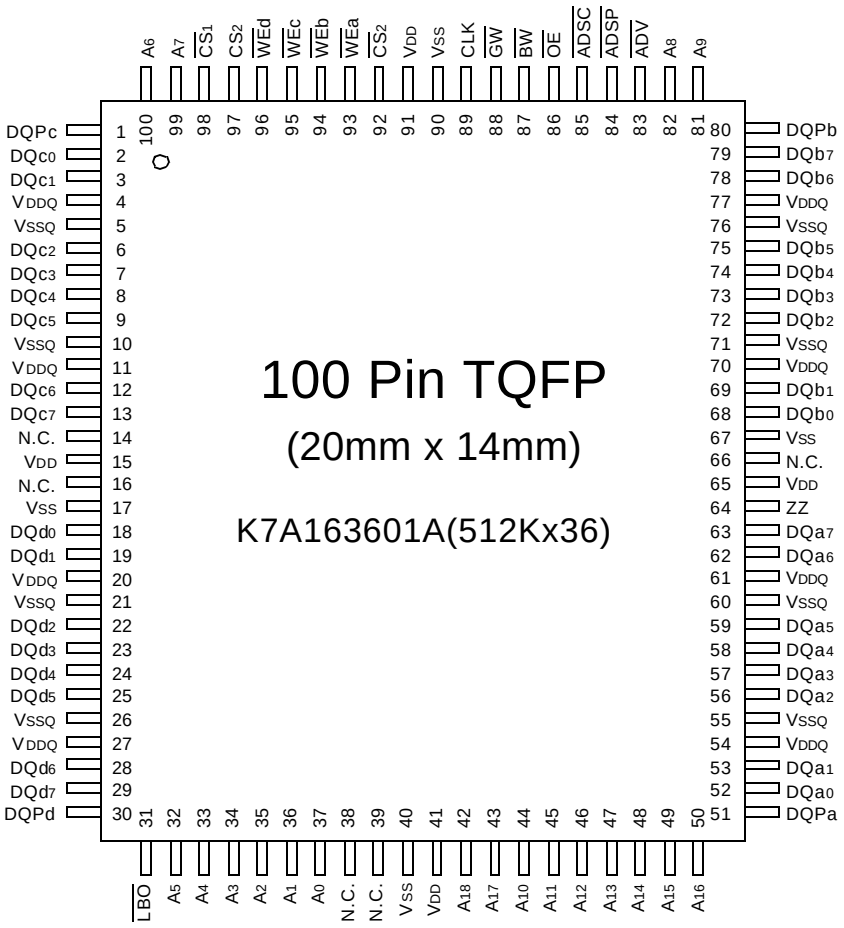
ZZ pin controls Power Down State and reduces Stand-by current regardless of CLK.

The K7A163601A and K7A161801A are fabricated using SAMSUNG's high performance CMOS technology and is available in a 100pin TQFP package. Multiple power and ground pins are utilized to minimize ground bounce.

## LOGIC BLOCK DIAGRAM



## PIN CONFIGURATION(TOP VIEW)

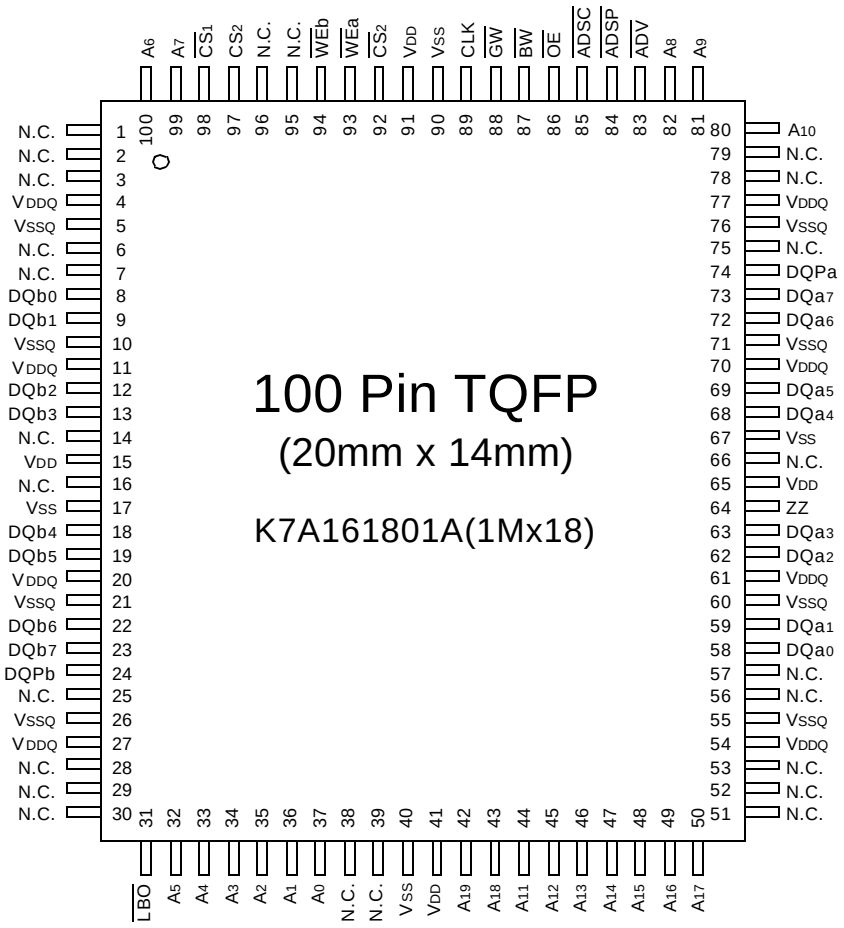



## PIN NAME

| SYMBOL | PIN NAME | TQFP PIN NO. | SYMBOL | PIN NAME | TQFP PIN NO. |
|---|---|---|---|---|---|
| $A_0$ - $A_{18}$ | Address Inputs | 32,33,34,35,36,37,42 | $V_{DD}$ | Power Supply(+3.3V) | 15,41,65,91 |
| | | 43,44,45,46,47,48,49 | $V_{SS}$ | Ground | 17,40,67,90 |
| | | 50,81,82,99,100 | | | |
| $\overline{ADV}$ | Burst Address Advance | 83 | N.C. | No Connect | 14,16,38,39,66 |
| $\overline{ADSP}$ | Address Status Processor | 84 | | | |
| $\overline{ADSC}$ | Address Status Controller | 85 | $DQa_0$~$a_7$ | Data Inputs/Outputs | 52,53,56,57,58,59,62,63 |
| CLK | Clock | 89 | $DQb_0$~$b_7$ | | 68,69,72,73,74,75,78,79 |
| $\overline{CS_1}$ | Chip Select | 98 | $DQc_0$~$c_7$ | | 2,3,6,7,8,9,12,13 |
| $CS_2$ | Chip Select | 97 | $DQd_0$~$d_7$ | | 18,19,22,23,24,25,28,29 |
| $\overline{CS_2}$ | Chip Select | 92 | DQPa~$P_d$ | | 51,80,1,30 |
| $\overline{WE}$x(x=a,b,c,d) | Byte Write Inputs | 93,94,95,96 | | | |
| $\overline{OE}$ | Output Enable | 86 | $V_{DDQ}$ | Output Power Supply | 4,11,20,27,54,61,70,77 |
| $\overline{GW}$ | Global Write Enable | 88 | | (3.3V or 2.5V) | |
| $\overline{BW}$ | Byte Write Enable | 87 | $V_{SSQ}$ | Output Ground | 5,10,21,26,55,60,71,76 |
| $\overline{ZZ}$ | Power Down Input | 64 | | | |
| $\overline{LBO}$ | Burst Mode Control | 31 | | | |

**Note :** 1. $A_0$ and $A_1$ are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

## PIN CONFIGURATION (TOP VIEW)

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|---|---|---|---|---|---|
| $A_0$ - $A_{19}$ | Address Inputs | 32,33,34,35,36,37,42 43,44,45,46,47,48,49 50 80,81,82,99,100 | $V_{DD}$ | Power Supply(+3.3V) | 15,41,65,91 |
| | | | $V_{SS}$ | Ground | 17,40,67,90 |
| $\overline{ADV}$ | Burst Address Advance | 83 | N.C. | No Connect | 1,2,3,6,7,14,16,25,28,29 30,38,39,51,52,53,56,57 66,75,78,79,95,96 |
| $\overline{ADSP}$ | Address Status Processor | 84 | | | |
| $\overline{ADSC}$ | Address Status Controller | 85 | | | |
| CLK | Clock | 89 | | | |
| $\overline{CS_1}$ | Chip Select | 98 | $DQa_0$ ~ $a_7$ | Data Inputs/Outputs | 58,59,62,63,68,69,72,73 |
| $CS_2$ | Chip Select | 97 | $DQb_0$ ~ $b_7$ | | 8,9,12,13,18,19,22,23 |
| $\overline{CS_2}$ | Chip Select | 92 | DQPa, Pb | | 74,24 |
| $\overline{WE}$x(x=a,b) | Byte Write Inputs | 93,94 | | | |
| $\overline{OE}$ | Output Enable | 86 | $V_{DDQ}$ | Output Power Supply (3.3V or 2.5V) | 4,11,20,27,54,61,70,77 |
| $\overline{GW}$ | Global Write Enable | 88 | | | |
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