

Document Title

256Kx36 & 512Kx18-Bit Pipelined NtRAM™

Revision History

<u>Rev. No.</u>	<u>History</u>	<u>Draft Date</u>	<u>Remark</u>
0.0	1. Initial document.	May . 18. 2001	Preliminary

The attached data sheets are prepared and approved by SAMSUNG Electronics. SAMSUNG Electronics CO., LTD. reserve the right to change the specifications. SAMSUNG Electronics will evaluate and reply to your requests and questions on the parameters of this device. If you have any ques- tions, please contact the SAMSUNG branch office near your office, call or contact Headquarters.

8Mb NtRAM(Flow Through / Pipelined) Ordering Information

Org.	Part Number	Mode	VDD	Speed FT ; Access Time(ns) Pipelined ; Cycle Time(MHz)	PKG	Temp
512Kx18	K7M801825B-Q(H)C65/75/85/90	FlowThrough	3.3	6.5/7.5/8.5/9.0 ns	Q: 100TQFP H: 119BGA	C: Commercial Temperature Range
	K7N801801B-Q(H)C16/15/13	Pipelined	3.3	167/150/133 MHz		
	K7N801809B-Q(H)C25/22/20	Pipelined	3.3	250/225/200 MHz		
	K7N801845B-Q(H)C16/15/13	Pipelined	2.5	167/150/133 MHz		
	K7N801849B-Q(H)C25/22/20	Pipelined	2.5	250/225/200 MHz		
256Kx36	K7M803625B-Q(H)C65/75/85/90	FlowThrough	3.3	6.5/7.5/8.5/9.0 ns		
	K7N803601B-Q(H)C16/15/13	Pipelined	3.3	167/150/133 MHz		
	K7N803609B-Q(H)C25/22/20	Pipelined	3.3	250/225/200 MHz		
	K7N803645B-Q(H)C16/15/13	Pipelined	2.5	167/150/133 MHz		
	K7N803649B-Q(H)C25/22/20	Pipelined	2.5	250/225/200 MHz		

256Kx36 & 512Kx18-Bit Pipelined NtRAM™

FEATURES

- 2.5V $\pm 5\%$ Power Supply.
- Byte Writable Function.
- Enable clock and suspend operation.
- Single READ/WRITE control pin.
- Self-Timed Write Cycle.
- Three Chip Enable for simple depth expansion with no data contention.
- A interleaved burst or a linear burst mode.
- Asynchronous output enable control.
- Power Down mode.
- TTL-Level Three-State Outputs.
- 100-TQFP-1420A / 119BGA(7x17 Ball Grid Array Package).

GENERAL DESCRIPTION

The K7N803649B and K7N801849B are 9,437,184 bits Synchronous Static SRAMs.

The NtRAM™, or No Turnaround Random Access Memory utilizes all the bandwidth in any combination of operating cycles. Address, data inputs, and all control signals except output enable and linear burst order are synchronized to input clock. Burst order control must be tied "High or Low".

Asynchronous inputs include the sleep mode enable(ZZ).

Output Enable controls the outputs at any given time.

Write cycles are internally self-timed and initiated by the rising edge of the clock input. This feature eliminates complex off-chip write pulse generation

and provides increased timing flexibility for incoming signals.

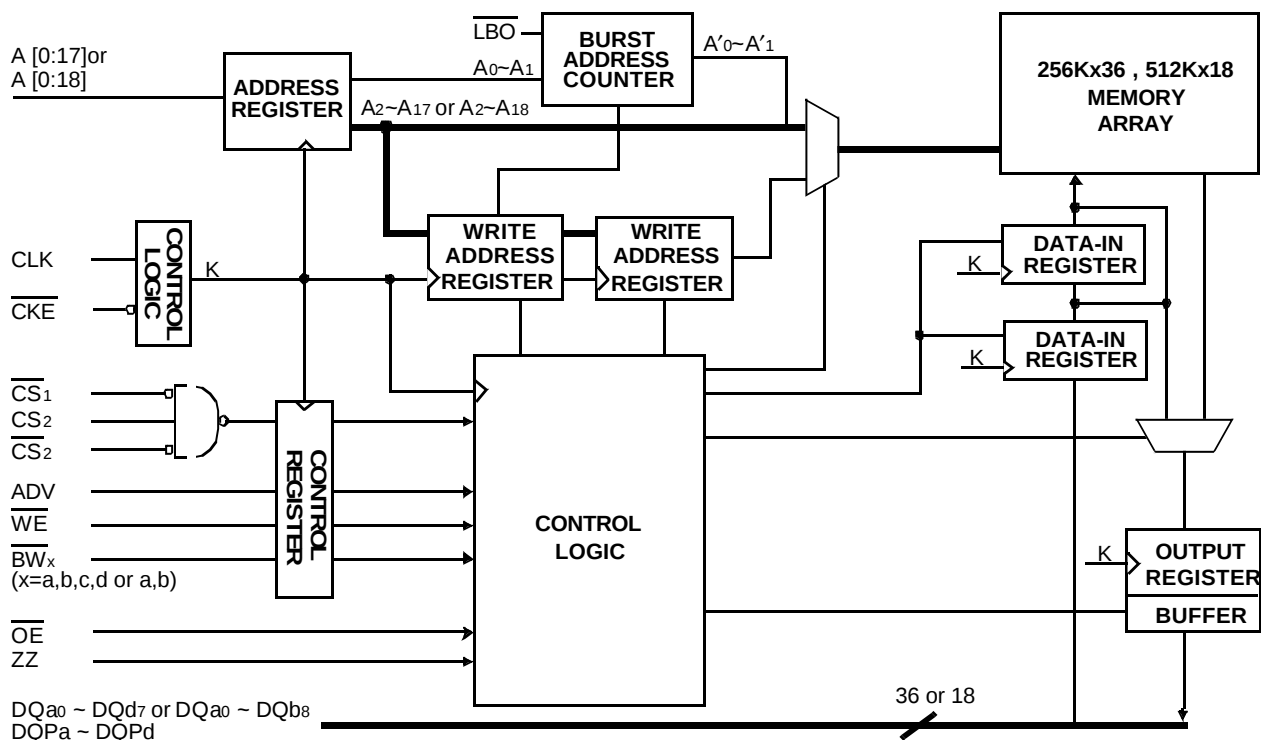
For read cycles, pipelined SRAM output data is temporarily stored by an edge triggered output register and then released to the output buffers at the next rising edge of clock.

The K7N803649B and K7N801849B are implemented with SAMSUNG's high performance CMOS technology and is available in 100pin TQFP and 119BGA packages. Multiple power and ground pins minimize ground bounce.

FAST ACCESS TIMES

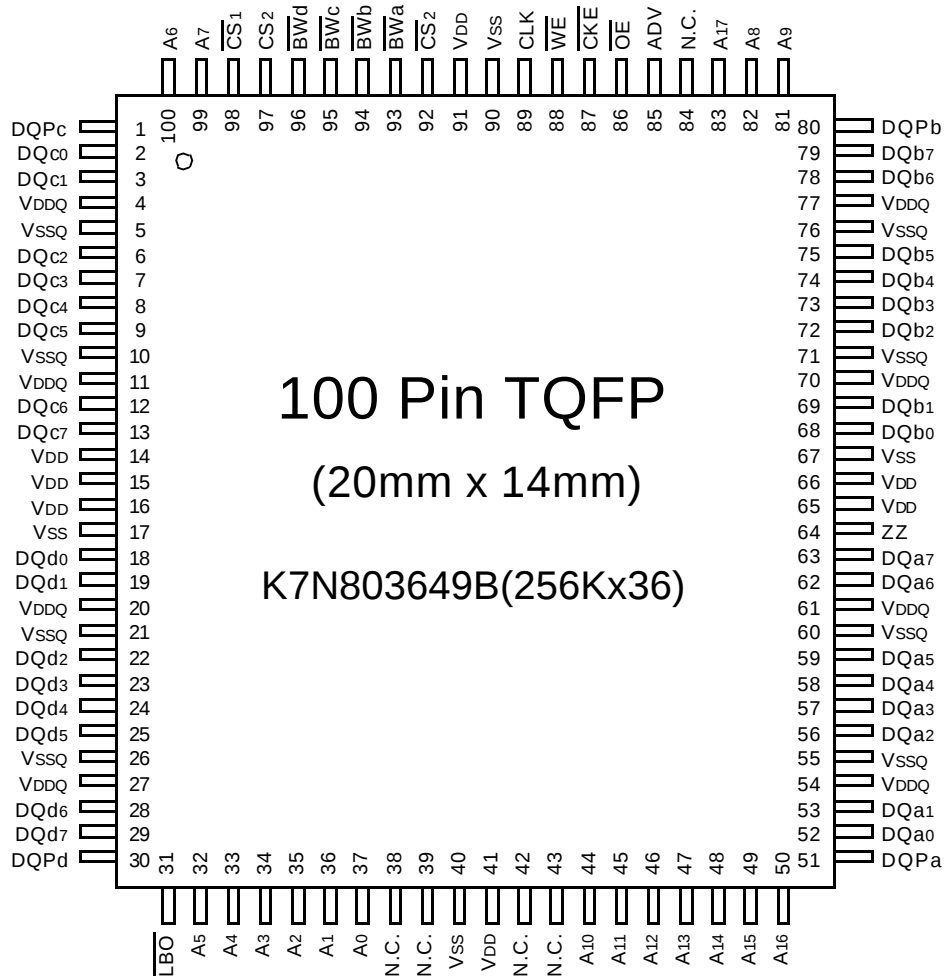
PARAMETER	Symbol	-25	-22	-20	Unit
Cycle Time	tCYC	4.0	4.4	5.0	ns
Clock Access Time	tCD	2.6	2.8	3.2	ns
Output Enable Access Time	tOE	2.6	2.8	3.2	ns

LOGIC BLOCK DIAGRAM



NtRAM™ and No Turnaround Random Access Memory are trademarks of Samsung, and its architecture and functionalities are supported by NEC and Toshiba.

PIN CONFIGURATION(TOP VIEW)

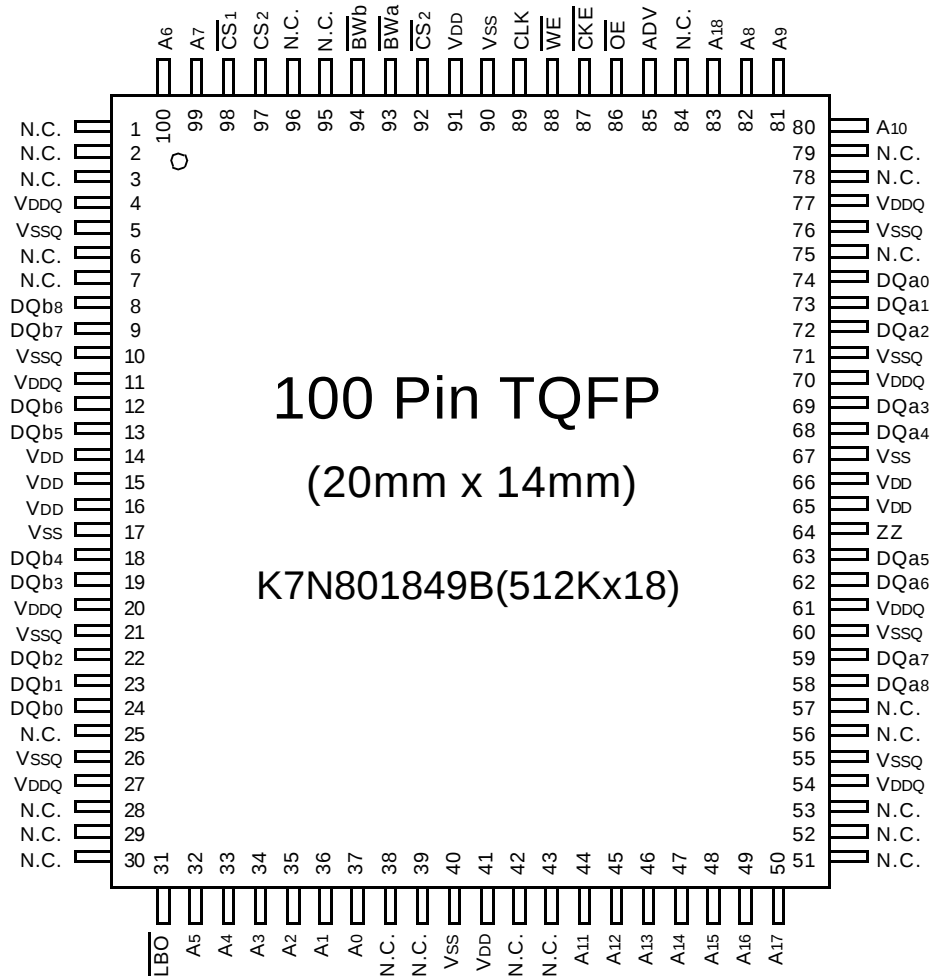


PIN NAME

SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A0 - A17	Address Inputs	32,33,34,35,36,37,44,45,46,47,48,49,50,81,82,83,99,100	VDD	Power Supply(+2.5V)	14,15,16,41,65,66,91
ADV	Address Advance/Load	85	Vss	Ground	17,40,67,90
WE	Read/Write Control Input	88	N.C.	No Connect	38,39,42,43,84
CLK	Clock	89	DQa0~a7	Data Inputs/Outputs	52,53,56,57,58,59,62,63
CKE	Clock Enable	87	DQb0~b7		68,69,72,73,74,75,78,79
CS1	Chip Select	98	DQc0~c7		2,3,6,7,8,9,12,13
CS2	Chip Select	97	DQd0~d7		18,19,22,23,24,25,28,29
CS2	Chip Select	92	DQPa~Pd		51,80,1,30
BWx	Byte Write Inputs	93,94,95,96	VDDQ	Output Power Supply (+2.5V)	4,11,20,27,54,61,70,77
OE	Output Enable	86	VssQ	Output Ground	5,10,21,26,55,60,71,76
ZZ	Power Sleep Mode	64			
LBO	Burst Mode Control	31			

Notes : 1. The pin 84 is reserved for address bit for the 16Mb NtRAM.
2. A₀ and A₁ are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

PIN CONFIGURATION(TOP VIEW)



PIN NAME

SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A0 - A18	Address Inputs	32,33,34,35,36,37,44,45,46,47,48,49,50,80,81,82,83,99,100	VDD	Power Supply(+2.5V)	14,15,16,41,65,66,91
			VSS	Ground	17,40,67,90
			N.C.	No Connect	1,2,3,6,7,25,28,29,30,38,39,42,43,51,52,53,56,57,75,78,79,84,95,96
ADV	Address Advance/Load	85			
WE	Read/Write Control Input	88			
CLK	Clock	89			
CKE	Clock Enable	87	DQa0~a8	Data Inputs/Outputs	58,59,62,63,68,69,72,73,74
CS1	Chip Select	98	DQb0~b8		8,9,12,13,18,19,22,23,24
CS2	Chip Select	97			
CS2	Chip Select	92			
BWx	Byte Write Inputs	93,94	VDDQ	Output Power Supply (+2.5V)	4,11,20,27,54,61,70,77
OE	Output Enable	86	VSSQ	Output Ground	5,10,21,26,55,60,71,76
ZZ	Power Sleep Mode	64			
LBO	Burst Mode Control	31			

Notes : 1. The pin 84 is reserved for address bit for the 16Mb NtRAM.
2. A0 and A1 are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

119BGA PACKAGE PIN CONFIGURATIONS (TOP VIEW)

K7N803649B(256Kx36)

	1	2	3	4	5	6	7
A	VDDQ	A	A	NC**	A	A	VDDQ
B	NC	CS2	A	ADV	A	$\overline{CS}2$	NC
C	NC	A	A	VDD	A	A	NC
D	DQc	DQPc	Vss	NC	Vss	DQPb	DQb
E	DQc	DQc	Vss	$\overline{CS}1$	Vss	DQb	DQb
F	VDDQ	DQc	Vss	$\overline{OE}$	Vss	DQb	VDDQ
G	DQc	DQc	$\overline{BW}c$	A	$\overline{BW}b$	DQb	DQb
H	DQc	DQc	Vss	$\overline{WE}$	Vss	DQb	DQb
J	VDDQ	VDD	NC	VDD	NC	VDD	VDDQ
K	DQd	DQd	Vss	CLK	Vss	DQa	DQa
L	DQd	DQd	$\overline{BW}d$	NC	$\overline{BW}a$	DQa	DQa
M	VDDQ	DQd	Vss	$\overline{CKE}$	Vss	DQa	VDDQ
N	DQd	DQd	Vss	A1*	Vss	DQa	DQa
P	DQd	DQPd	Vss	A0*	Vss	DQPa	DQa
R	NC	A	$\overline{LBO}$	VDD	NC	A	NC
T	NC	NC	A	A	A	NC	ZZ
U	VDDQ	TMS	TDI	TCK	TDO	NC	VDDQ

Note : * A₀ and A₁ are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

** Pin 4A is reserved for address expansion to 16Mb.

PIN NAME

SYMBOL	PIN NAME	SYMBOL	PIN NAME
A	Address Inputs	VDD	Power Supply
A ₀ ,A ₁	Burst Address Inputs	Vss	Ground
ADV	Address Advance/Load	N.C.	No Connect
$\overline{WE}$	Read/Write Control Input		
CLK	Clock	DQa	Data Inputs/Outputs
$\overline{CKE}$	Clock Enable	DQb	Data Inputs/Outputs
$\overline{CS}1$	Chip Select	DQc	Data Inputs/Outputs
$\overline{CS}2$	Chip Select	DQd	Data Inputs/Outputs
$\overline{CS}2$	Chip Select	DQPa~Pd	Data Inputs/Outputs
$\overline{BW}x$	Byte Write Inputs		
(x=a,b,c,d)		VDDQ	Output Power Supply
$\overline{OE}$	Output Enable		
ZZ	Power Sleep Mode		
$\overline{LBO}$	Burst Mode Control		
TCK	JTAG Test Clock		
TMS	JTAG Test Mode Select		
TDI	JTAG Test Data Input		
TDO	JTAG Test Data Output		

119BGA PACKAGE PIN CONFIGURATIONS (TOP VIEW)

K7N801849B(512Kx18)

	1	2	3	4	5	6	7
A	VDDQ	A	A	NC**	A	A	VDDQ
B	NC	CS2	A	ADV	A	$\overline{CS}2$	NC
C	NC	A	A	VDD	A	A	NC
D	DQb	NC	VSS	NC	VSS	DQPa	NC
E	NC	DQb	VSS	$\overline{CS}1$	VSS	NC	DQa
F	VDDQ	NC	VSS	$\overline{OE}$	VSS	DQa	VDDQ
G	NC	DQb	$\overline{BW}b$	A	VSS	NC	DQa
H	DQb	NC	VSS	$\overline{WE}$	VSS	DQa	NC
J	VDDQ	VDD	NC	VDD	NC	VDD	VDDQ
K	NC	DQb	VSS	CLK	VSS	NC	DQa
L	DQb	NC	VSS	NC	$\overline{BW}a$	DQa	NC
M	VDDQ	DQb	VSS	$\overline{CKE}$	VSS	NC	VDDQ
N	DQb	NC	VSS	A1*	VSS	DQa	NC
P	NC	DQPb	VSS	A0*	VSS	NC	DQa
R	NC	A	$\overline{LBO}$	VDD	NC	A	NC
T	NC	A	A	NC	A	A	ZZ
U	VDDQ	TMS	TDI	TCK	TDO	NC	VDDQ

Note : * A₀ and A₁ are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

** Pin 4A is reserved for address expansion to 16Mb.

PIN NAME

SYMBOL	PIN NAME	SYMBOL	PIN NAME
A	Address Inputs	VDD	Power Supply
A ₀ ,A ₁	Burst Address Inputs	VSS	Ground
ADV	Address Advance/Load	N.C.	No Connect
$\overline{WE}$	Read/Write Control Input		
CLK	Clock		
$\overline{CKE}$	Clock Enable	DQa	Data Inputs/Outputs
$\overline{CS}1$	Chip Select	DQb	Data Inputs/Outputs
CS ₂	Chip Select	DQPa, Pb	Data Inputs/Outputs
$\overline{CS}2$	Chip Select		
$\overline{BW}x$	Byte Write Inputs	VDDQ	Output Power Supply
(x=a,b)			
$\overline{OE}$	Output Enable		
ZZ	Power Sleep Mode		
$\overline{LBO}$	Burst Mode Control		
TCK	JTAG Test Clock		
TMS	JTAG Test Mode Select		
TDI	JTAG Test Data Input		
TDO	JTAG Test Data Output		

FUNCTION DESCRIPTION

The K7N803649B and K7N801849B are NtRAM™ designed to sustain 100% bus bandwidth by eliminating turnaround cycle when there is transition from Read to Write, or vice versa.

All inputs (with the exception of $\overline{OE}$, $\overline{LBO}$ and $\overline{ZZ}$) are synchronized to rising clock edges.

All read, write and deselect cycles are initiated by the ADV input. Subsequent burst addresses can be internally generated by the burst advance pin (ADV). ADV should be driven to Low once the device has been deselected in order to load a new address for next operation.

Clock Enable($\overline{CKE}$) pin allows the operation of the chip to be suspended as long as necessary. When $\overline{CKE}$ is high, all synchronous inputs are ignored and the internal device registers will hold their previous values.

NtRAM™ latches external address and initiates a cycle, when $\overline{CKE}$, ADV are driven to low and all three chip enables($\overline{CS1}$, $\overline{CS2}$, $\overline{CS2}$) are active .

Output Enable($\overline{OE}$) can be used to disable the output at any given time.

Read operation is initiated when at the rising edge of the clock, the address presented to the address inputs are latched in the address register, $\overline{CKE}$ is driven low, all three chip enables($\overline{CS1}$, $\overline{CS2}$, $\overline{CS2}$) are active, the write enable input signals $\overline{WE}$ are driven high, and ADV driven low. The internal array is read between the first rising edge and the second rising edge of the clock and the data is latched in the output register. At the second clock edge the data is driven out of the SRAM. Also during read operation $\overline{OE}$ must be driven low for the device to drive out the requested data.

Write operation occurs when $\overline{WE}$ is driven low at the rising edge of the clock. $\overline{BW[d:a]}$ can be used for byte write operation. The pipelined NtRAM™ uses a late-late write cycle to utilize 100% of the bandwidth.

At the first rising edge of the clock, $\overline{WE}$ and address are registered, and the data associated with that address is required two cycle later.

Subsequent addresses are generated by ADV High for the burst access as shown below. The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion.

The burst sequence is determined by the state of the $\overline{LBO}$ pin. When this pin is low, linear burst sequence is selected.

And when this pin is high, Interleaved burst sequence is selected.

During normal operation, $\overline{ZZ}$ must be driven low. When $\overline{ZZ}$ is driven high, the SRAM will enter a Power Sleep Mode after 2 cycles. At this time, internal state of the SRAM is preserved. When $\overline{ZZ}$ returns to low, the SRAM normally operates after 2 cycles of wake up time.

BURST SEQUENCE TABLE

(Interleaved Burst, $\overline{LBO}$ =High)

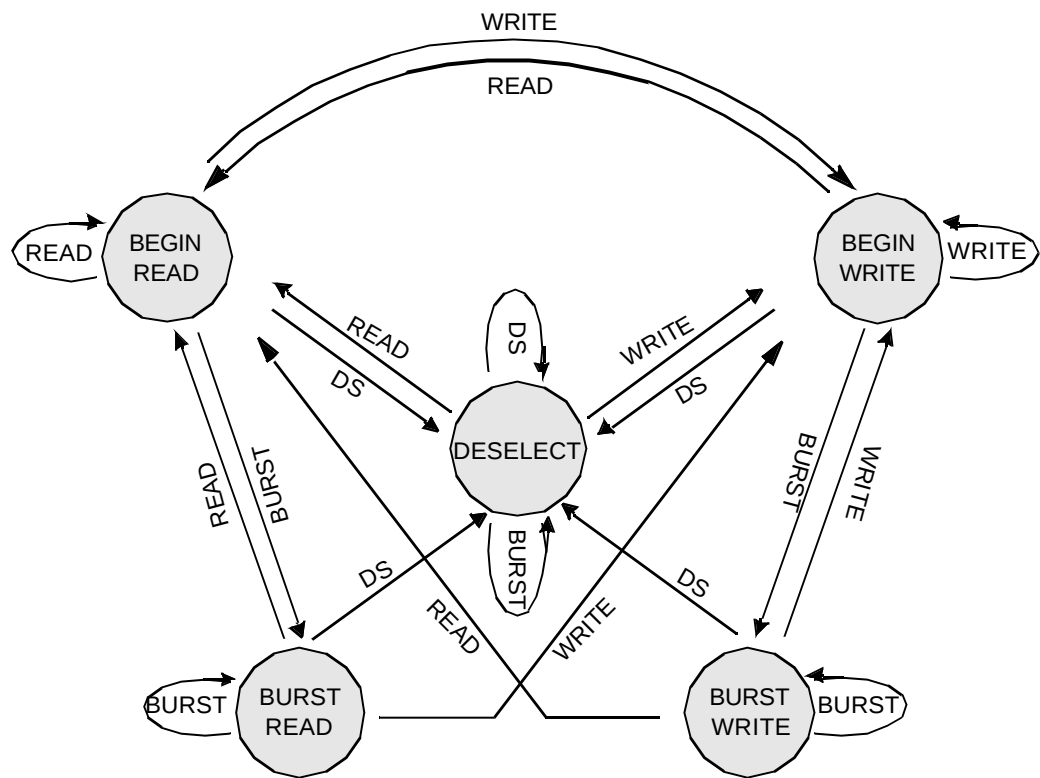
$\overline{\text{LBO}}$ PIN	HIGH	Case 1		Case 2		Case 3		Case 4	
		A ₁	A ₀	A ₁	A ₀	A ₁	A ₀	A ₁	A ₀
First Address ↓ Fourth Address		0	0	0	1	1	0	1	1
		0	1	0	0	1	1	1	0
		1	0	1	1	0	0	0	1
		1	1	1	0	0	1	0	0

(Linear Burst, $\overline{LBO}$ =Low)

$\overline{\text{LBO}}$ PIN	LOW	Case 1		Case 2		Case 3		Case 4	
		A1	A0	A1	A0	A1	A0	A1	A0
First Address ↓ Fourth Address		0	0	0	1	1	0	1	1
		0	1	1	0	1	1	0	0
		1	0	1	1	0	0	0	1
		1	1	0	0	0	1	1	0

Note : 1. $\overline{LBO}$ pin must be tied to High or Low, and Floating State must not be allowed.

STATE DIAGRAM FOR NtRAM™



COMMAND	ACTION
DS	DESELECT
READ	BEGIN READ
WRITE	BEGIN WRITE
BURST	BEGIN READ BEGIN WRITE CONTINUE DESELECT

Notes : 1. An IGNORE CLOCK EDGE cycle is not shown in the above diagram. This is because CKE HIGH only blocks the clock(CLK) input and does not change the state of the device.
2. States change on the rising edge of the clock(CLK)

TRUTH TABLES

SYNCHRONOUS TRUTH TABLE

CS ₁	CS ₂	CS ₂	ADV	WE	BW _x	OE	CKE	CLK	ADDRESS ACCESSED	OPERATION
H	X	X	L	X	X	X	L	↑	N/A	Not Selected
X	L	X	L	X	X	X	L	↑	N/A	Not Selected
X	X	H	L	X	X	X	L	↑	N/A	Not Selected
X	X	X	H	X	X	X	L	↑	N/A	Not Selected Continue
L	H	L	L	H	X	L	L	↑	External Address	Begin Burst Read Cycle
X	X	X	H	X	X	L	L	↑	Next Address	Continue Burst Read Cycle
L	H	L	L	H	X	H	L	↑	External Address	NOP/Dummy Read
X	X	X	H	X	X	H	L	↑	Next Address	Dummy Read
L	H	L	L	L	L	X	L	↑	External Address	Begin Burst Write Cycle
X	X	X	H	X	L	X	L	↑	Next Address	Continue Burst Write Cycle
L	H	L	L	L	H	X	L	↑	N/A	NOP/Write Abort
X	X	X	H	X	H	X	L	↑	Next Address	Write Abort
X	X	X	X	X	X	X	H	↑	Current Address	Ignore Clock

- Notes :** 1. X means "Don't Care". 2. The rising edge of clock is symbolized by (↑).
3. A continue deselect cycle can only be entered if a deselect cycle is executed first.
4. WRITE = L means Write operation in WRITE TRUTH TABLE.
WRITE = H means Read operation in WRITE TRUTH TABLE.
5. Operation finally depends on status of asynchronous input pins(ZZ and OE).

WRITE TRUTH TABLE_(x36)

<u>WE</u>	<u>BW</u> a	<u>BW</u> b	<u>BW</u> c	<u>BW</u> d	OPERATION
H	X	X	X	X	READ
L	L	H	H	H	WRITE BYTE a
L	H	L	H	H	WRITE BYTE b
L	H	H	L	H	WRITE BYTE c
L	H	H	H	L	WRITE BYTE d
L	L	L	L	L	WRITE ALL BYTES
L	H	H	H	H	WRITE ABORT/NOP

- Notes :** 1. X means "Don't Care".
2. All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).

WRITE TRUTH TABLE_(x18)

<u>WE</u>	<u>BW</u> a	<u>BW</u> b	OPERATION
H	X	X	READ
L	L	H	WRITE BYTE a
L	H	L	WRITE BYTE b
L	L	L	WRITE ALL BYTES
L	H	H	WRITE ABORT/NOP

- Notes :** 1. X means "Don't Care".
2. All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).

ASYNCHRONOUS TRUTH TABLE

Operation	ZZ	$\overline{OE}$	I/O STATUS
Sleep Mode	H	X	High-Z
Read	L	L	DQ
	L	H	High-Z
Write	L	X	Din, High-Z
Deselected	L	X	High-Z

Notes

1. X means "Don't Care".
2. Sleep Mode means power Sleep Mode of which stand-by current does not depend on cycle time.
3. Deselected means power Sleep Mode of which stand-by current depends on cycle time.

ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Voltage on VDD Supply Relative to VSS	VDD	-0.3 to 3.6	V
Voltage on Any Other Pin Relative to VSS	VIN	-0.3 to VDD+0.3	V
Power Dissipation	Pd	1.4	W
Storage Temperature	TSTG	-65 to 150	°C
Operating Temperature	TOPR	0 to 70	°C
Storage Temperature Range Under Bias	TBIAS	-10 to 85	°C

*Note : Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING CONDITIONS(0°C ≤ TA ≤ 70°C)

PARAMETER	SYMBOL	MIN	Typ.	MAX	UNIT
Supply Voltage	VDD	2.375	2.5	2.625	V
	VDDQ	2.375	2.5	2.625	V
Ground	VSS	0	0	0	V

*Note : VDD and VDDQ must be supplied with identical voltage levels.

CAPACITANCE*(TA=25°C, f=1MHz)

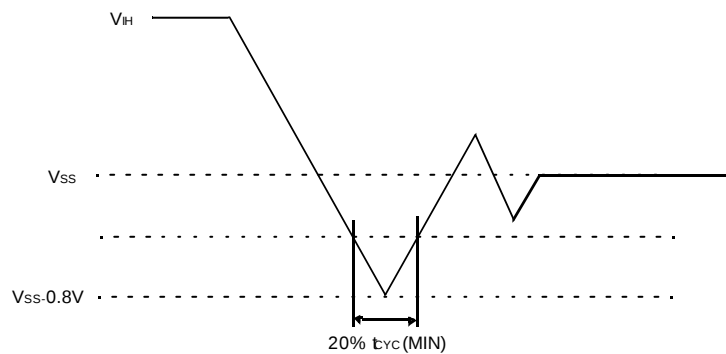
PARAMETER	SYMBOL	TEST CONDI-	MIN	MAX	UNIT
Input Capacitance	CIN	VIN=0V	-	5	pF
Output Capacitance	COUT	VOUT=0V	-	7	pF

*Note : Sampled not 100% tested.

DC ELECTRICAL CHARACTERISTICS ($V_{DD}=2.5V \pm 5\%$, $T_A=0^\circ C$ to $+70^\circ C$)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNIT	NOTES
Input Leakage Current(except ZZ)	IIL	$V_{DD}=\text{Max}$; $V_{IN}=V_{SS}$ to V_{DD}	-2	+2	μA	
Output Leakage Current	IOL	Output Disabled,	-2	+2	μA	
Operating Current	ICC	$V_{DD}=\text{Max}$ $I_{OUT}=0mA$ Cycle Time $\geq t_{CYC}$ Min	-25	-	440	mA 1,2
			-22	-	410	
			-20	-	380	
Standby Current	ISB	Device deselected, $I_{OUT}=0mA$, $ZZ \leq V_{IL}$, $f=\text{Max}$, All Inputs $\leq 0.2V$ or $\geq V_{DD}-0.2V$	-25	-	160	mA
			-22	-	150	
			-20	-	140	
	ISB1	Device deselected, $I_{OUT}=0mA$, $ZZ \leq 0.2V$, $f=0$, All Inputs=fixed ($V_{DD}-0.2V$ or $0.2V$)	-	80	mA	
	ISB2	Device deselected, $I_{OUT}=0mA$, $ZZ \geq V_{DD}-0.2V$, $f=\text{Max}$, All Inputs $\leq V_{IL}$ or $\geq V_{IH}$	-	40	mA	
Output Low Voltage	VOL	$I_{OL}=1.0mA$	-	0.4	V	
Output High Voltage	VOH	$I_{OH}=-1.0mA$	2.0	-	V	
Input Low Voltage	VIL		-0.3*	0.7	V	
Input High Voltage	VIH		1.7	$V_{DD}+0.3^{**}$	V	3

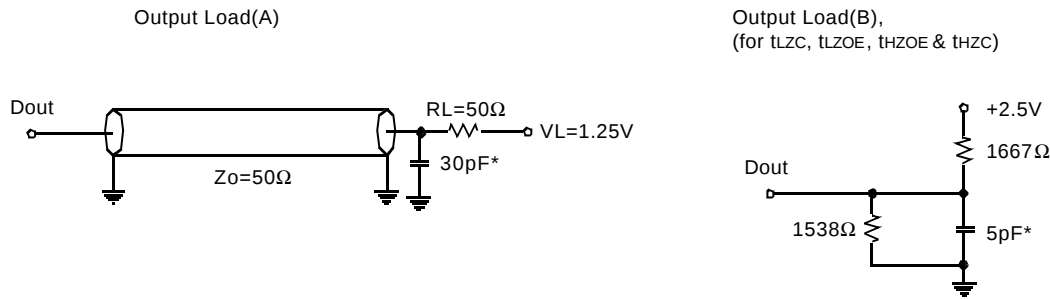
Notes : 1. Reference AC Operating Conditions and Characteristics for input and timing.
2. Data states are all zero.
3. In Case of I/O Pins, the Max. $V_{IH}=V_{DDQ}+0.3V$



TEST CONDITIONS

($T_A=0$ to $70^\circ C$, $V_{DD}=2.5V \pm 5\%$, unless otherwise specified)

PARAMETER	VALUE
Input Pulse Level	0 to 2.5V
Input Rise and Fall Time(Measured at 20% to 80%)	1.0V/ns
Input and Output Timing Reference Levels	1.25V
Output Load	See Fig. 1



* Including Scope and Jig Capacitance

Fig. 1

AC TIMING CHARACTERISTICS

(VDD=2.5V ±5%, TA=0 to 70°C)

PARAMETER	SYMBOL	-25		-22		-20		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Cycle Time	tCYC	4.0	-	4.4	-	5.0	-	ns
Clock Access Time	tCD	-	2.6	-	2.8	-	3.2	ns
Output Enable to Data Valid	tOE	-	2.6	-	2.8	-	3.2	ns
Clock High to Output Low-Z	tLZC	0.8	-	1.0	-	1.0	-	ns
Output Hold from Clock High	tOH	0.8	-	1.0	-	1.0	-	ns
Output Enable Low to Output Low-Z	tLZOE	0	-	0	-	0	-	ns
Output Enable High to Output High-Z	tHZOE	-	2.6	-	2.8	-	3.0	ns
Clock High to Output High-Z	tHZC	-	2.6	-	2.8	-	3.0	ns
Clock High Pulse Width	tCH	1.7	-	2.0	-	2.0	-	ns
Clock Low Pulse Width	tCL	1.7	-	2.0	-	2.0	-	ns
Address Setup to Clock High	tAS	1.2	-	1.4	-	1.4	-	ns
CKE Setup to Clock High	tCES	1.2	-	1.4	-	1.4	-	ns
Data Setup to Clock High	tDS	1.2	-	1.4	-	1.4	-	ns
Write Setup to Clock High ($\overline{WE}$, $\overline{BWE}$)	tWS	1.2	-	1.4	-	1.4	-	ns
Address Advance Setup to Clock High	tADVS	1.2	-	1.4	-	1.4	-	ns
Chip Select Setup to Clock High	tCSS	1.2	-	1.4	-	1.4	-	ns
Address Hold from Clock High	tAH	0.3	-	0.4	-	0.4	-	ns
CKE Hold from Clock High	tCEH	0.3	-	0.4	-	0.4	-	ns
Data Hold from Clock High	tDH	0.3	-	0.4	-	0.4	-	ns
Write Hold from Clock High ($\overline{WE}$, $\overline{BWE}$)	tWH	0.3	-	0.4	-	0.4	-	ns
Address Advance Hold from Clock High	tADVH	0.3	-	0.4	-	0.4	-	ns
Chip Select Hold from Clock High	tCSH	0.3	-	0.4	-	0.4	-	ns
ZZ High to Power Down	tpDS	2	-	2	-	2	-	cycle
ZZ Low to Power Up	tpUS	2	-	2	-	2	-	cycle

Notes :

1. All address inputs must meet the specified setup and hold times for all rising clock(CLK) edges when ADV is sampled low and $\overline{CS}$ is sampled low. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.
2. Chip selects must be valid at each rising edge of CLK(when ADV is Low) to remain enabled.
3. A write cycle is defined by $\overline{WE}$ low having been registered into the device at ADV Low, A Read cycle is defined by $\overline{WE}$ High with ADV Low. Both cases must meet setup and hold times.
4. To avoid bus contention, At a given voltage and temperature tLZC is more than tHZC.
The specs as shown do not imply bus contention because tLZC is a Min. parameter that is worst case at totally different test conditions (0°C, 2.625V) than tHZC, which is a Max. parameter(worst case at 70°C, 2.375V)
It is not possible for two SRAMs on the same board to be at such different voltage and temperature.

SLEEP MODE

SLEEP MODE is a low current, power-down mode in which the device is deselected and current is reduced to I_{SB2} . The duration of SLEEP MODE is dictated by the length of time the ZZ is in a High state.

After entering SLEEP MODE, all inputs except ZZ become disabled and all outputs go to High-Z

The ZZ pin is an asynchronous, active high input that causes the device to enter SLEEP MODE.

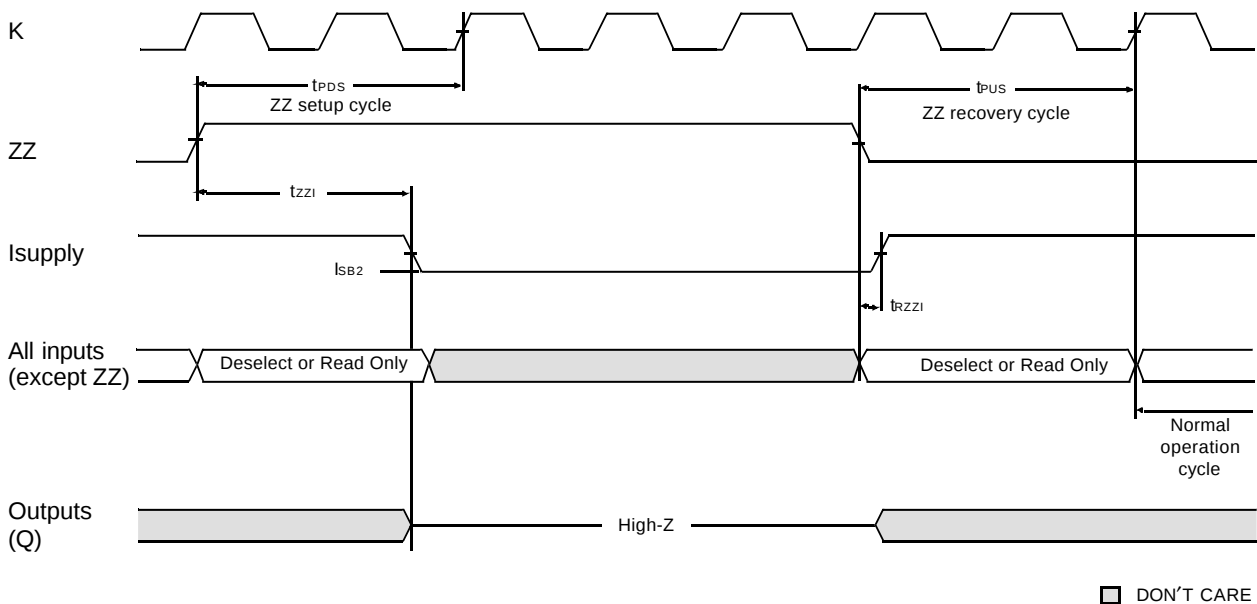
When the ZZ pin becomes a logic High, I_{SB2} is guaranteed after the time t_{ZZI} is met. Any operation pending when entering SLEEP MODE is not guaranteed to successful complete. Therefore, SLEEP MODE (READ or WRITE) must not be initiated until valid pending operations are completed. Similarly, when exiting SLEEP MODE during t_{PUS} , only a DESELECT or READ cycle should be given while the SRAM is transitioning out of SLEEP MODE.

SLEEP MODE ELECTRICAL CHARACTERISTICS

($V_{DD}, V_{DDQ} = 2.5V \pm 5\%$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS
Current during SLEEP MODE	$ZZ \geq V_{IH}$	I_{SB2}		10	mA
ZZ active to input ignored		t_{PDS}	2		cycle
ZZ inactive to input sampled		t_{PUS}	2		cycle
ZZ active to SLEEP current		t_{ZZI}		2	cycle
ZZ inactive to exit SLEEP current		t_{RZZI}	0		

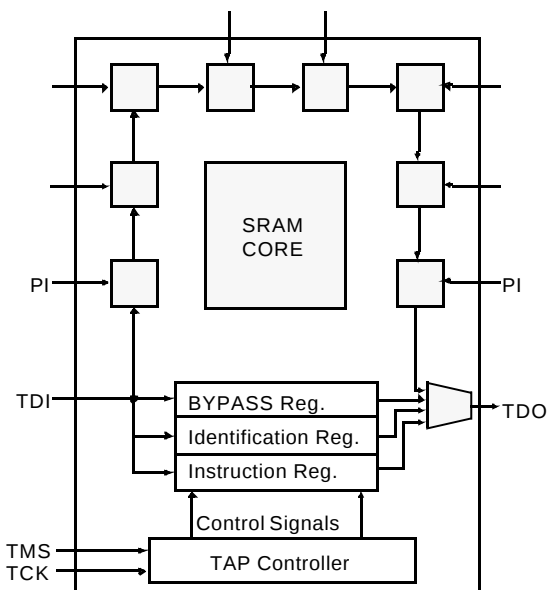
SLEEP MODE WAVEFORM



IEEE 1149.1 TEST ACCESS PORT AND BOUNDARY SCAN-JTAG

This part contains an IEEE standard 1149.1 Compatible Test Access Port (TAP). The package pads are monitored by the Serial Scan circuitry when in test mode. This is to support connectivity testing during manufacturing and system diagnostics. Internal data is not driven out of the SRAM under JTAG control. In conformance with IEEE 1149.1, the SRAM contains a TAP controller, Instruction Register, Bypass Register and ID register. The TAP controller has a standard 16-state machine that resets internally upon power-up, therefore, TRST signal is not required. It is possible to use this device without utilizing the TAP. To disable the TAP controller without interfacing with normal operation of the SRAM, TCK must be tied to Vss to preclude mid level input. TMS and TDI are designed so an undriven input will produce a response identical to the application of a logic 1, and may be left unconnected. But they may also be tied to VDD through a resistor. TDO should be left unconnected.

JTAG Block Diagram



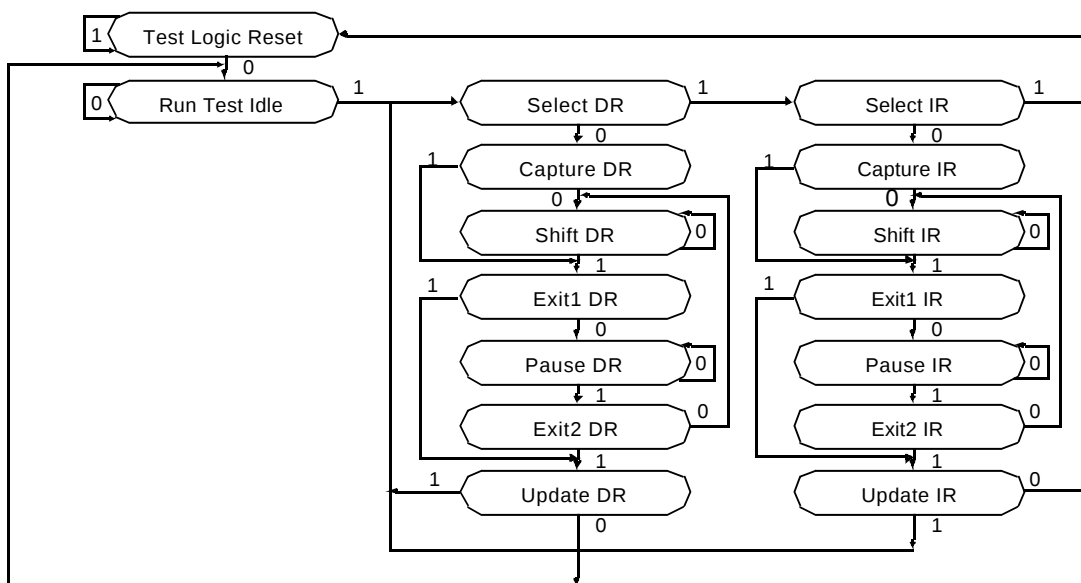
JTAG Instruction Coding

IR2	IR1	IR0	Instruction	TDO Output	Notes
0	0	0	SAMPLE-Z	Boundary Scan Register	1
0	0	1	IDCODE	Identification Register	2
0	1	0	SAMPLE-Z	Boundary Scan Register	1
0	1	1	BYPASS	Bypass Register	3
1	0	0	SAMPLE	Boundary Scan Register	4
1	0	1	BYPASS	Bypass Register	3
1	1	0	BYPASS	Bypass Register	3
1	1	1	BYPASS	Bypass Register	3

NOTE :

1. Places DQs in Hi-Z in order to sample all input data regardless of other SRAM inputs.
2. TDI is sampled as an input to the first ID register to allow for the serial shift of the external TDI data.
3. Bypass register is initiated to Vss when BYPASS instruction is invoked. The Bypass Register also holds serially loaded TDI when exiting the Shift DR states.
4. SAMPLE instruction dose not places DQs in Hi-Z.

TAP Controller State Diagram



SCAN REGISTER DEFINITION

Part	Instruction Register	Bypass Register	ID Register	Boundary Scan
256Kx36	3 bits	1 bits	32 bits	70 bits
512Kx18	3 bits	1 bits	32 bits	70 bits

ID REGISTER DEFINITION

Part	Revision Number (31:28)	Part Configuration (27:18)	Vendor Definition (17:12)	Samsung JEDEC Code (11: 1)	Start Bit(0)
256Kx36	0000	00110 00100	XXXXXX	00001001110	1
512Kx18	0000	00111 00011	XXXXXX	00001001110	1

119BGA BOUNDARY SCAN EXIT ORDER(x36)

36	4F	$\overline{OE}$		A	4G	35
37	4B	ADV		CLK	4K	34
38	4E	$\overline{CS_1}$		$\overline{CKE}$	4M	33
39	4H	$\overline{WE}$		NC	4A	32
40	3G	$\overline{BW_c}$		$\overline{BW_b}$	5G	31
41	3C	A		A	5C	30
42	3B	A		DQPb	6D	29
43	2D	DQPc		DQb	6E	28
44	1E	DQc		DQb	6G	27
45	2F	DQc		DQb	7H	26
46	1G	DQc		DQb	7D	25
47	2H	DQc		DQb	7E	24
48	1D	DQc		DQb	6F	23
49	2E	DQc		DQb	7G	22
50	2G	DQc		DQb	6H	21
51	1H	DQc		A	5B	20
52	3A	A		A	5A	19
53	2B	CS_2		$\overline{CS_2}$	6B	18
54	2C	A		A	6A	17
55	2A	A		A	6C	16
56	3R	$\overline{LBO}$		DQa	7K	15
57	2K	DQd		DQa	6L	14
58	1L	DQd		DQa	6N	13
59	2M	DQd		DQa	7P	12
60	1N	DQd		DQa	6K	11
61	1P	DQd		DQa	7L	10
62	1K	DQd		DQa	6M	9
63	2L	DQd		DQa	7N	8
64	2N	DQd		DQPa	6P	7
65	2P	DQPd		ZZ	7T	6
66	2R	A		A	6R	5
67	3T	A		$\overline{BW_a}$	5L	4
68	4N	A ₁		A	5T	3
69	2T	NC		A	4T	2
70	4P	A ₀		$\overline{BW_d}$	3L	1

119BGA BOUNDARY SCAN EXIT ORDER(x18)

36	4F	$\overline{OE}$		A	4G	35
37	4B	ADV		CLK	4K	34
38	4E	$\overline{CS_1}$		$\overline{CKE}$	4M	33
39	4H	$\overline{WE}$		NC	4A	32
40	3G	$\overline{BW_b}$		NC	5G	31
41	3C	A		A	5C	30
42	3B	A		NC	7D	29
43	2D	NC		NC	6E	28
44	1E	NC		NC	6G	27
45	2F	NC		NC	7H	26
46	1G	NC		DQa	6D	25
47	2H	NC		DQa	7E	24
48	1D	DQb		DQa	6F	23
49	2E	DQb		DQa	7G	22
50	2G	DQb		DQa	6H	21
51	1H	DQb		A	5B	20
52	3A	A		A	5A	19
53	2B	CS_2		$\overline{CS_2}$	6B	18
54	2C	A		A	6A	17
55	2A	A		A	6C	16
56	3R	$\overline{LBO}$		DQa	7K	15
57	2K	DQb		DQa	6L	14
58	1L	DQb		DQa	6N	13
59	2M	DQb		DQa	7P	12
60	1N	DQb		NC	6K	11
61	2P	DQb		NC	7L	10
62	1K	NC		NC	6M	9
63	2L	NC		NC	7N	8
64	2N	NC		NC	6P	7
65	1P	NC		ZZ	7T	6
66	2R	A		A	6R	5
67	3T	A		$\overline{BW_a}$	5L	4
68	4N	A ₁		A	5T	3
69	2T	A		A	6T	2
70	4P	A ₀		NC	3L	1

NOTE : NC ; Don't care.

JTAG DC OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Note
Power Supply Voltage	V _{DD}	2.375	2.5	2.625	V	
Input High Level	V _{IH}	1.7	-	V _{DD} +0.3	V	1
Input Low Level	V _{IL}	-0.3	-	0.7	V	
Output High Voltage	V _{OH}	2.0	-	-	V	
Output Low Voltage	V _{OL}	-	-	0.4	V	

NOTE : The input level of SRAM pin is to follow the SRAM DC specification.

1. In Case of I/O Pins, the Max. V_{IH}=V_{DDQ}+0.3V

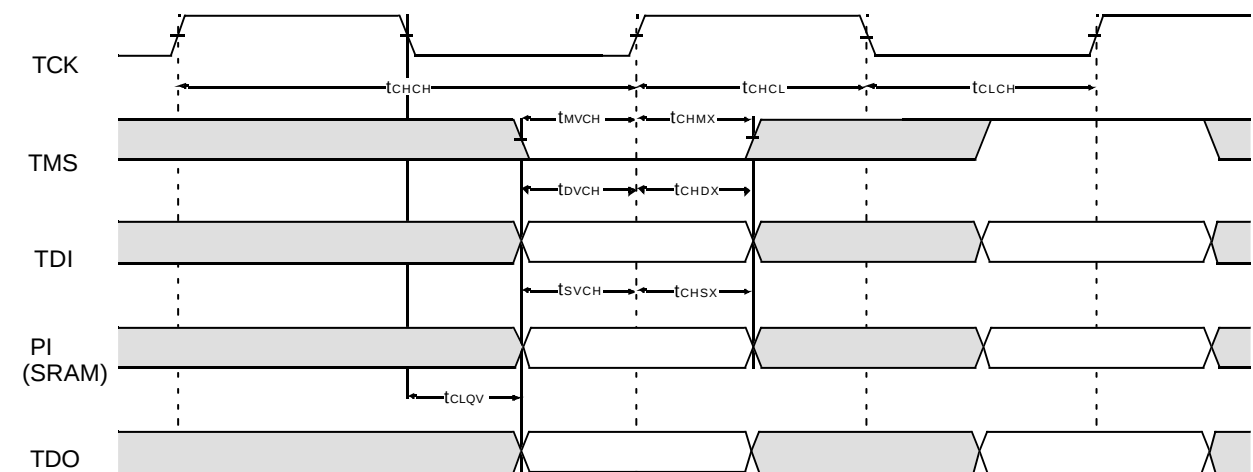
JTAG AC TEST CONDITIONS

Parameter	Symbol	Min	Unit	Note
Input High/Low Level	V _{IH} /V _{IL}	2.5 / 0	V	
Input Rise/Fall Time	TR/TF	1.0 / 1.0	ns	
Input and Output Timing Reference Level		V _{DDQ} /2	V	

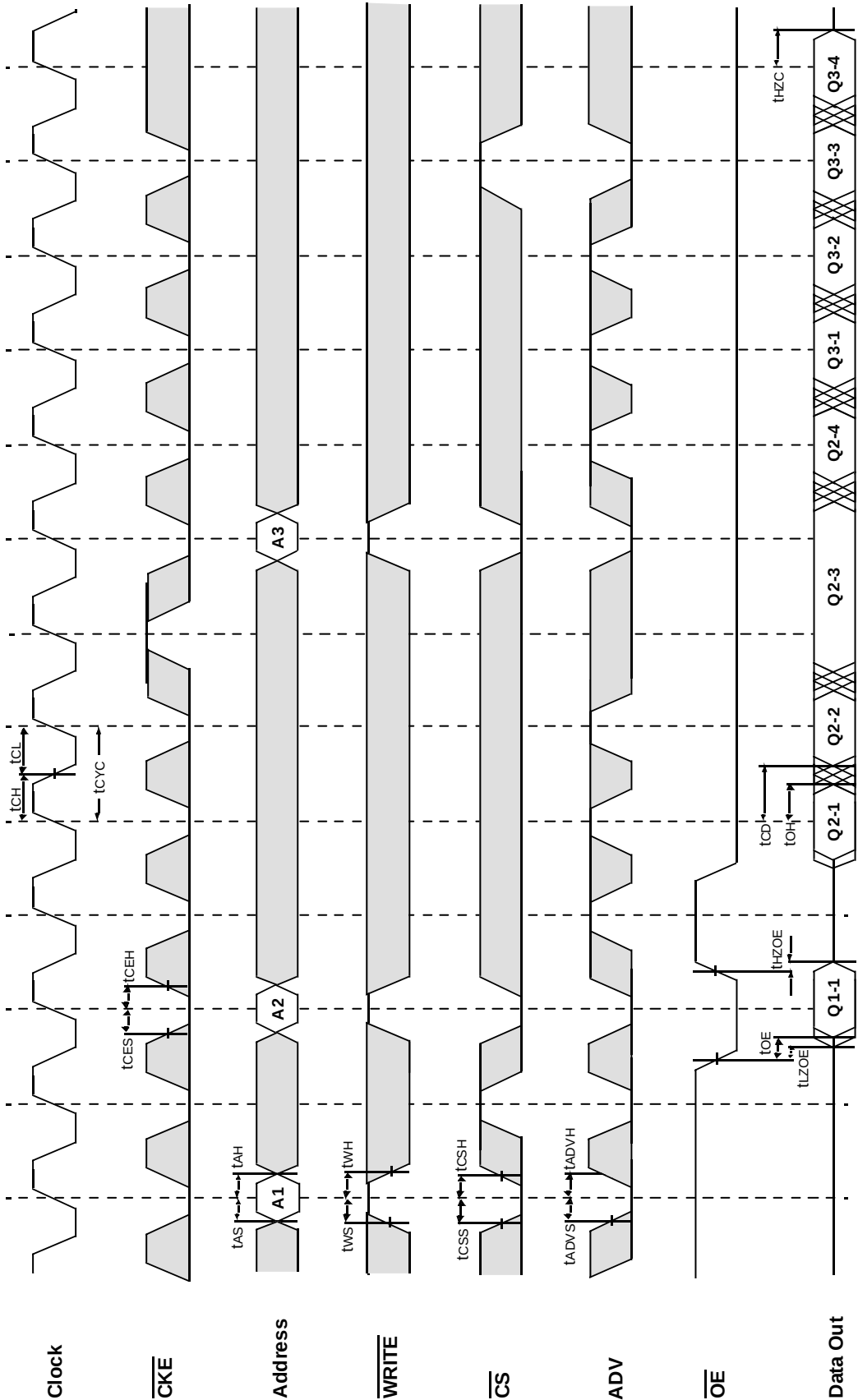
JTAG AC Characteristics

Parameter	Symbol	Min	Max	Unit	Note
TCK Cycle Time	t _{CHCH}	50	-	ns	
TCK High Pulse Width	t _{CHCL}	20	-	ns	
TCK Low Pulse Width	t _{CLCH}	20	-	ns	
TMS Input Setup Time	t _{MVCH}	5	-	ns	
TMS Input Hold Time	t _{CHMX}	5	-	ns	
TDI Input Setup Time	t _{DVCH}	5	-	ns	
TDI Input Hold Time	t _{CHDX}	5	-	ns	
SRAM Input Setup Time	t _{SVCH}	5	-	ns	
SRAM Input Hold Time	t _{CHSX}	5	-	ns	
Clock Low to Output Valid	t _{CLQV}	0	10	ns	

JTAG TIMING DIAGRAM



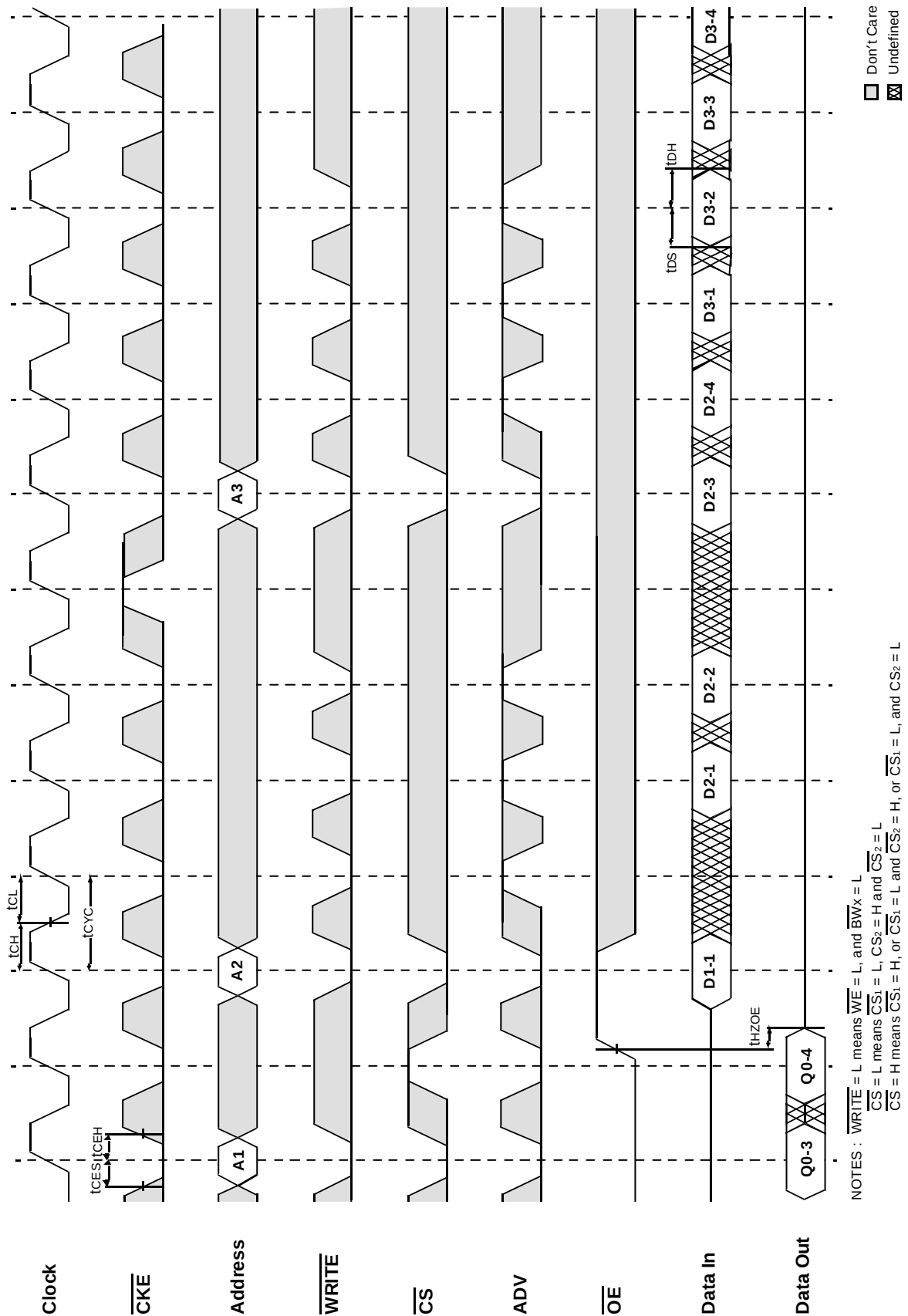
TIMING WAVEFORM OF READ CYCLE



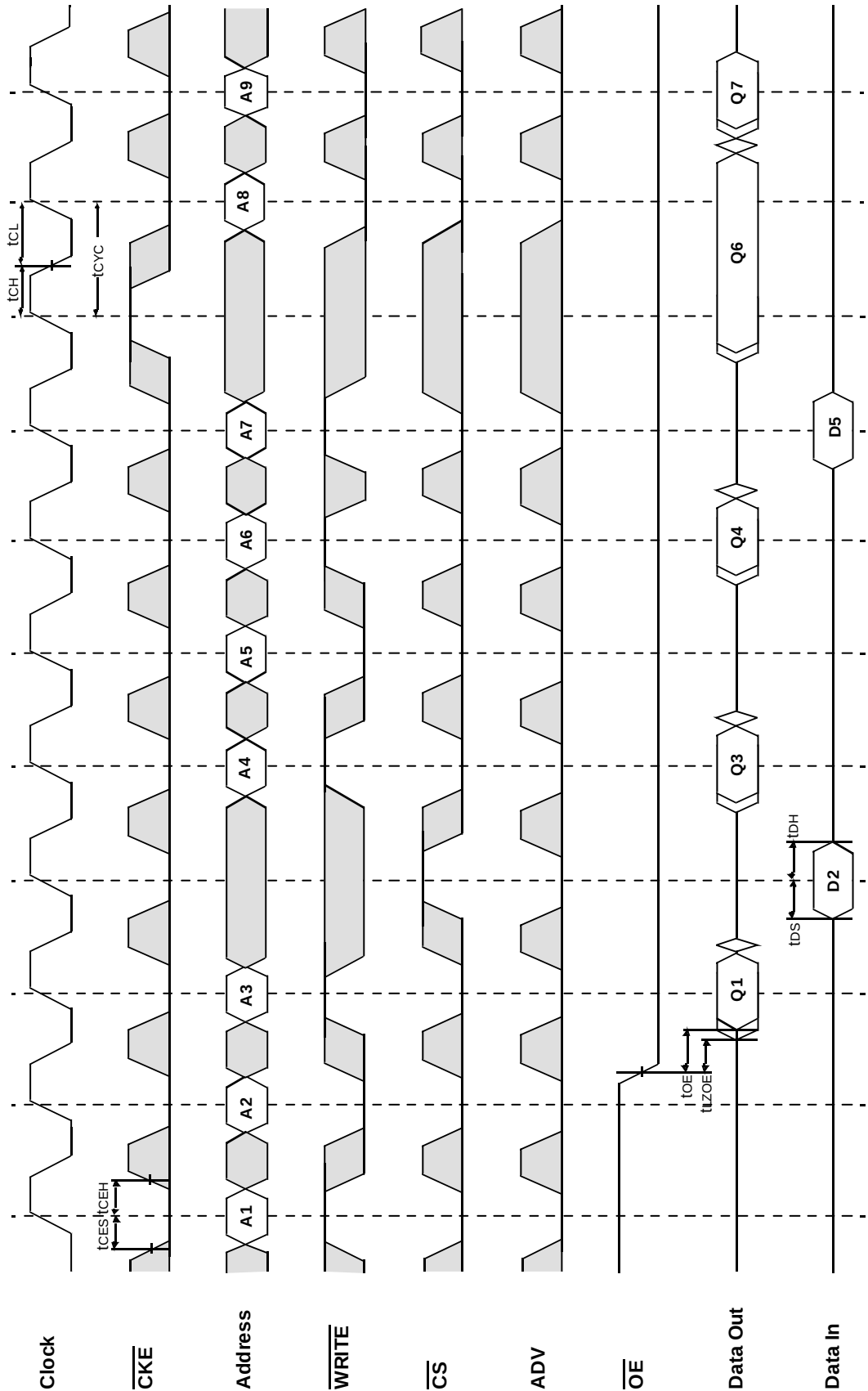
NOTES : $\overline{WRITE} = L$ means $\overline{WE} = L$, and $\overline{BWx} = L$
 $\overline{CS} = L$ means $\overline{CS_1} = L$, $\overline{CS_2} = H$ and $\overline{CS_2} = L$
 $\overline{CS} = H$ means $\overline{CS_1} = H$, or $\overline{CS_1} = L$ and $\overline{CS_2} = H$, or $\overline{CS_1} = L$, and $\overline{CS_2} = L$

□ Don't Care
⊠ Undefined

TIMING WAVEFORM OF WRTE CYCLE



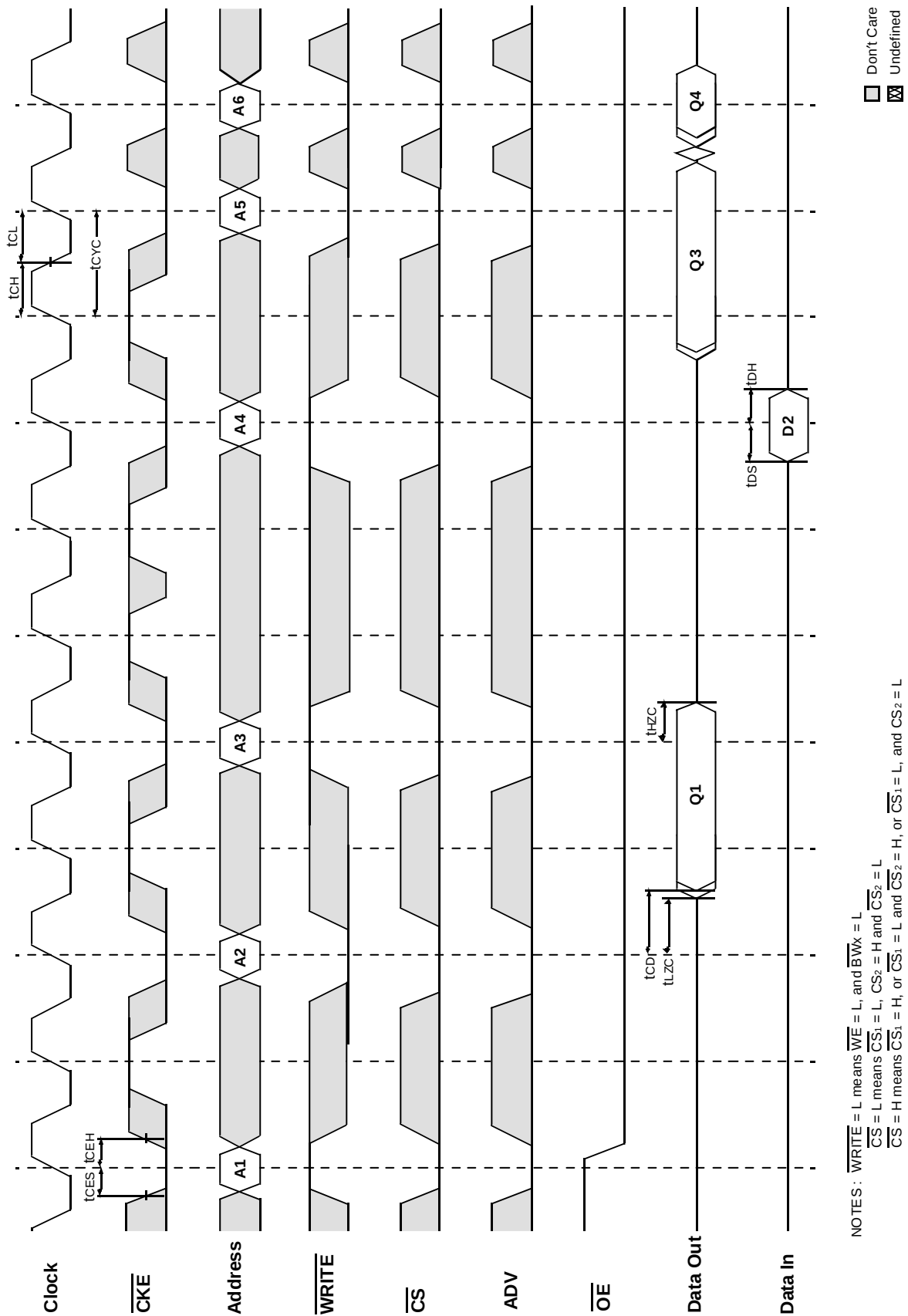
TIMING WAVEFORM OF SINGLE READ/WRITE



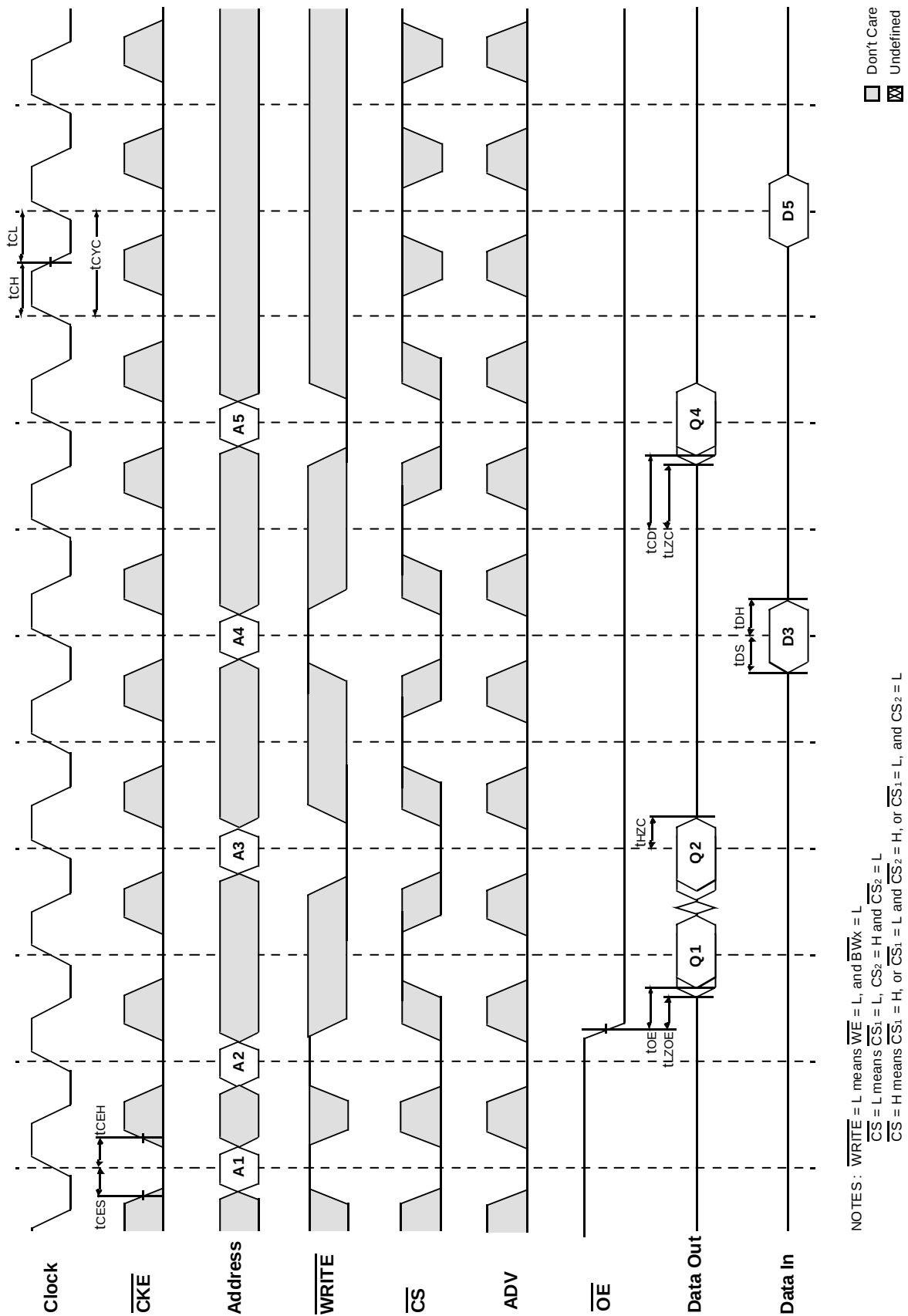
NOTES : $\overline{\text{WRITE}} = \text{L}$ means $\overline{\text{WE}} = \text{L}$, and $\overline{\text{BW}} = \text{L}$
 $\overline{\text{CS}} = \text{L}$ means $\overline{\text{CS}}_1 = \text{L}$, $\overline{\text{CS}}_2 = \text{H}$ and $\overline{\text{CS}}_2 = \text{L}$
 $\overline{\text{CS}} = \text{H}$ means $\overline{\text{CS}}_1 = \text{H}$, or $\overline{\text{CS}}_1 = \text{L}$ and $\overline{\text{CS}}_2 = \text{H}$, or $\overline{\text{CS}}_1 = \text{L}$, and $\overline{\text{CS}}_2 = \text{L}$

□ Don't Care
⊗ Undefined

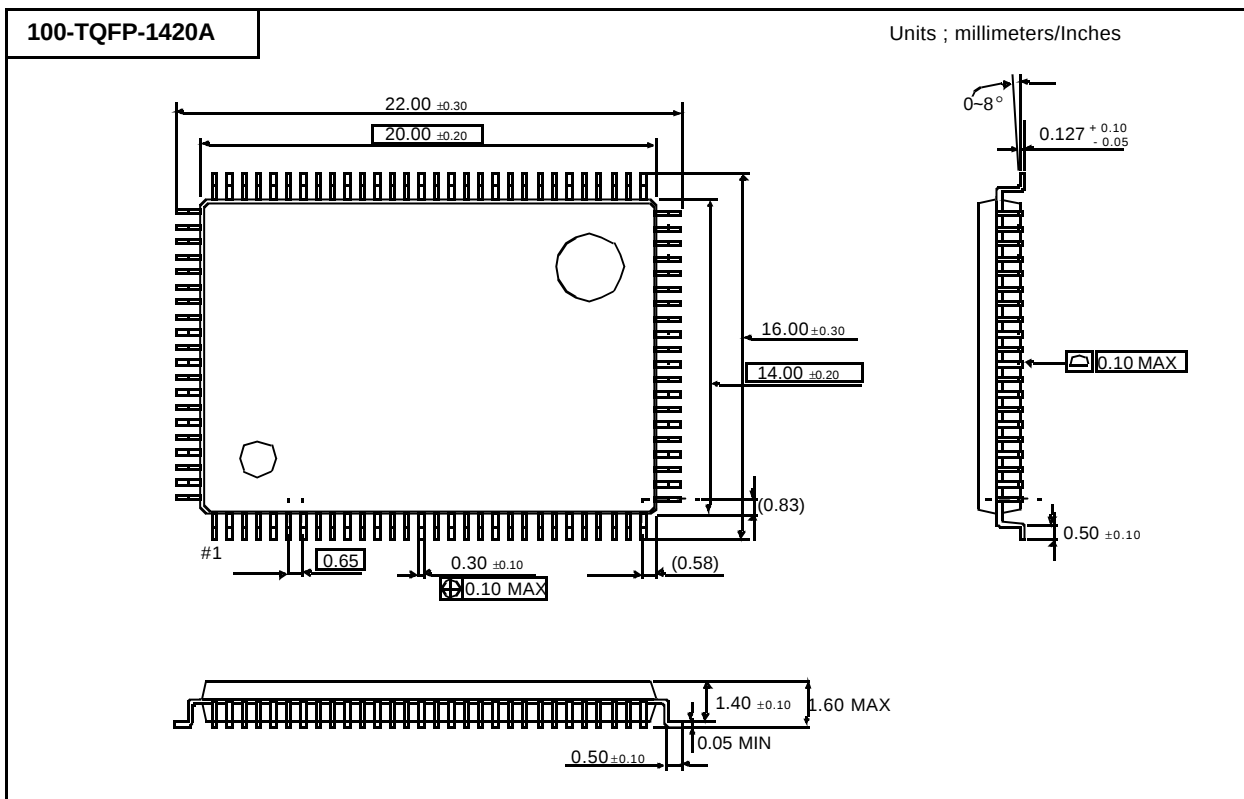
TIMING WAVEFORM OF CKE OPERATION



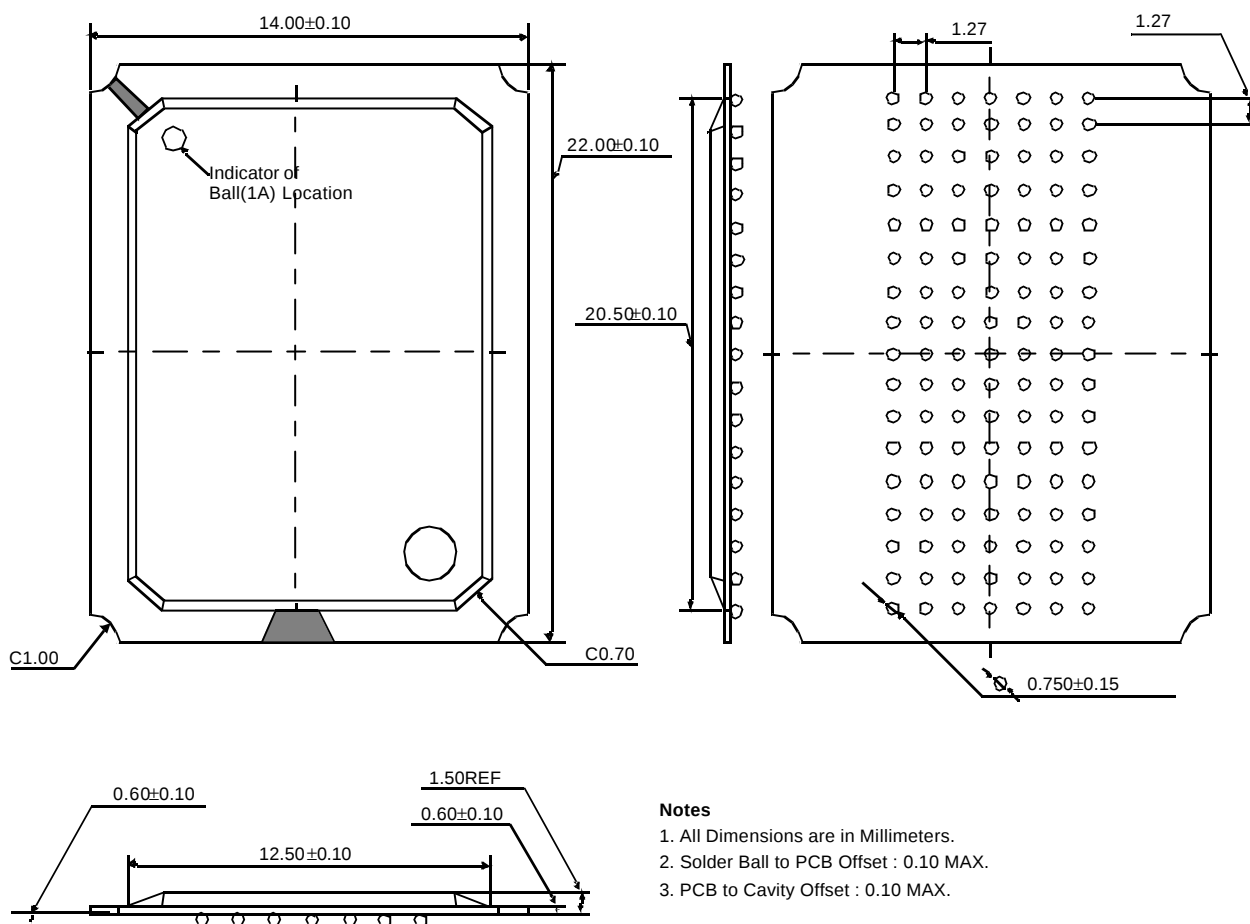
TIMING WAVEFORM OF $\overline{\text{CS}}$ OPERATION



PACKAGE DIMENSIONS



119BGA PACKAGE DIMENSIONS



Notes

1. All Dimensions are in Millimeters.
2. Solder Ball to PCB Offset : 0.10 MAX.
3. PCB to Cavity Offset : 0.10 MAX.