512Kx36 & 1Mx18-Bit Pipelined N*t*RAM™

FEATURES

- 3.3V+0.165V/-0.165V Power Supply.
- I/O Supply Voltage 3.3V+0.165V/-0.165V for 3.3V I/O or 2.5V+0.4V/-0.125V for 2.5V I/O.
- Byte Writable Function.
- Enable clock and suspend operation.
- Single READ/WRITE control pin.
- Self-Timed Write Cycle.
- Three Chip Enable for simple depth expansion with no data-contention .
- A interleaved burst or a linear burst mode.
- Asynchronous output enable control.
- Power Down mode.
- 100-TQFP-1420A /119BGA(7x17 Ball Grid Array Package).

FAST ACCESS TIMES

PARAMETER	Symbol	-25	-22	-20	Unit
Cycle Time	tCYC	4.0	4.4	5.0	ns
Clock Access Time	tCD	2.6	2.8	3.2	ns
Output Enable Access Time	tOE	2.6	2.8	3.2	ns

GENERAL DESCRIPTION

The K7N163609A and K7N161809A are 18,874,368-bits Synchronous Static SRAMs.

The N*t*RAM™, or No Turnaround Random Access Memory utilizes all the bandwidth in any combination of operating cycles. Address, data inputs, and all control signals except output enable and linear burst order are synchronized to input clock. Burst order control must be tied "High or Low".

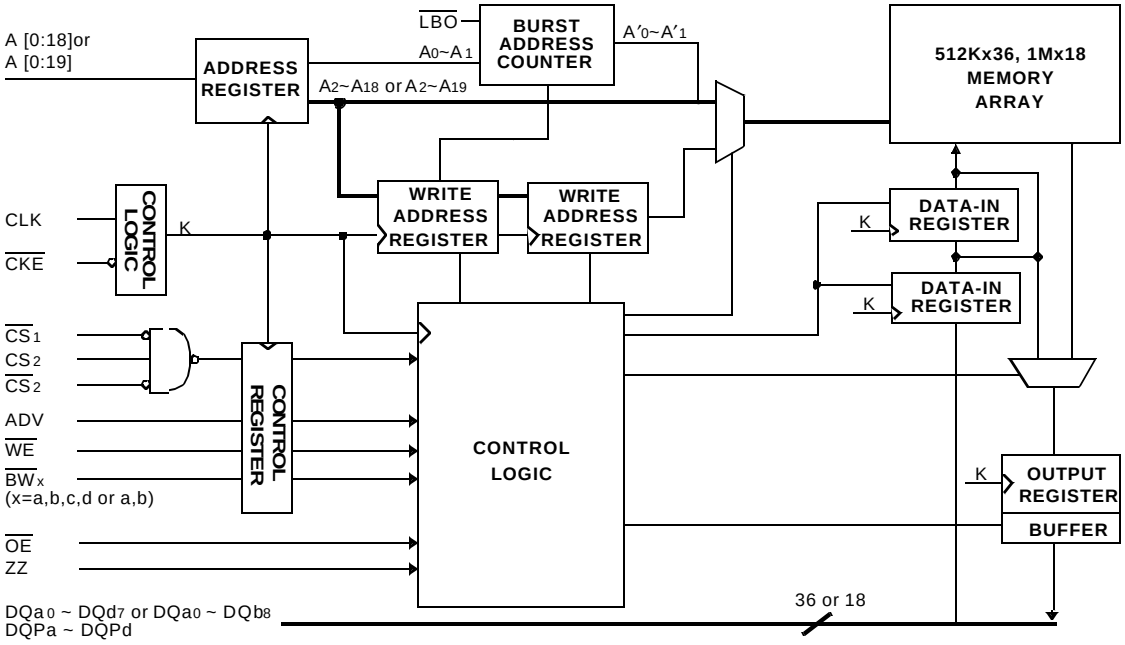
Asynchronous inputs include the sleep mode enable(ZZ). Output Enable controls the outputs at any given time.

Write cycles are internally self-timed and initiated by the rising edge of the clock input. This feature eliminates complex off-chip write pulse generation and provides increased timing flexibility for incoming signals.

For read cycles, pipelined SRAM output data is temporarily stored by an edge triggered output register and then released to the output buffers at the next rising edge of clock.

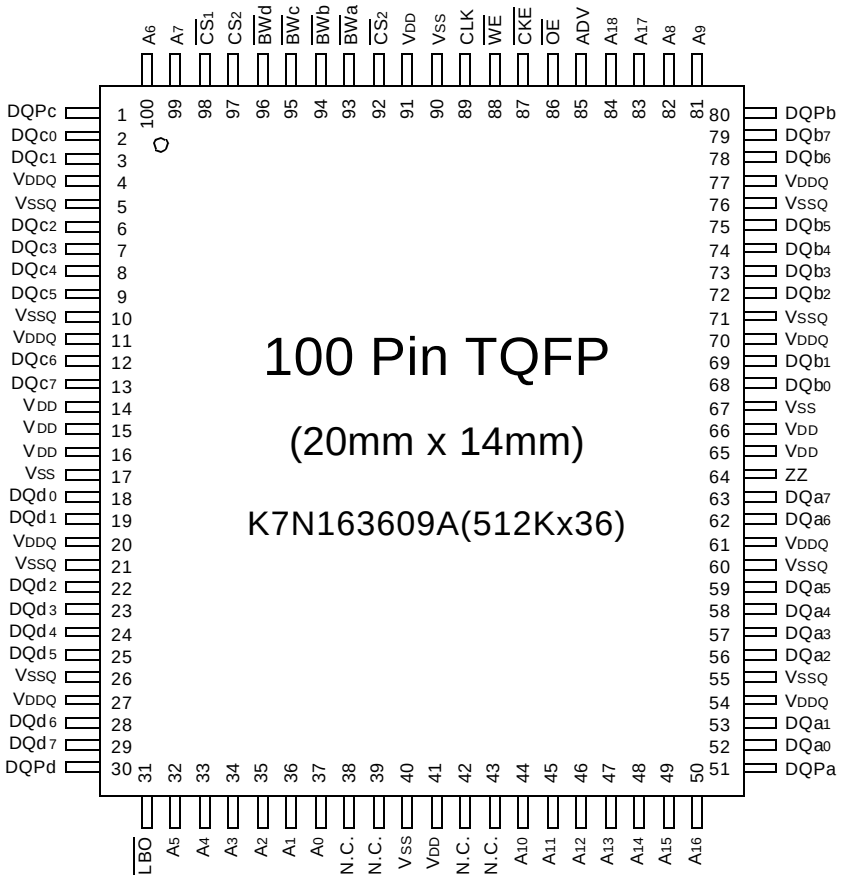
The K7N163609A and K7N161809A are implemented with SAMSUNG′s high performance CMOS technology and is available in 100pin TQFP and 119BGA packages. Multiple power and ground pins minimize ground bounce.

LOGIC BLOCK DIAGRAM



SAMSUNG ELECTRONICS

PIN CONFIGURATION (TOP VIEW)

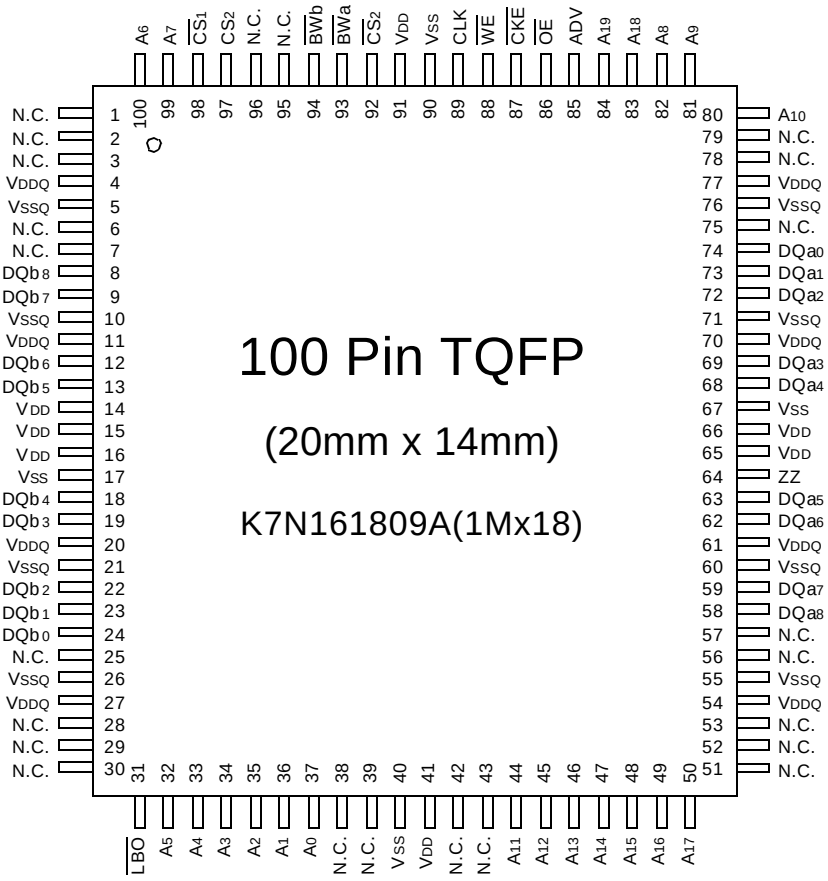


PIN NAME

SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A0 - A18	Address Inputs	32,33,34,35,36,37,44,45,46,47,48,49,50,81,82,83,84,99,100	VDD	Power Supply(+3.3V)	14,15,16,41,65,66,91
			VSS	Ground	17,40,67,90
ADV	Address Advance/Load	85	N.C.	No Connect	38,39,42,43
WE	Read/Write Control Input	88			
CLK	Clock	89	DQa0~a7	Data Inputs/Outputs	52,53,56,57,58,59,62,63
CKE	Clock Enable	87	DQb0~b7	Data Inputs/Outputs	68,69,72,73,74,75,78,79
CS1	Chip Select	98	DQc0~c7	Data Inputs/Outputs	2,3,6,7,8,9,12,13
CS2	Chip Select	97	DQd0~d7	Data Inputs/Outputs	18,19,22,23,24,25,28,29
CS2	Chip Select	92	DQPa~Pd	Data Inputs/Outputs	51,80,1,30
BWx(x=a,b,c,d)	Byte Write Inputs	93,94,95,96			
OE	Output Enable	86	VDDQ	Output Power Supply (3.3V or 2.5V)	4,11,20,27,54,61,70,77
ZZ	Power Sleep Mode	64			
LBO	Burst Mode Control	31	VSSQ	Output Ground	5,10,21,26,55,60,71,76

Note : 1. A0 and A1 are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

PIN CONFIGURATION (TOP VIEW)



PIN NAME

SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A_0 - A_{19}	Address Inputs	32,33,34,35,36,37,44,45,46,47,48,49,50,80,81,82,83,84,99,100	V_{DD}	Power Supply(+3.3V)	14,15,16,41,65,66,91
			V_{SS}	Ground	17,40,67,90
$\overline{ADV}$	Address Advance/Load	85	N.C.	No Connect	1,2,3,6,7,25,28,29,30,38,39,42,43,51,52,53,56,57,75,78,79,95,96
$\overline{WE}$	Read/Write Control Input	88			
$\overline{CLK}$	Clock	89			
$\overline{CKE}$	Clock Enable	87			
$\overline{CS_1}$	Chip Select	98	$DQa_{0\sim a8}$	Data Inputs/Outputs	58,59,62,63,68,69,72,73,74
CS_2	Chip Select	97	$DQb_{0\sim b8}$	Data Inputs/Outputs	8,9,12,13,18,19,22,23,24
$\overline{CS_2}$	Chip Select	92			
$\overline{BW}$x(x=a,b)	Byte Write Inputs	93,94			
$\overline{OE}$	Output Enable	86	V_{DDQ}	Output Power Supply (3.3V or 2.5V)	4,11,20,27,54,61,70,77
$\overline{ZZ}$	Power Sleep Mode	64			
$\overline{LBO}$	Burst Mode Control	31	V_{SSQ}	Output Ground	5,10,21,26,55,60,71,76

NOTE: A_0 and A_1 are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

119BGA PACKAGE PIN CONFIGURATIONS(TOP VIEW)

K7N163609A(512Kx36)

	1	2	3	4	5	6	7
A	V_{DDQ}	A	A	A	A	A	V_{DDQ}
B	NC	CS_2	A	ADV	A	$\overline{CS_2}$	NC
C	NC	A	A	V_{DD}	A	A	NC
D	DQc	DQPc	V_{SS}	NC	V_{SS}	DQPb	DQb
E	DQc	DQc	V_{SS}	$\overline{CS_1}$	V_{SS}	DQb	DQb
F	V_{DDQ}	DQc	V_{SS}	$\overline{OE}$	V_{SS}	DQb	V_{DDQ}
G	DQc	DQc	$\overline{BW}$c	A	$\overline{BW}$b	DQb	DQb
H	DQc	DQc	V_{SS}	$\overline{WE}$	V_{SS}	DQb	DQb
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	DQd	DQd	V_{SS}	CLK	V_{SS}	DQa	DQa
L	DQd	DQd	$\overline{BW}$d	NC	$\overline{BW}$a	DQa	DQa
M	V_{DDQ}	DQd	V_{SS}	$\overline{CKE}$	V_{SS}	DQa	V_{DDQ}
N	DQd	DQd	V_{SS}	A_1*	V_{SS}	DQa	DQa
P	DQd	DQPd	V_{SS}	A_0*	V_{SS}	DQPa	DQa
R	NC	A	$\overline{LBO}$	V_{DD}	NC	A	NC
T	NC	NC	A	A	A	NC	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

Note : * A_0 and A_1 are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

PIN NAME

SYMBOL	PIN NAME	SYMBOL	PIN NAME
A	Address Inputs	V_{DD}	Power Supply
		V_{SS}	Ground
A_0,A_1	Burst Address Inputs		
ADV	Address Advance/Load	N.C.	No Connect
$\overline{WE}$	Read/Write Control Input		
CLK	Clock	DQa	Data Inputs/Outputs
$\overline{CKE}$	Clock Enable	DQb	Data Inputs/Outputs
$\overline{CS_1}$	Chip Select	DQc	Data Inputs/Outputs
CS_2	Chip Select	DQd	Data Inputs/Outputs
$\overline{CS_2}$	Chip Select	DQPa~Pd	Data Inputs/Outputs
$\overline{BW}$x	Byte Write Inputs		
(x=a,b,c,d)		V_{DDQ}	Output Power Supply
$\overline{OE}$	Output Enable		
ZZ	Power Sleep Mode		
$\overline{LBO}$	Burst Mode Control		
TCK	JTAG Test Clock		
TMS	JTAG Test Mode Select		
TDI	JTAG Test Data Input		
TDO	JTAG Test Data Output		

119BGA PACKAGE PIN CONFIGURATIONS(TOP VIEW)

K7N161809A(1Mx18)

	1	2	3	4	5	6	7
A	V_{DDQ}	A	A	A	A	A	V_{DDQ}
B	NC	CS_2	A	ADV	A	$\overline{CS_2}$	NC
C	NC	A	A	V_{DD}	A	A	NC
D	DQb	NC	V_{SS}	NC	V_{SS}	DQPa	NC
E	NC	DQb	V_{SS}	$\overline{CS_1}$	V_{SS}	NC	DQa
F	V_{DDQ}	NC	V_{SS}	$\overline{OE}$	V_{SS}	DQa	V_{DDQ}
G	NC	DQb	$\overline{BW}$b	A	V_{SS}	NC	DQa
H	DQb	NC	V_{SS}	$\overline{WE}$	V_{SS}	DQa	NC
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	NC	DQb	V_{SS}	CLK	V_{SS}	NC	DQa
L	DQb	NC	V_{SS}	NC	$\overline{BW}$a	DQa	NC
M	V_{DDQ}	DQb	V_{SS}	$\overline{CKE}$	V_{SS}	NC	V_{DDQ}
N	DQb	NC	V_{SS}	A_1*	V_{SS}	DQa	NC
P	NC	DQPb	V_{SS}	A_0*	V_{SS}	NC	DQa
R	NC	A	$\overline{LBO}$	V_{DD}	NC	A	NC
T	NC	A	A	NC	A	A	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

Note : * A_0 and A_1 are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

PIN NAME

SYMBOL	PIN NAME	SYMBOL	PIN NAME
A	Address Inputs	V_{DD}	Power Supply
		V_{SS}	Ground
A_0,A_1	Burst Address Inputs		
ADV	Address Advance/Load	N.C.	No Connect
$\overline{WE}$	Read/Write Control Input		
CLK	Clock		
$\overline{CKE}$	Clock Enable	DQa	Data Inputs/Outputs
$\overline{CS_1}$	Chip Select	DQb	Data Inputs/Outputs
CS_2	Chip Select	DQPa, Pb	Data Inputs/Outputs
$\overline{CS_2}$	Chip Select		
$\overline{BW}$x (x=a,b)	Byte Write Inputs	V_{DDQ}	Output Power Supply
$\overline{OE}$	Output Enable		
ZZ	Power Sleep Mode		
$\overline{LBO}$	Burst Mode Control		
TCK	JTAG Test Clock		
TMS	JTAG Test Mode Select		
TDI	JTAG Test Data Input		
TDO	JTAG Test Data Output		