

Document Title**128Kx8 bit Super Low Power and Low Voltage CMOS Static RAM****Revision History**

<u>Revision No.</u>	<u>History</u>	<u>Draft Data</u>	<u>Remark</u>
0.0	Design target	November 3, 1998	Advance
0.1	Revise	January 9, 1999	Preliminary
1.0	Finalize - Change V _{DR} : 1.0 to 1.5V - Change I _{DR} test condition : V _{CC} =1.2 to 1.5V	February 25, 1999	Final

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128Kx8 bit Super Low Power and Low Voltage CMOS Static RAM

FEATURES

- Process Technology: Full CMOS
- Organization: 128K x8 bit
- Power Supply Voltage: 2.7~3.3V
- Low Data Retention Voltage: 1.5V(Min)
- Three state output status and TTL Compatible
- Package Type: 32-TSOP1-0813.4F
48-FBGA-6.00x7.00

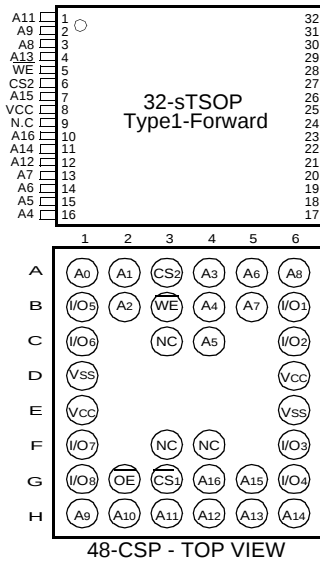
GENERAL DESCRIPTION

The KM68FU1000A families are fabricated by SAMSUNG's advanced full CMOS process technology. The families support industrial temperature range and have various package types for user flexibility of system design. The families also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

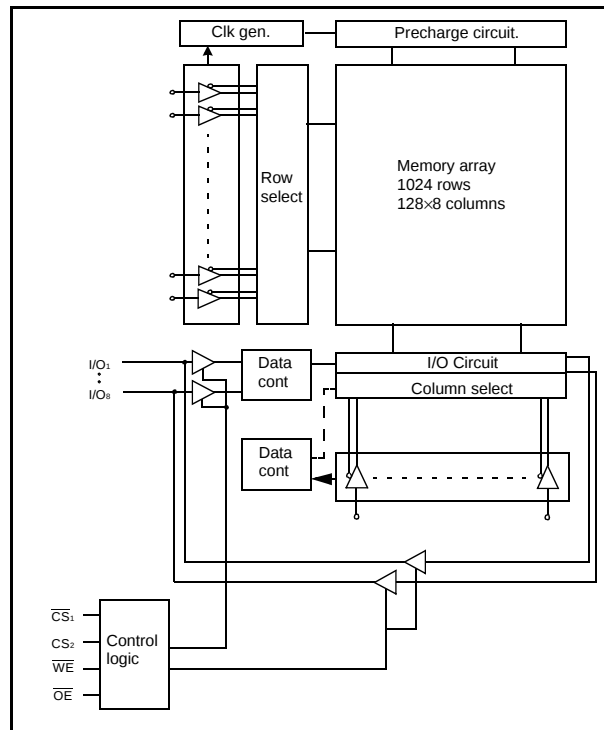
Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation		PKG Type
				Standby (Isb1, Typ.)	Operating (Icc1, Max)	
KM68FU1000A	Industrial(-40~85°C)	2.7~3.3V	70/100ns	0.5μA	4mA	32-sTSOP1-F 48-FBGA

PIN DESCRIPTION



Name	Function	Name	Function
CS ₁ , CS ₂	Chip Select Inputs	I/O ₁ ~I/O ₈	Data Inputs/Outputs
OE	Output Enable Input	Vcc	Power
WE	Write Enable Input	Vss	Ground
A ₀ ~A ₁₆	Address Inputs	N.C.	No Connection

FUNCTIONAL BLOCK DIAGRAM



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PRODUCT LIST

Industrial Temperature Products(-40~85°C)	
Part Name	Function
KM68FU1000ATGI-7 KM68FU1000ATGI-10	32-sTSOP1 F, 70ns, 3.0V 32-sTSOP1 F, 100ns, 3.0V
KM68FU1000AFI-7 KM68FU1000AFI-10	48-FBGA with 48 ball, 70ns, 3.0V 48-FBGA with 48 ball, 100ns, 3.0V

FUNCTIONAL DESCRIPTION

$\overline{CS}_1$	CS_2	$\overline{OE}$	$\overline{WE}$	I/O	Mode	Power
H	X ¹⁾	X ¹⁾	X ¹⁾	High-Z	Deselected	Standby
X ¹⁾	L	X ¹⁾	X ¹⁾	High-Z	Deselected	Standby
L	H	H	H	High-Z	Output Disabled	Active
L	H	L	H	Dout	Read	Active
L	H	X ¹⁾	L	Din	Write	Active

1. X means don't care (Must be high or low states)

ABSOLUTE MAXIMUM RATINGS¹⁾

Item	Symbol	Ratings	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-0.2 to 3.6V	V
Voltage on Vcc supply relative to Vss	V _{CC}	-0.2 to 4.0V	V
Power Dissipation	P _D	1.0	W
Storage temperature	T _{STG}	-55 to 150	°C
Operating Temperature	T _A	-40 to 85	°C

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS¹⁾

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V _{CC}	2.7	3.0	3.3	V
Ground	V _{SS}	0	0	0	V
Input high voltage	V _{IH}	2.2	-	V _{CC} +0.2 ²⁾	V
Input low voltage	V _{IL}	-0.2 ³⁾	-	0.4	V

Note :

1. T_A=-40 to 85°C, otherwise specified
2. Overshoot: V_{CC}+2.0V in case of pulse width ≤20ns.
3. Undershoot: -2.0V in case of pulse width ≤20ns.
4. Overshoot and undershoot are sampled, not 100% tested.

CAPACITANCE¹⁾ (f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C _{IN}	V _{IN} =0V	-	8	pF
Input/Output capacitance	C _{IO}	V _{IO} =0V	-	10	pF

1. Capacitance is sampled, not 100% tested

DC AND OPERATING CHARACTERISTICS

Item	Symbol	Test Conditions	Min	Typ	Max	Unit
Input leakage current	I _{LI}	V _{IN} =V _{SS} to V _{CC}	-1	-	1	μA
Output leakage current	I _{LO}	$\overline{CS_1}$ =V _{IH} or CS ₂ =V _{IL} or $\overline{OE}$ =V _{IH} or $\overline{WE}$ =V _{IL} , V _{IO} =V _{SS} to V _{CC}	-1	-	1	μA
Operating power supply current	I _{CC}	I _{IO} =0mA, $\overline{CS_1}$ =V _{IL} , CS ₂ =V _{IH} , V _{IN} =V _{IH} or V _{IL}	-	-	2	mA
Average operating current	I _{CC1}	Cycle time=1μs, 100%duty, I _{IO} =0mA, $\overline{CS_1}$ ≤0.2V, CS ₂ ≥V _{CC} -0.2V, V _{IN} ≤0.2V	-	-	4	mA
	I _{CC2}	Cycle time=Min, 100% duty, I _{IO} =0mA, $\overline{CS_1}$ =V _{IL} , CS ₂ =V _{IH} , V _{IN} =V _{IH} or V _{IL}	-	-	25	mA
Output low voltage	V _{OL}	I _{OL} =2.1mA	-	-	0.4	V
Output high voltage	V _{OH}	I _{OH} =-1.0mA	2.4	-	-	V
Standby Current(TTL)	I _{SB}	$\overline{CS_1}$ =V _{IH} , CS ₂ =V _{IL} , Other inputs=V _{IH} or V _{IL}	-	-	0.3	mA
Standby Current(CMOS)	I _{SB1}	$\overline{CS_1}$ ≥V _{CC} -0.2V, CS ₂ ≥V _{CC} -0.2V or CS ₂ ≤0.2V, Other inputs=0~V _{CC}	-	0.5	5 ¹⁾	μA

1. Super low power product=1μA with special handling.

AC OPERATING CONDITIONS

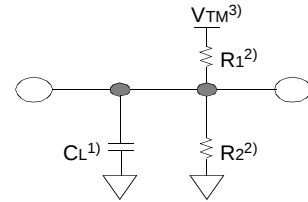
TEST CONDITIONS (Test Load and Test Input/Output Reference)

Input pulse level: 0.2 to 2.2V

Input rising and falling time: 5ns

Input and output reference voltage: 1.5V

Output load (See right): $C_L = 100\text{pF} + 1\text{TTL}$



1. Including scope and jig capacitance

2. $R_1 = 3070\Omega$, $R_2 = 3150\Omega$

3. $V_{TM} = 2.8\text{V}$

AC CHARACTERISTICS ($V_{CC} = 2.7 \sim 3.3\text{V}$, $T_A = -40$ to 85°C)

Parameter List		Symbol	Speed Bins				Units
			70ns		100ns		
			Min	Max	Min	Max	
Read	Read cycle time	t _{RC}	70	-	100	-	ns
	Address access time	t _{AA}	-	70	-	100	ns
	Chip select to output	t _{CO1} , t _{CO2}	-	70	-	100	ns
	Output enable to valid output	t _{OE}	-	35	-	50	ns
	Chip select to low-Z output	t _{LZ}	10	-	10	-	ns
	Output enable to low-Z output	t _{OLZ}	5	-	5	-	ns
	Chip disable to high-Z output	t _{HZ}	0	25	0	30	ns
	Output disable to high-Z output	t _{OHZ}	0	25	0	30	ns
	Output hold from address change	t _{OH}	10	-	15	-	ns
Write	Write cycle time	t _{WC}	70	-	100	-	ns
	Chip select to end of write	t _{CW}	60	-	80	-	ns
	Address set-up time	t _{AS}	0	-	0	-	ns
	Address valid to end of write	t _{AW}	60	-	80	-	ns
	Write pulse width	t _{WP}	55	-	70	-	ns
	Write recovery time	t _{WR}	0	-	0	-	ns
	Write to output high-Z	t _{WHZ}	0	25	0	30	ns
	Data to write time overlap	t _{DW}	30	-	40	-	ns
	Data hold from write time	t _{DH}	0	-	0	-	ns
	End write to output low-Z	t _{OW}	5	-	5	-	ns

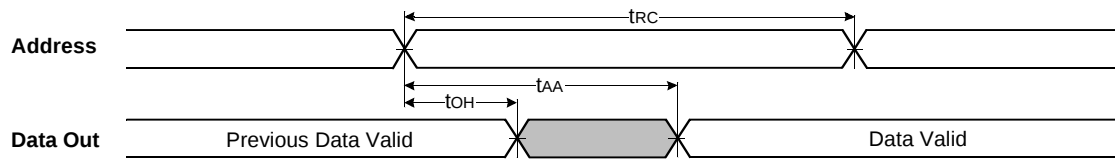
DATA RETENTION CHARACTERISTICS

Item	Symbol	Test Condition	Min	Typ	Max	Unit
V_{CC} for data retention	V_{DR}	$\overline{CS}_1 \geq V_{CC} - 0.2\text{V}^{(1)}$	1.5	-	3.3	V
Data retention current	I_{DR}	$V_{CC} = 1.5\text{V}$, $\overline{CS}_1 \geq V_{CC} - 0.2\text{V}^{(1)}$	-	-	1	μA
Data retention set-up time	t_{SDR}	See data retention waveform	0	-	-	ms
Recovery time	t_{RDR}		t_{RC}	-	-	

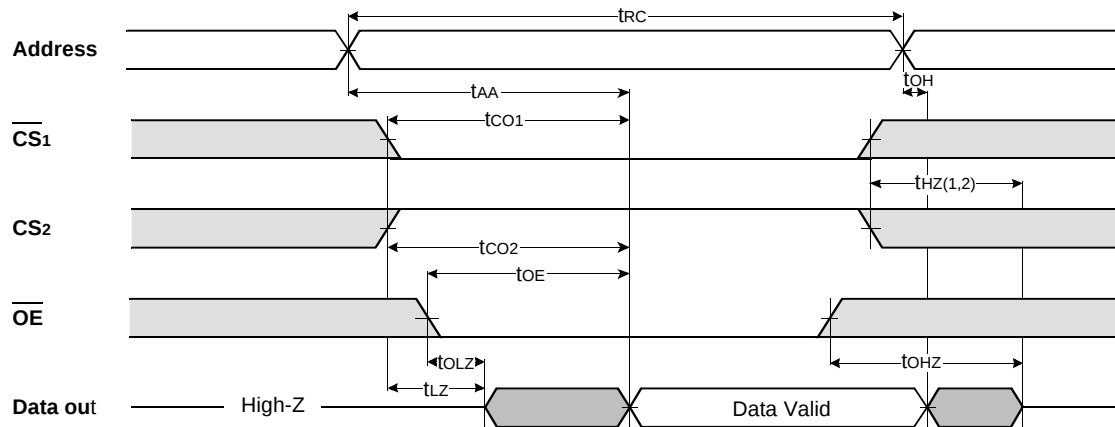
1. $\overline{CS}_1 \geq V_{CC} - 0.2\text{V}$, $\overline{CS}_2 \geq V_{CC} - 0.2\text{V}$ ($\overline{CS}_1$ controlled) or $\overline{CS}_2 \leq 0.2\text{V}$ ($\overline{CS}_2$ controlled)

TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{CS1}=\overline{OE}=V_{IL}$, $CS2=\overline{WE}=V_{IH}$)



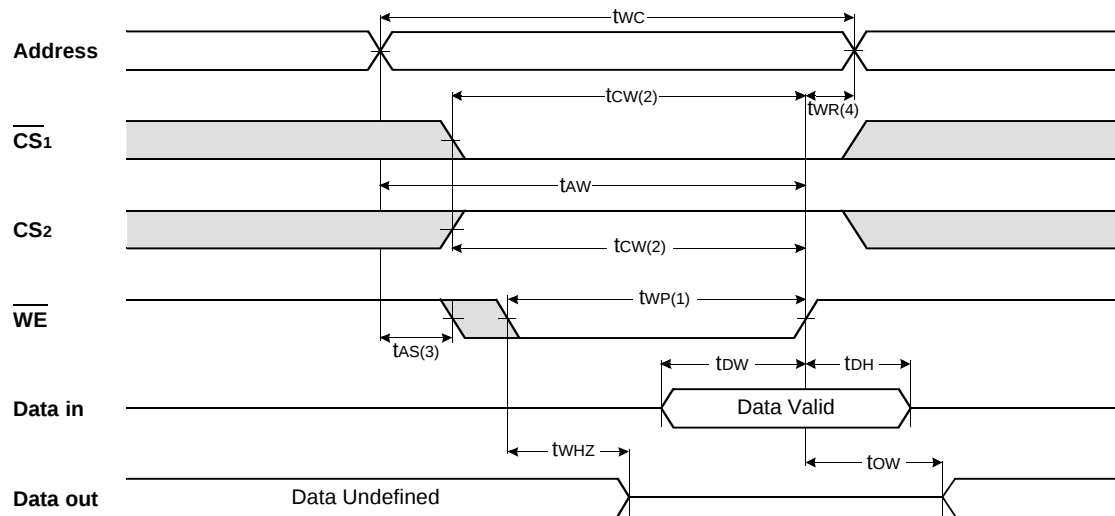
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}=V_{IH}$)



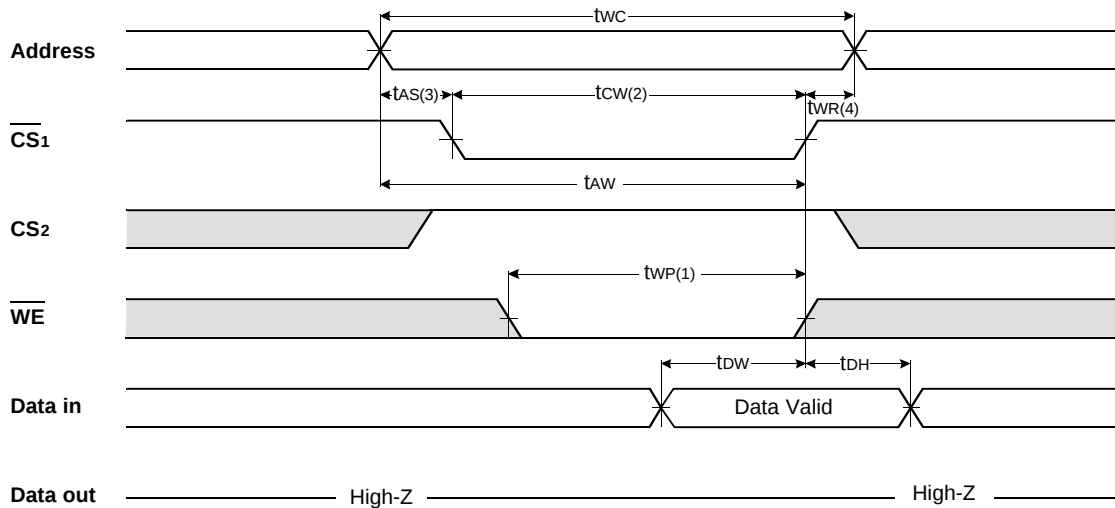
NOTES (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, $t_{HZ}(\text{Max.})$ is less than $t_{LZ}(\text{Min.})$ both for a given device and from device to device interconnection.

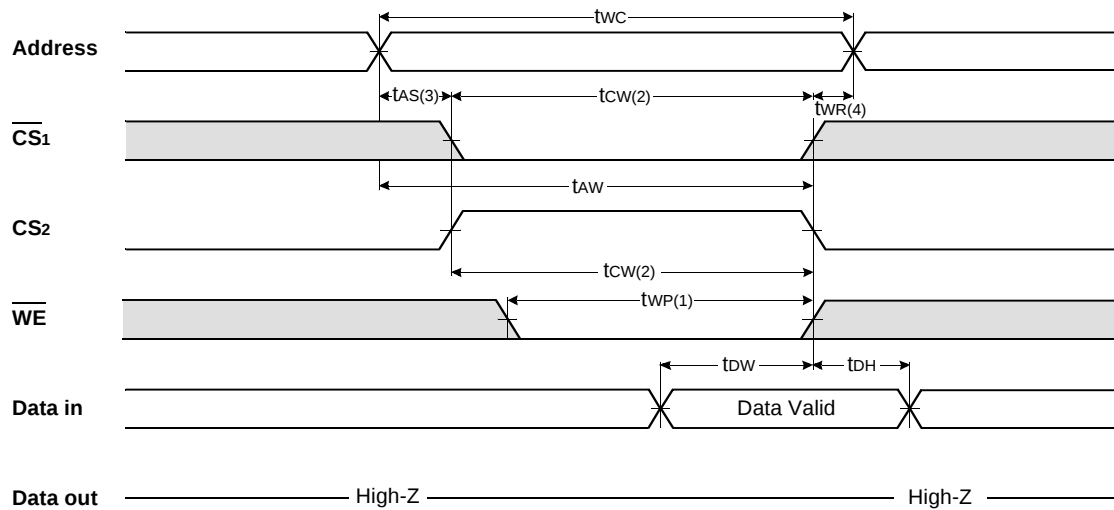
TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{\text{WE}}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{\text{CS1}}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(3) (CS₂ Controlled)

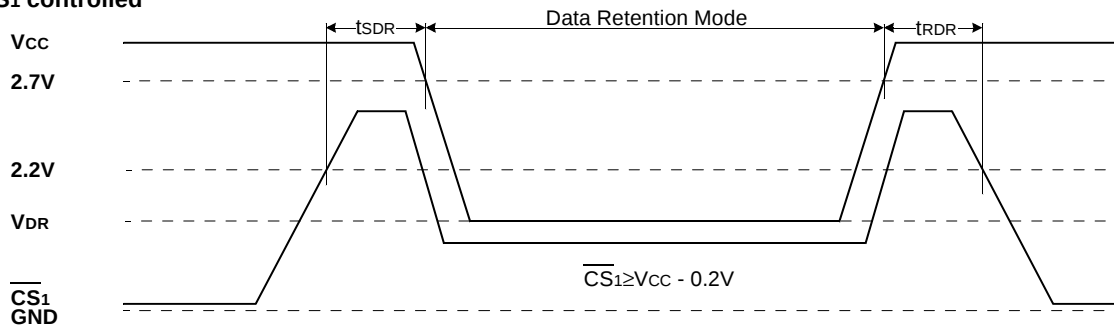


NOTES (WRITE CYCLE)

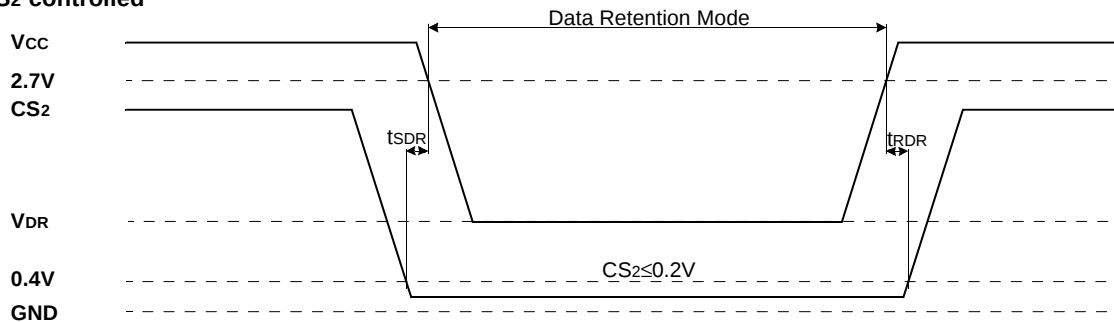
1. A write occurs during the overlap of a low $\overline{CS_1}$, a high CS₂ and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS_1}$ goes low, CS₂ going high and WE going low : A write ends at the earliest transition among CS₁ going high, CS₂ going low and WE going high, tWP is measured from the beginning of write to the end of write.
2. tCW is measured from the CS₁ going low or CS₂ going high to the end of write.
3. tAS is measured from the address valid to the beginning of write.
4. tWR is measured from the end of write to the address change. tWR1 applied in case a write ends as $\overline{CS_1}$ or $\overline{WE}$ going high tWR2 applied in case a write ends as CS₂ going to low.

DATA RETENTION WAVE FORM

CS₁ controlled



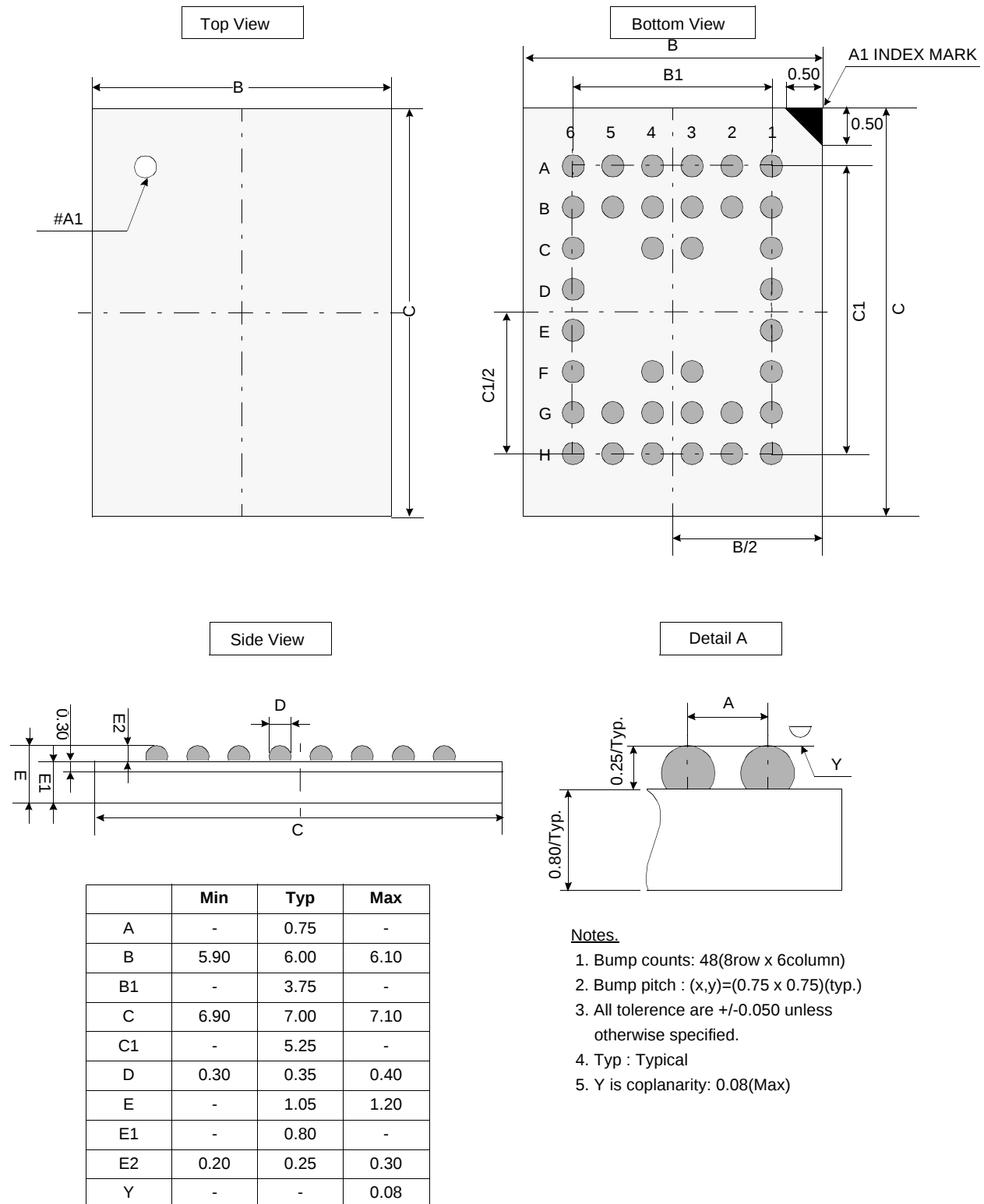
CS₂ controlled



PACKAGE OUTLINE

Units: millimeters

48 BALL FINE PITCH BGA(0.75mm ball pitch)



Notes.

1. Bump counts: 48(8row x 6column)
2. Bump pitch : (x,y)=(0.75 x 0.75)(typ.)
3. All tolerance are +/-0.050 unless otherwise specified.
4. Typ : Typical
5. Y is coplanarity: 0.08(Max)

PACKAGE DIMENSIONS

Units: millimeters(inches)

32 PIN THIN SMALL OUTLINE PACKAGE TYPE I (0813.4F)

