

Document Title

256Kx16 bit Super Low Power and Low Voltage Full CMOS Static RAM

Revision History

<u>Revision No.</u>	<u>History</u>	<u>Draft Date</u>	<u>Remark</u>
0.0	Initial Draft	April 8, 1998	Advance
0.1	Revise - DC characteristics change Icc1: 3mA → 4mA Icc2: 30mA → 35mA ISB1: 15/1μA(LL/SL) → 10/5μA(LL/SL) IDR: 3/1μA(LL/SL, Vcc=1.5V) → 3/2μA(LL/SL, Vcc=1.2V) - 48-CSP package dimension change Die thickness: 0.32mm → 0.45mm E: 0.80mm → 0.93mm E1: 0.55mm → 0.68mm	July 15, 1998	Preliminary
0.11	Errata correction	August 17, 1998	
1.0	Finalize	January 7, 1999	Final
2.0	Revise - Change VDR 1.0V to 1.5V - Change IDR test condition ; Vcc=1.2V to 1.5V	May 13, 1999	Final

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256K x 16 bit Super Low Power and Low Voltage Full CMOS Static RAM

FEATURES

- Process Technology: Full CMOS
- Organization: 256K x16 bit
- Power Supply Voltage: 2.4~2.6V
- Low Data Retention Voltage: 1.5V(Min)
- Three state output status and TTL Compatible
- Package Type: 48-μBGA-8.20x8.70

GENERAL DESCRIPTION

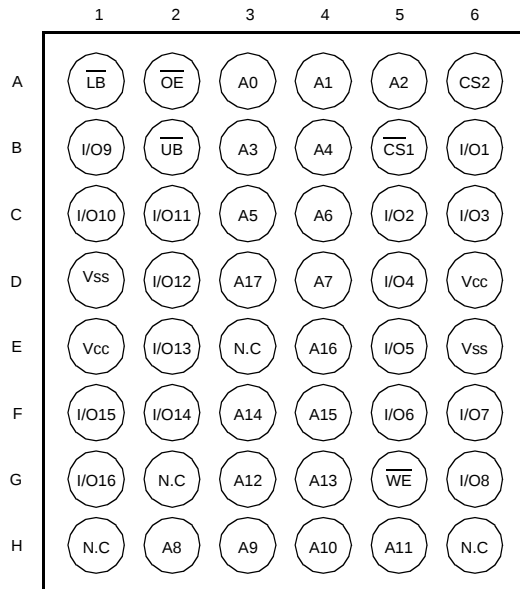
The KM616FS4110 families are fabricated by SAMSUNG's advanced full CMOS process technology. The families support industrial temperature range and 48 ball Chip Scale Package for user flexibility of system design. The family also supports low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation		PKG Type
				Standby (Isb1, Typ.)	Operating (Icc1, Max)	
KM616FS4110	Industrial(-40~85°C)	2.4~2.6V	70 ¹⁾ /100ns	0.5μA	4mA	48-μBGA

1. The parameter is measured with 30pF test load.

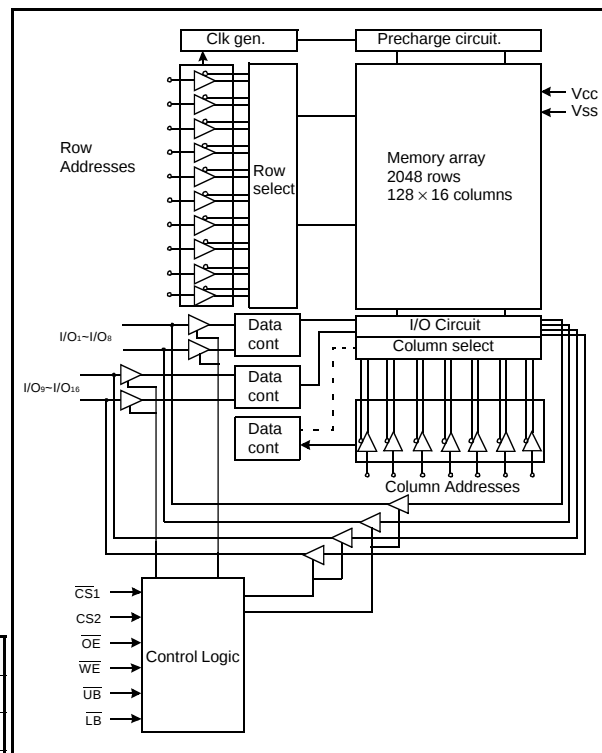
PIN DESCRIPTION



48-ball CSP - Top View (Ball Down)

Name	Function	Name	Function
CS1, CS2	Chip Select Inputs	Vcc	Power
OE	Output Enable Input	Vss	Ground
WE	Write Enable Input	UB	Upper Byte(I/O9~16)
A0~A17	Address Inputs	LB	Lower Byte(I/O1~8)
I/O1~I/O16	Data Inputs/Outputs	N.C.	No Connection

FUNCTIONAL BLOCK DIAGRAM



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PRODUCT LIST

Industrial Temperature Products(-40~85°C)	
Part Name	Function
KM616FS4110ZI-7 KM616FS4110ZI-10	48-μBGA with 48 ball, 70ns, 2.5V 48-μBGA with 48 ball, 100ns, 2.5V

FUNCTIONAL DESCRIPTION

$\overline{CS}_1$	CS_2	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	I/O1-8	I/O9-16	Mode	Power
H	X ¹⁾	X ¹⁾	X ¹⁾	X ¹⁾	X ¹⁾	High-Z	High-Z	Deselected	Standby
X ¹⁾	L	X ¹⁾	X ¹⁾	X ¹⁾	X ¹⁾	High-Z	High-Z	Deselected	Standby
X ¹⁾	X ¹⁾	X ¹⁾	X ¹⁾	H	H	High-Z	High-Z	Deselected	Standby
L	H	H	H	L	X ¹⁾	High-Z	High-Z	Output Disabled	Active
L	H	H	H	X ¹⁾	L	High-Z	High-Z	Output Disabled	Active
L	H	L	H	L	H	Dout	High-Z	Lower Byte Read	Active
L	H	L	H	H	L	High-Z	Dout	Upper Byte Read	Active
L	H	L	H	L	L	Dout	Dout	Word Read	Active
L	H	X ¹⁾	L	L	H	Din	High-Z	Lower Byte Write	Active
L	H	X ¹⁾	L	H	L	High-Z	Din	Upper Byte Write	Active
L	H	X ¹⁾	L	L	L	Din	Din	Word Write	Active

1. X means don't care. (Must be low or high state)

ABSOLUTE MAXIMUM RATINGS¹⁾

Item	Symbol	Ratings	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-0.2 to 3.0V	V
Voltage on Vcc supply relative to Vss	V _{CC}	-0.2 to 3.6V	V
Power Dissipation	P _D	1.0	W
Storage temperature	T _{STG}	-55 to 150	°C
Operating Temperature	T _A	-40 to 85	°C

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS¹⁾

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V _{CC}	2.4	2.5	2.6	V
Ground	V _{SS}	0	0	0	V
Input high voltage	V _{IH}	2.0	-	V _{CC} +0.2 ²⁾	V
Input low voltage	V _{IL}	-0.2 ³⁾	-	0.6	V

Note:

1. Industrial Product: T_A=-40 to 85°C, otherwise specified
2. Overshoot: V_{CC} + 1.0 V in case of pulse width ≤ 20ns
3. Undershoot: -1.0 V in case of pulse width ≤ 20ns
4. Overshoot and undershoot are sampled, not 100% tested.

CAPACITANCE¹⁾ (f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C _{IN}	V _{IN} =0V	-	8	pF
Input/Output capacitance	C _{IO}	V _{IO} =0V	-	10	pF

1. Capacitance is sampled, not 100% tested

DC AND OPERATING CHARACTERISTICS

Item	Symbol	Test Conditions	Min	Typ	Max	Unit
Input leakage current	I _{LI}	V _{IN} =V _{SS} to V _{CC}	-1	-	1	μA
Output leakage current	I _{LO}	$\overline{CS}_1 = V_{IH}$, CS ₂ =V _{IL} or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$, V _{IO} =V _{SS} to V _{CC}	-1	-	1	μA
Operating power supply	I _{CC}	I _{IO} =0mA, $\overline{CS}_1 = V_{IL}$, CS ₂ =V _{IH} , V _{IN} =V _{IH} or V _{IL}	-	-	2	mA
Average operating current	I _{CC1}	Cycle time=1μs, 100%duty, I _{IO} =0mA, $\overline{CS}_1 \leq 0.2V$, CS ₂ ≥V _{CC} -0.2V, V _{IN} ≤0.2V or V _{IN} ≥V _{CC} -0.2V	-	-	4	mA
	I _{CC2}	Cycle time=Min, I _{IO} =0mA, 100% duty, $\overline{CS}_1 = V_{IL}$, CS ₂ =V _{IH} , V _{IN} =V _{IL} or V _{IH}	-	-	35	mA
Output low voltage	V _{OL}	I _{OL} = 0.5mA	-	-	0.4	V
Output high voltage	V _{OH}	I _{OH} = -0.5mA	2.0	-	-	V
Standby Current(TTL)	I _{SB}	$\overline{CS}_1 = V_{IH}$, CS ₂ =V _{IL} , Other inputs=V _{IH} or V _{IL}	-	-	0.3	mA
Standby Current (CMOS)	I _{SB1}	$\overline{CS}_1 \geq V_{CC}-0.2V$, CS ₂ ≥V _{CC} -0.2V($\overline{CS}_1$ controlled) or CS ₂ ≤0.2V(CS ₂ controlled), Other inputs=0~V _{CC}	-	0.5	10 ¹⁾	μA

1. Super low power product=5μA with special handling.

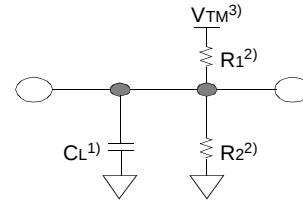
AC OPERATING CONDITIONS

TEST CONDITIONS (Test Load and Test Input/Output Reference)

Input pulse level: 0.4 to 2.2V

Input rising and falling time: 5ns

Input and output reference voltage: 1.1V

Output load (See right): $C_L = 100\text{pF} + 1\text{TTL}$
 $C_L = 30\text{pF} + 1\text{TTL}$ 

1. Including scope and jig capacitance

2. $R_1 = 3070\Omega$, $R_2 = 3150\Omega$ 3. $V_{TM} = 2.3\text{V}$ AC CHARACTERISTICS ($T_A = -40$ to 85°C , $V_{CC} = 2.4 \sim 2.6\text{V}$)

Parameter List		Symbol	Speed Bins				Units
			70ns		100ns		
			Min	Max	Min	Max	
Read	Read cycle time	t _{RC}	70	-	100	-	ns
	Address access time	t _{AA}	-	70	-	100	ns
	Chip select to output	t _{CO}	-	70	-	100	ns
	Output enable to valid output	t _{OE}	-	35	-	50	ns
	$\overline{\text{UB}}$, $\overline{\text{LB}}$ Access Time	t _{BA}	-	70	-	100	ns
	Chip select to low-Z output	t _{LZ}	10	-	10	-	ns
	$\overline{\text{UB}}$, $\overline{\text{LB}}$ enable to low-Z output	t _{BLZ}	10	-	10	-	ns
	Output enable to low-Z output	t _{OLZ}	5	-	5	-	ns
	Chip disable to high-Z output	t _{HZ}	0	25	0	30	ns
	$\overline{\text{UB}}$, $\overline{\text{LB}}$ disable to high-Z output	t _{BHZ}	0	25	0	30	ns
	Output disable to high-Z output	t _{OHZ}	0	25	0	30	ns
	Output hold from address change	t _{OH}	10	-	15	-	ns
Write	Write cycle time	t _{WC}	70	-	100	-	ns
	Chip select to end of write	t _{CW}	60	-	80	-	ns
	Address set-up time	t _{AS}	0	-	0	-	ns
	Address valid to end of write	t _{AW}	60	-	80	-	ns
	$\overline{\text{UB}}$, $\overline{\text{LB}}$ Valid to End of Write	t _{BW}	60	-	80	-	ns
	Write pulse width	t _{WP}	55	-	70	-	ns
	Write recovery time	t _{WR}	0	-	0	-	ns
	Write to output high-Z	t _{WHZ}	0	25	0	30	ns
	Data to write time overlap	t _{DW}	30	-	40	-	ns
	Data hold from write time	t _{DH}	0	-	0	-	ns
	End write to output low-Z	t _{OW}	5	-	5	-	ns

Note: Functional check only with CS2, when the device is required CS2 access in a system it must be applied 100ns speed bin.

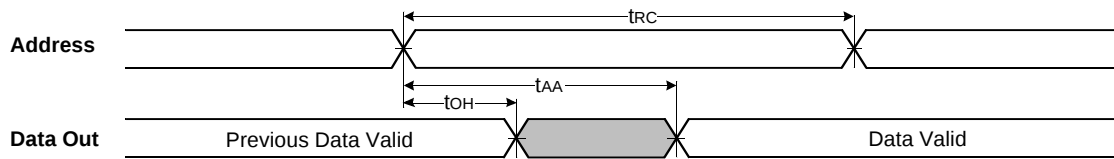
DATA RETENTION CHARACTERISTICS

Item	Symbol	Test Condition	Min	Typ	Max	Unit
V _{CC} for data retention	VDR	$\overline{\text{CS}}_1 \geq V_{CC} - 0.2\text{V}^{(1)}$	1.5	-	2.6	V
Data retention current	IDR	$V_{CC} = 1.5\text{V}$, $\overline{\text{CS}}_1 \geq V_{CC} - 0.2\text{V}^{(1)}$	-	0.5	3 ⁽²⁾	μA
Data retention set-up time	t _{SDR}	See data retention waveform	0	-	-	ns
Recovery time	t _{RDR}		t _{RC}	-	-	

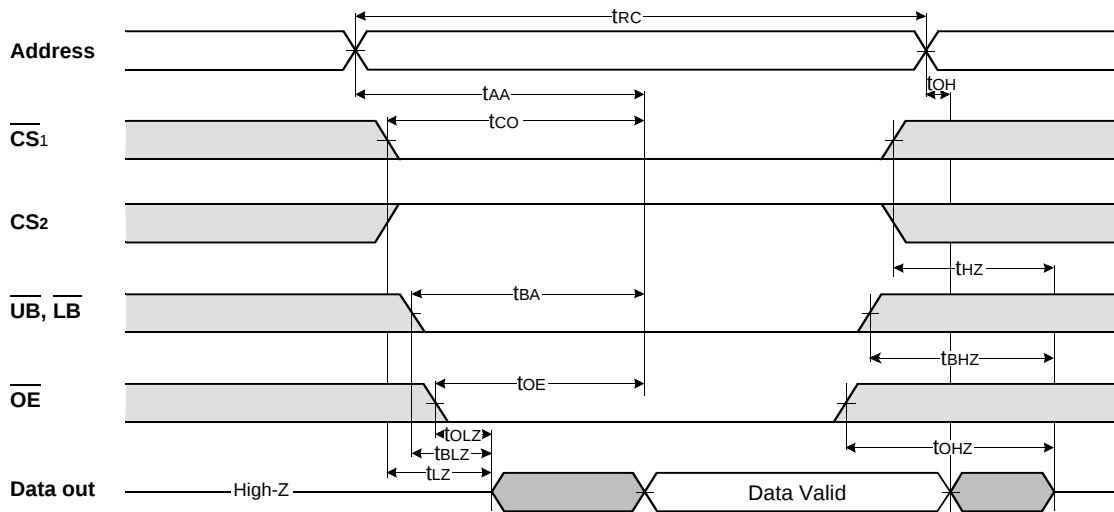
1. $\overline{\text{CS}}_1 \geq V_{CC} - 0.2\text{V}$, $\overline{\text{CS}}_2 \geq V_{CC} - 0.2\text{V}$ ($\overline{\text{CS}}_1$ controlled) or $\overline{\text{CS}}_2 \leq 0.2\text{V}$ ($\overline{\text{CS}}_2$ controlled)2. Super low power product = $2\mu\text{A}$ with special handling.

TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{CS1}=\overline{OE}=V_{IL}$, $\overline{CS2}=\overline{WE}=V_{IH}$, $\overline{UB}$ or/and $\overline{LB}=V_{IL}$)



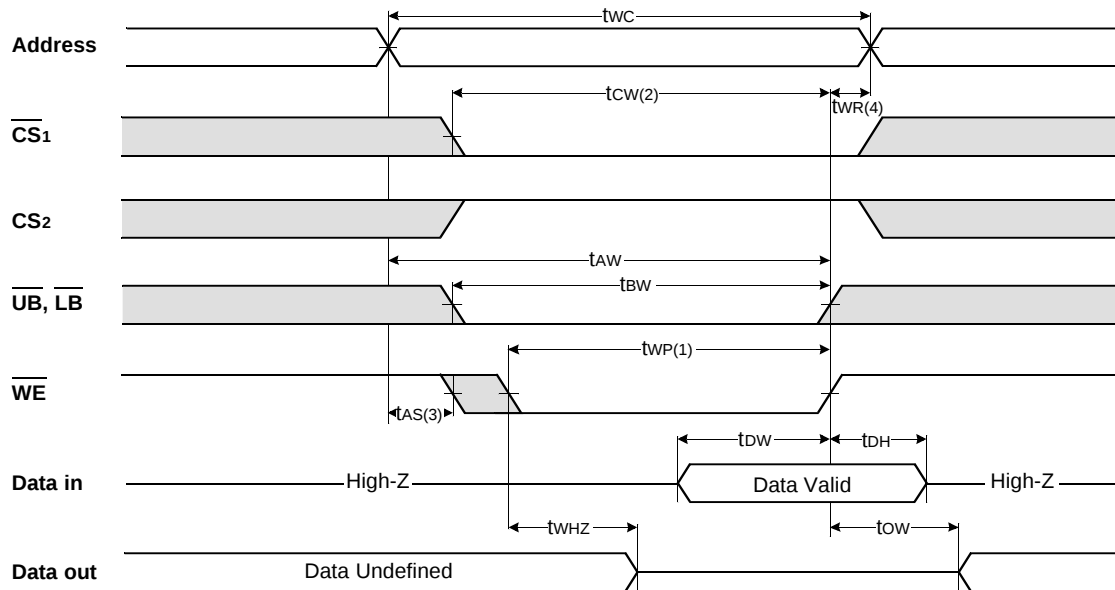
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}=V_{IH}$)



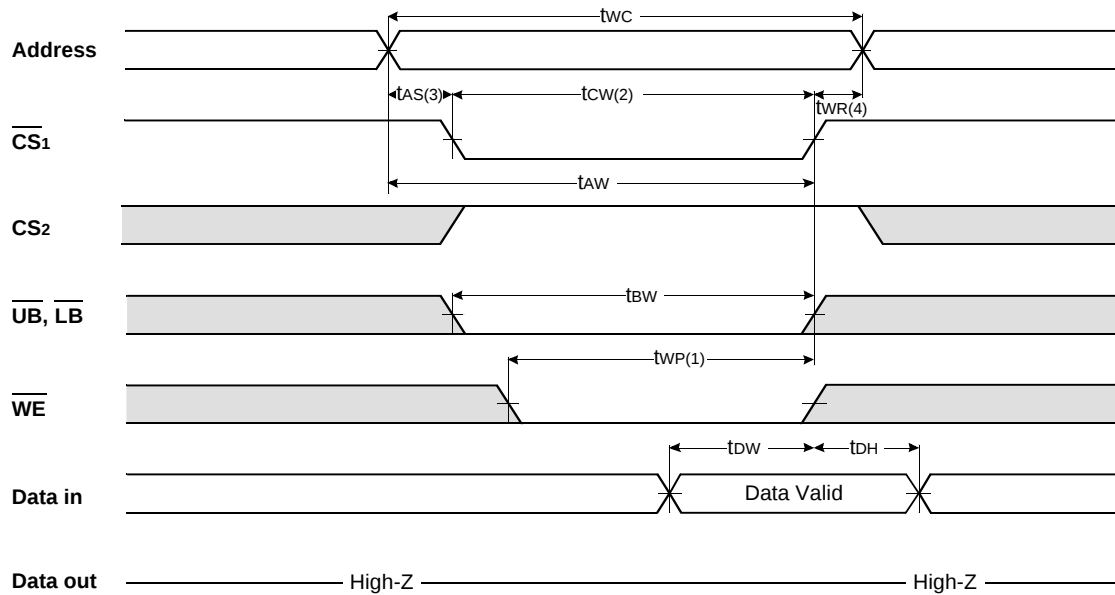
NOTES (READ CYCLE)

1. t_{THZ} and t_{TOHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, $t_{THZ}(\text{Max.})$ is less than $t_{TLZ}(\text{Min.})$ both for a given device and from device to device interconnection.

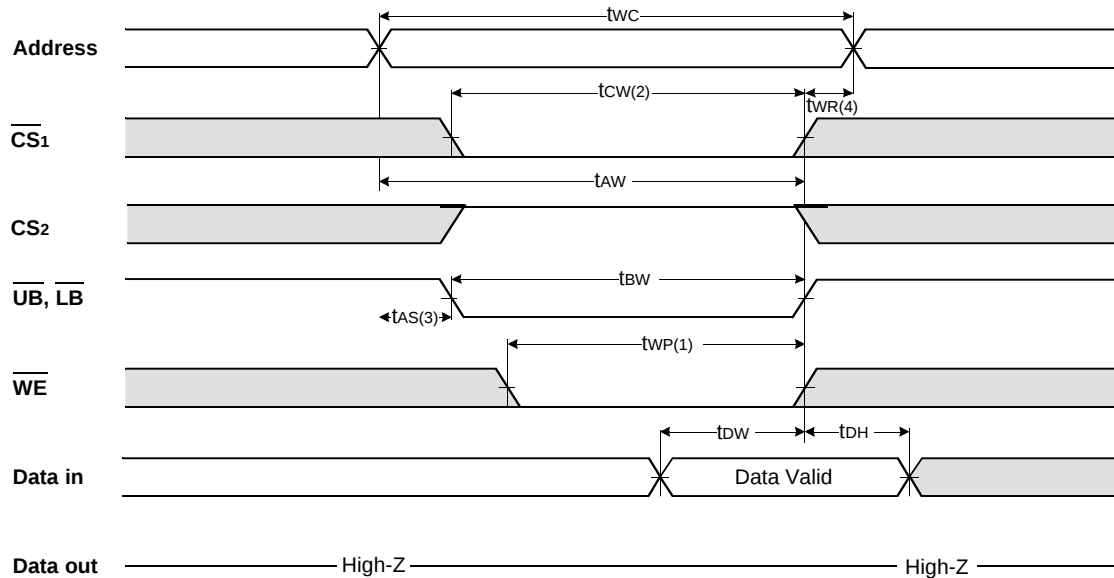
TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{\text{WE}}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{\text{CS1}}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(3) ($\overline{UB}$, $\overline{LB}$ Controlled)

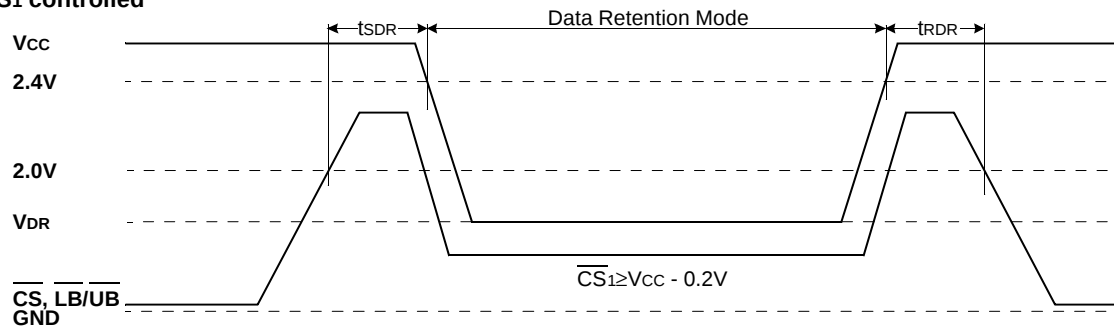


NOTES (WRITE CYCLE)

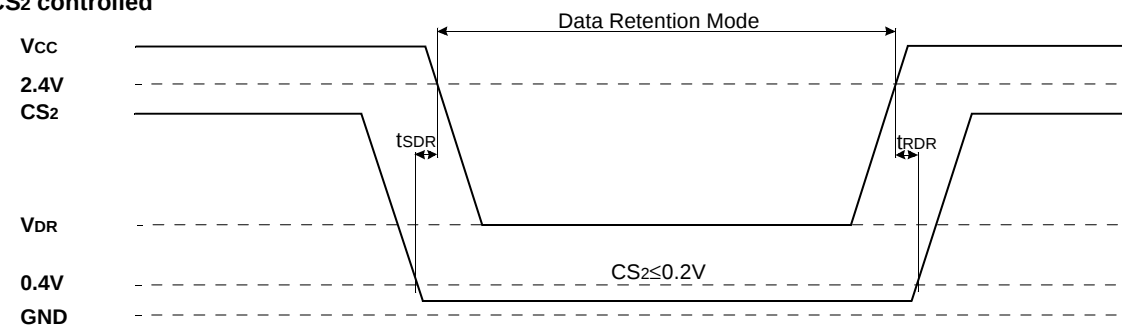
1. A write occurs during the overlap(t_{WP}) of low $\overline{CS1}$ and low $\overline{WE}$. A write begins when $\overline{CS1}$ goes low and $\overline{WE}$ goes low with asserting $\overline{UB}$ or $\overline{LB}$ for single byte operation or simultaneously asserting $\overline{UB}$ and $\overline{LB}$ for double byte operation. A write ends at the earliest transition when $\overline{CS1}$ goes high and $\overline{WE}$ goes high. The t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the $\overline{CS1}$ going low to end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{CS1}$ or $\overline{WE}$ going high.

DATA RETENTION WAVE FORM

$\overline{CS1}$ controlled

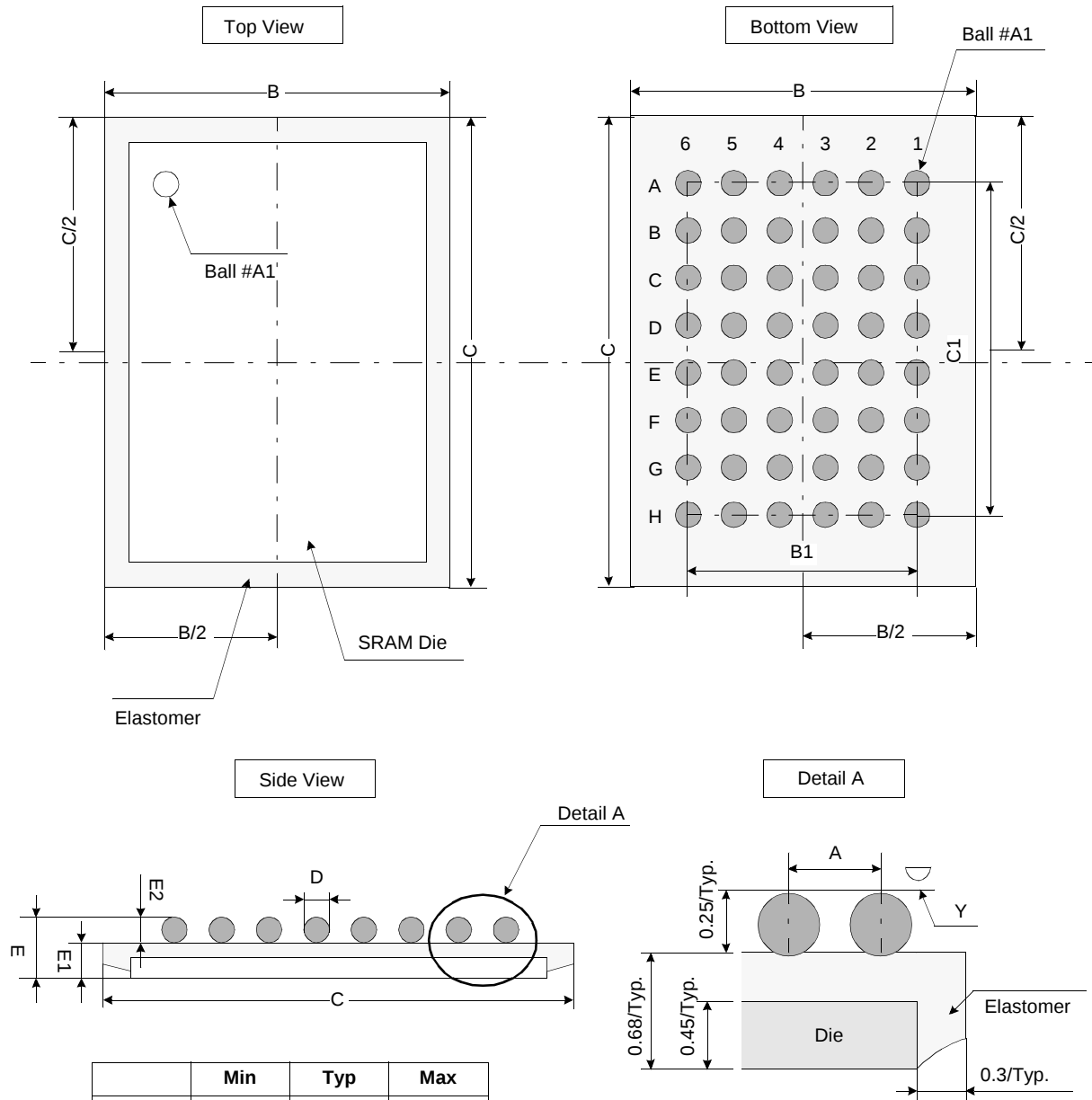


$\overline{CS2}$ controlled



PACKAGE DIMENSIONS

Units: millimeters



Notes.

1. Bump counts: 48(8row x 6column)
2. Bump pitch: (x,y)=(0.75 x 0.75)(typ.)
3. All tolerance are +/-0.050 unless otherwise specified.
4. Typ: Typical
5. Y is coplanarity: 0.08(Max)