

Document Title

64Kx8 bit Low Power and Low Voltage CMOS Static RAM

Revision History

<u>Revision No.</u>	<u>History</u>	<u>Draft Data</u>	<u>Remark</u>
0	Design target	November 25, 1997	Advance
1.0	Finalize	August 27, 1998	Final

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64Kx8 bit Low Power and Low Voltage CMOS Static RAM

FEATURES

- Process Technology: TFT
- Organization: 64Kx8
- Power Supply Voltage
 - KM68V512A family: 3.0~3.6V
 - KM68U512A family: 2.7~3.3V
- Low Data Retention Voltage: 2V(Min)
- Three state output and TTL Compatible
- Package Type: 32-TSOP1-0820F, 32-TSOP1-0813.4F

GENERAL DESCRIPTION

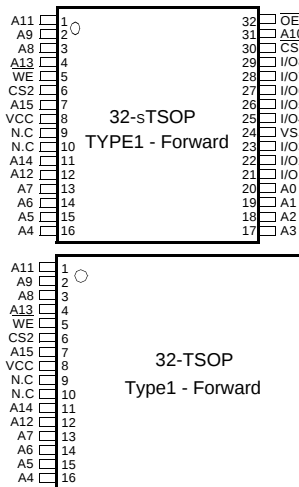
The K6T0908V2B and K6T0908U2B families are fabricated by SAMSUNG's advanced CMOS process technology. The families support various operating temperature ranges and has various package types for user flexibility of system design. The family also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation		PKG Type
				Standby (Isb1, Max)	Operating (Icc2, Max)	
K6T0908V2B-B	Commercial(0~70°C)	3.0 ~ 3.6V	85 ¹⁾ /100ns	10μA	30mA	32-TSOP1-F 32-sTSOP1-F
K6T0908U2B-B		2.7 ~ 3.3V			25mA	
K6T0908V2B-F	Industrial(-40~85°C)	3.0 ~ 3.6V			30mA	
K6T0908U2B-F		2.7 ~ 3.3V			25mA	

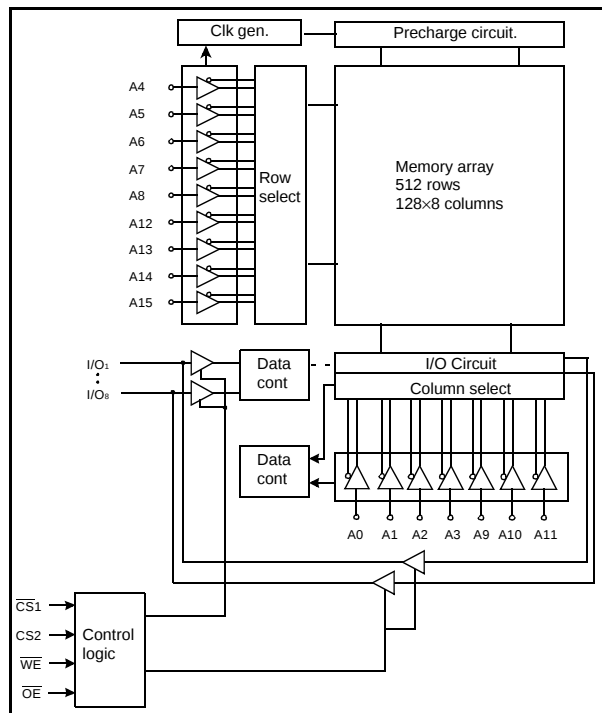
1. The parameter is measured with 30pF test load.

PIN DESCRIPTION



Name	Function	Name	Function
CS1, CS2	Chip Select Inputs	I/O1~I/O8	Data Inputs/Outputs
OE	Output Enable	Vcc	Power
WE	Write Enable Input	Vss	Ground
A0~A15	Address Inputs	N.C	No Connection

FUNCTIONAL BLOCK DIAGRAM



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PRODUCT LIST

Commercial Temperature Products(0~70°C)		Industrial Temperature Products(-40~85°C)	
Part Name	Function	Part Name	Function
K6T0908V2B-TB85 K6T0908V2B-TB10	32-TSOP1 F, 85ns, 3.3V, LL 32-TSOP1 F, 100ns, 3.3V, LL	K6T0908V2B-TF85 K6T0908V2B-TF10 K6T0908V2B-YF85 K6T0908V2B-YF10	32-TSOP1 F, 85ns, 3.3V, LL 32-TSOP1 F, 100ns, 3.3V, LL 32-sTSOP1 F, 85ns,3.3V,LL 32-sTSOP1 F, 100ns,3.3V,LL
K6T0908U2B-TB85 K6T0908U2B-TB10	32-TSOP1 F, 85ns, 3.0V, LL 32-TSOP1 F, 100ns, 3.0V, LL	K6T0908U2B-TF85 K6T0908U2B-TF10 K6T0908U2B-YF85 K6T0908U2B-YF10	32-TSOP1 F, 85ns, 3.0V, LL 32-TSOP1 F, 100ns, 3.0V, LL 32-sTSOP1 F, 85ns, 3.0V, LL 32-sTSOP1 F, 100ns,3.0V, LL

FUNCTIONAL DESCRIPTION

CS ₁	CS ₂	OE	WE	I/O	Mode	Power
H	X ¹⁾	X ¹⁾	X ¹⁾	High-Z	Deselected	Standby
X ¹⁾	L	X ¹⁾	X ¹⁾	High-Z	Deselected	Standby
L	H	H	H	High-Z	Output Disabled	Active
L	H	L	H	Dout	Read	Active
L	H	X ¹⁾	L	Din	Write	Active

1. X means don't care (Must be in high or low states)

ABSOLUTE MAXIMUM RATINGS¹⁾

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	V _{IN} ,V _{OUT}	-0.5 to V _{CC} +0.5	V	-
Voltage on Vcc supply relative to Vss	V _{CC}	-0.3 to 4.6	V	-
Power Dissipation	P _D	1	W	-
Storage temperature	T _{STG}	-65 to 150	°C	-
Operating Temperature	T _A	0 to 70	°C	K6T0908V2B-L, K6T0908U2B-L
		-40 to 85	°C	K6T0908V2B-P, K6T0908U2B-P
Soldering temperature and time	T _{SOLDER}	260°C, 10sec (Lead Only)	-	-

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS¹⁾

Item	Symbol	Product	Min	Typ	Max	Unit
Supply voltage	V _{CC}	K6T0908V2B Family	3.0	3.3	3.6	V
		K6T0908U2B Family	2.7	3.0	3.3	V
Ground	V _{SS}	All Family	0	0	0	V
Input high voltage	V _{IH}	K6T0908V2B, K6T0908U2B Family	2.2	-	V _{CC} +0.3V ²⁾	V
Input low voltage	V _{IL}	K6T0908V2B, K6T0908U2B Family	-0.3 ³⁾	-	0.6	V

Note:

1. Commercial Product : T_A=0 to 70°C, otherwise specifiedIndustrial Product : T_A=-40 to 85°C, otherwise specified2. Overshoot : V_{CC}+3.0V in case of pulse width ≤ 30ns

3. Undershoot : -3.0V in case of pulse width ≤ 30ns

4. Overshoot and undershoot are sampled, not 100% tested

CAPACITANCE¹⁾ (f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C _{IN}	V _{IN} =0V	-	6	pF
Input/Output capacitance	C _{IO}	V _{IO} =0V	-	8	pF

1. Capacitance is sampled, not 100% tested

DC AND OPERATING CHARACTERISTICS

Item	Symbol	Test Conditions		Min	Typ	Max	Unit
Input leakage current	I _{LI}	V _{IN} =V _{SS} to V _{CC}		-1	-	1	μA
Output leakage current	I _{LO}	$\overline{CS_1}$ =V _{IH} or CS ₂ =V _{IL} or $\overline{OE}$ =V _{IH} or $\overline{WE}$ =V _{IL} , V _{IO} =V _{SS} to V _{CC}		-1	-	1	μA
Operating power supply	I _{CC}	I _{IO} =0mA, $\overline{CS_1}$ =V _{IL} , CS ₂ =V _{IH} , V _{IN} =V _{IH} or V _{IL} , Read		-	-	5	mA
Average operating current	I _{CC1}	Cycle time=1μs, 100% duty, I _{IO} =0mA, $\overline{CS_1}$ ≤0.2V, CS ₂ ≥V _{CC} -0.2V, V _{IN} ≤0.2V or V _{IN} ≥V _{CC} -0.2V		-	-	5	mA
	I _{CC2}	Cycle time=Min, 100% duty, I _{IO} =0mA	K6T0908V2B	-	-	30	mA
		$\overline{CS_1}$ =V _{IL} , CS ₂ =V _{IH} , V _{IN} =V _{IL} or V _{IH}	K6T0908U2B	-	-	25	mA
Output low voltage	V _{OL}	I _{OL} =2.1mA		-	-	0.4	V
Output high voltage	V _{OH}	I _{OH} =-1.0mA		2.4	-	-	V
Standby Current(TTL)	I _{SB}	$\overline{CS_1}$ =V _{IH} , CS ₂ =V _{IL} , Other inputs=V _{IL} or V _{IH}		-	-	0.3	mA
Standby Current (CMOS)	I _{SB1}	$\overline{CS_1}$ ≥V _{CC} -0.2V, CS ₂ ≥V _{CC} -0.2V, or CS ₂ ≤0.2V, Other inputs=0~V _{CC}		-	-	10	μA

AC OPERATING CONDITIONS

TEST CONDITIONS (Test Load and Test Input/Output Reference)

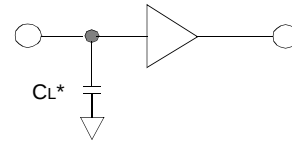
Input pulse level : 0.4 to 2.2V

Input rising and falling time : 5ns

Input and output reference voltage : 1.5V

Output load (See right) : $C_L^{(1)}=100\text{pF}+1\text{TTL}$

1. 85ns part tested with 30pF test load.



* Including scope and jig capacitance

AC CHARACTERISTICS (K6T0908V2B Family: $V_{CC}=3.0\sim 3.6\text{V}$, K6T0908U2B Family: $V_{CC}=2.7\sim 3.3\text{V}$, Commercial products: $T_A=0$ to 70°C , Industrial products: $T_A=-40$ to 85°C)

Parameter List		Symbol	Speed Bins				Units
			85ns		100ns		
			Min	Max	Min	Max	
Read	Read cycle time	t _{RC}	85	-	100	-	ns
	Address access time	t _{AA}	-	85	-	100	ns
	Chip select to output	t _{CO}	-	85	-	100	ns
	Output enable to valid output	t _{OE}	-	45	-	50	ns
	Chip select to low-Z output	t _{LZ}	10	-	10	-	ns
	Output enable to low-Z output	t _{OLZ}	5	-	5	-	ns
	Chip disable to high-Z output	t _{HZ}	0	30	0	30	ns
	Output disable to high-Z output	t _{OHZ}	0	20	0	20	ns
	Output hold from address change	t _{OH}	10	-	15	-	ns
Write	Write cycle time	t _{WC}	85	-	100	-	ns
	Chip select to end of write	t _{CW}	70	-	80	-	ns
	Address set-up time	t _{AS}	0	-	0	-	ns
	Address valid to end of write	t _{AW}	70	-	80	-	ns
	Write pulse width	t _{WP}	60	-	70	-	ns
	Write recovery time	t _{WR}	0	-	0	-	ns
	Write recovery time	t _{WR1}	0	-	0	-	ns
	Write to output high-Z	t _{WHZ}	0	25	0	30	ns
	Data to write time overlap	t _{DW}	35	-	40	-	ns
	Data hold from write time	t _{DH}	0	-	0	-	ns
	End write to output low-Z	t _{OW}	5	-	5	-	ns

DATA RETENTION CHARACTERISTICS

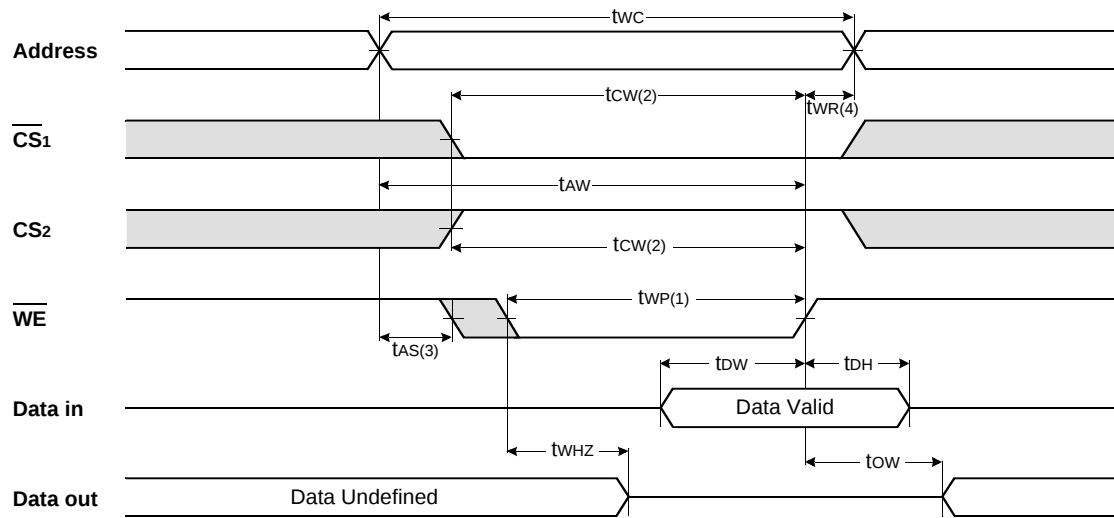
Item	Sym	Test Condition	Min	Typ	Max	Unit
V _{CC} for data retention	V _{DR}	$\overline{CS}_1 \geq V_{CC}-2.0\text{V}$, $CS_2 \geq V_{CC}-2.0\text{V}$ or $CS_2 \leq 0.2\text{V}$	2.0	-	3.6	V
Data retention current	I _{DR}	$V_{CC}=3.0\text{V}$, $\overline{CS}_1 \leq V_{CC}-0.2\text{V}$, $CS_2 \geq V_{CC}-0.2\text{V}$ or $CS_2 \leq 0.2\text{V}$	-	-	10	μA
Data retention set-up time	t _{SDR}	See data retention waveform	0	-	-	ms
Recovery time	t _{RDR}		5	-	-	

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{\text{CS}}_1=\overline{\text{OE}}=\text{V}_{\text{IL}}$, $\overline{\text{WE}}=\text{V}_{\text{IH}}$)

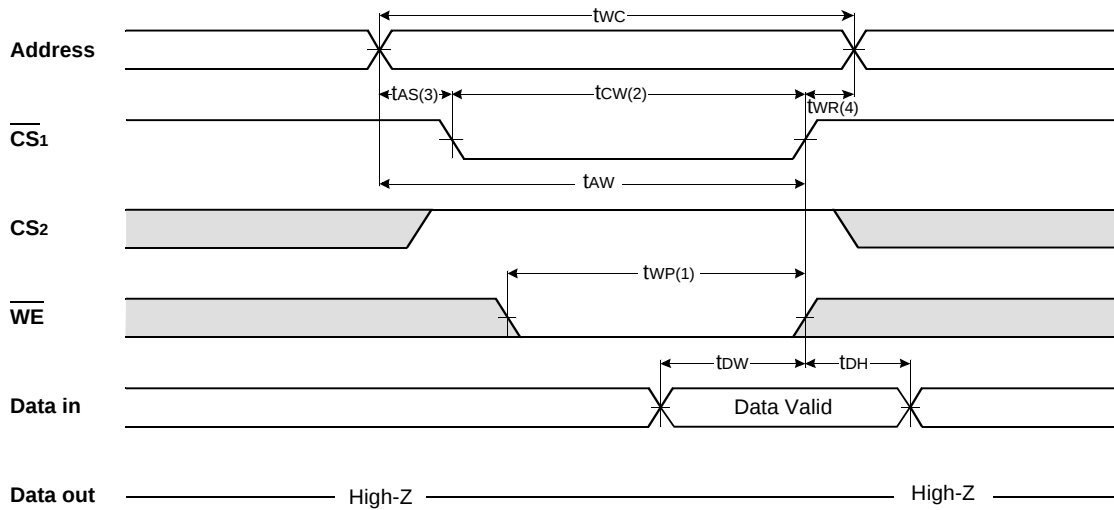


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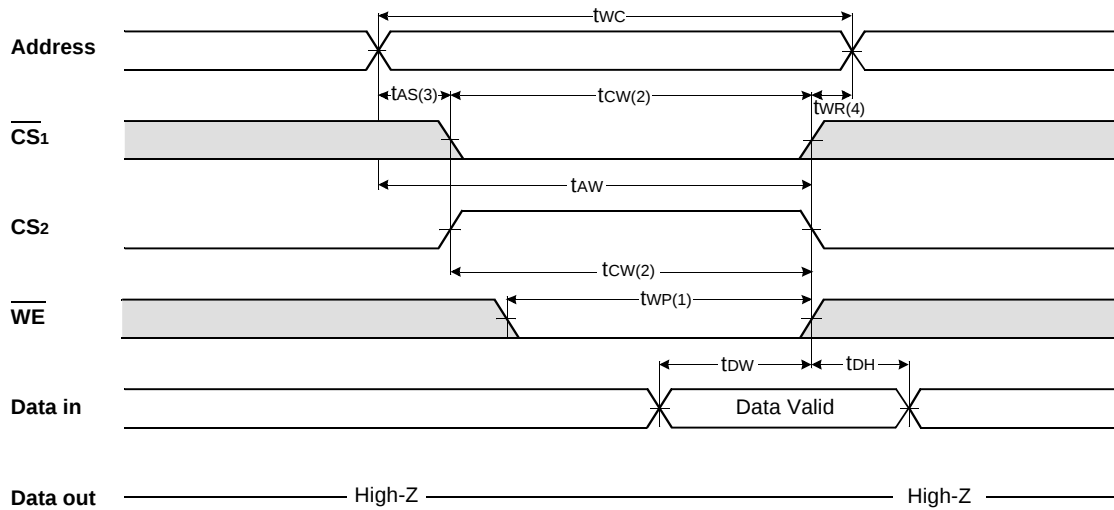
TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{\text{WE}}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{\text{CS1}}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(3) (CS₂ Controlled)

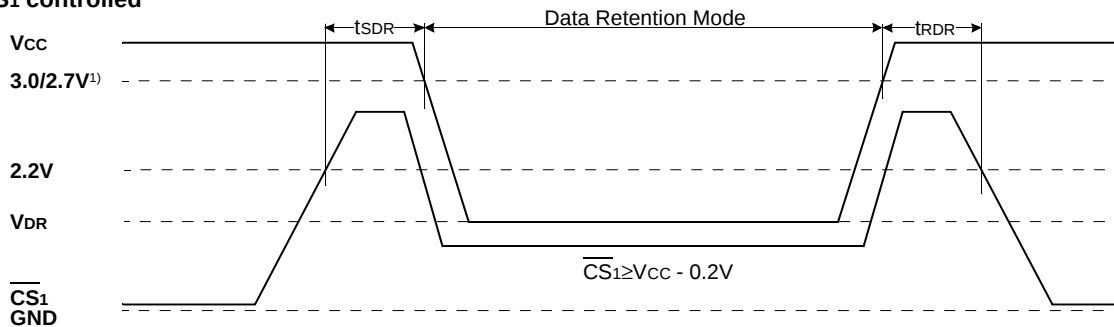


NOTES (WRITE CYCLE)

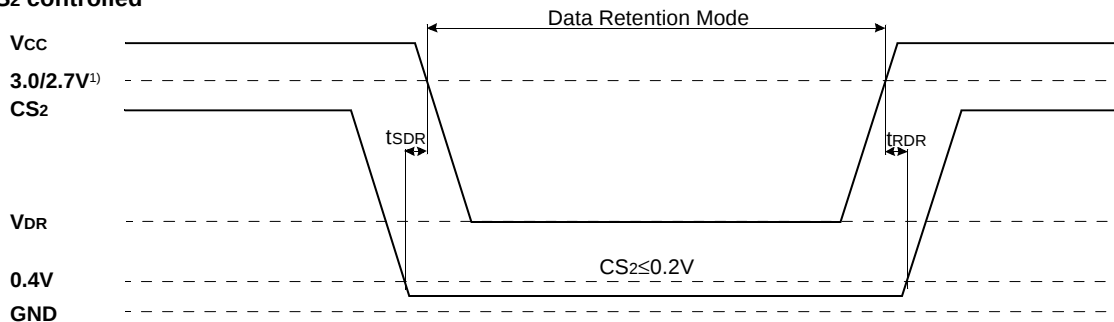
1. A write occurs during the overlap of a low $\overline{CS_1}$, a high CS_2 and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS_1}$ goes low, CS_2 going high and $\overline{WE}$ going low : A write end at the earliest transition among $\overline{CS_1}$ going high, CS_2 going low and $\overline{WE}$ going high, t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the $\overline{CS_1}$ going low or CS_2 going high to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. $t_{WR(1)}$ applied in case a write ends as $\overline{CS_1}$ or $\overline{WE}$ going high $t_{WR(2)}$ applied in case a write ends as CS_2 going to low.

DATA RETENTION WAVE FORM

$\overline{CS_1}$ controlled



CS₂ controlled



1. 3.0V for K6T0908V2B Family, 2.7V for K6T0908U2B Family

CMOS SRAM

Units: millimeter(Inch)

Technical drawing of a rectangular component with dimensions and tolerances. The drawing includes a top view and a side view.

Top View Dimensions:

- Overall width: 20.00 ± 0.20
- Overall height: 0.787 ± 0.008
- Left side features:
 - Top edge: $0.20 \begin{smallmatrix} +0.10 \\ -0.05 \end{smallmatrix}$
 - Bottom edge: $0.008 \begin{smallmatrix} +0.004 \\ -0.002 \end{smallmatrix}$
- Right side features:
 - Top edge: $8.40 \begin{smallmatrix} +0.10 \\ -0.05 \end{smallmatrix}$
 - Bottom edge: $0.331 \begin{smallmatrix} +0.004 \\ -0.002 \end{smallmatrix}$
- Internal dimensions:
 - Width: 18.40 ± 0.10
 - Height: 0.724 ± 0.004
- Corner radius: $0.25 \begin{smallmatrix} +0.10 \\ -0.05 \end{smallmatrix}$ TYP
- Bottom edge chamfer: $0.45 \sim 0.75 \begin{smallmatrix} +0.004 \\ -0.002 \end{smallmatrix}$

Side View Dimensions:

- Overall height: $8.00 \begin{smallmatrix} +0.10 \\ -0.05 \end{smallmatrix}$
- Internal height: $0.315 \begin{smallmatrix} +0.004 \\ -0.002 \end{smallmatrix}$
- Bottom edge: $0.05 \begin{smallmatrix} +0.002 \\ -0.001 \end{smallmatrix}$ MIN
- Internal width: 1.00 ± 0.10
- Internal height: 0.039 ± 0.004
- Internal width: $1.20 \begin{smallmatrix} +0.004 \\ -0.002 \end{smallmatrix}$
- Internal height: $0.047 \begin{smallmatrix} +0.004 \\ -0.002 \end{smallmatrix}$ MAX
- Bottom edge: $0.15 \begin{smallmatrix} +0.10 \\ -0.05 \end{smallmatrix}$
- Internal width: $0.006 \begin{smallmatrix} +0.004 \\ -0.002 \end{smallmatrix}$
- Internal height: $0.004 \begin{smallmatrix} +0.004 \\ -0.002 \end{smallmatrix}$ MAX
- Internal width: $1.10 \begin{smallmatrix} +0.004 \\ -0.002 \end{smallmatrix}$ MAX

[illegible]