

Document Title**64K x16 bit Low Power CMOS Static RAM****Revision History**

<u>Revision No.</u>	<u>History</u>	<u>Draft Data</u>	<u>Remark</u>
0.0	Initial draft	August 12, 1995	Preliminary
1.0	Finalize - One datasheet for commercial and industrial part.	April 15, 1996	Final
2.0	Revised - Change datasheet format. - Remove Icc write current value. - Remove low power product from product	February 12, 1998	Final

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64K x16 bit Low Power CMOS Static RAM**FEATURES SUMMARY**

- Process Technology: Poly Load
- Organization: 64K x16
- Data Byte Control: $\overline{\text{LB}}=\text{I/O}_1\sim 8$, $\overline{\text{UB}}=\text{I/O}_9\sim 16$
- Power Supply Voltage: 4.5~5.5V
- Low Data Retention Voltage: 2V(Min)
- Three state output and TTL Compatible
- Package Type: 44-TSOP2-400F/R

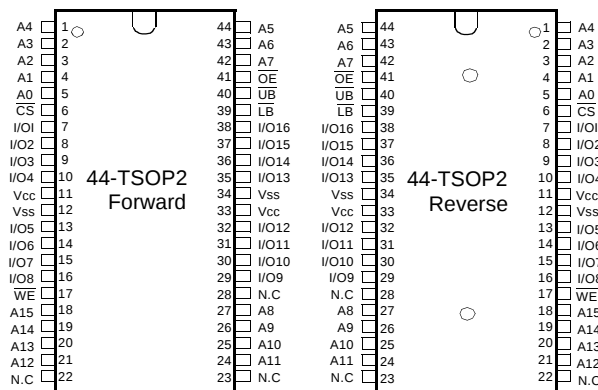
GENERAL DESCRIPTION

The K6L1016C3B families are fabricated by SAMSUNG's advanced CMOS process technology. The families support various operating temperature ranges and have various package types for user flexibility of system design. The families also support low data retention voltage for battery back-up operation with low data retention current.

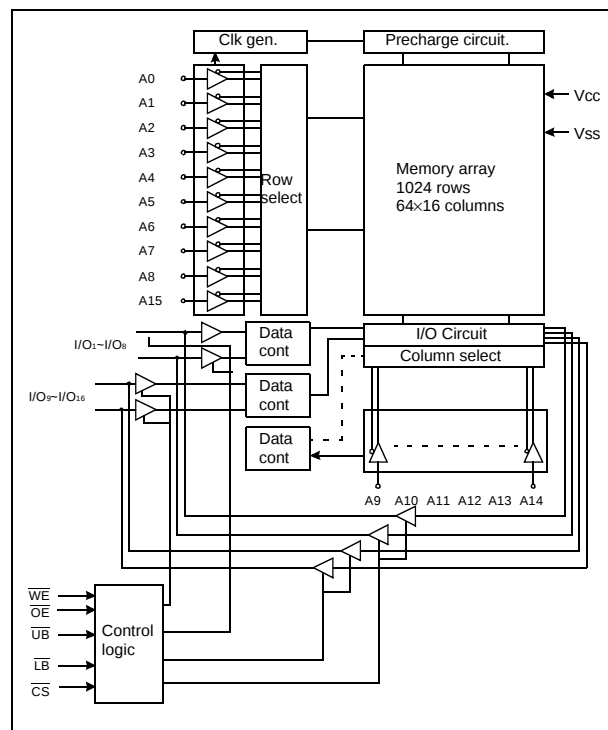
PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation		PKG Type
				Standby (I _{SB1} , Max)	Operating (I _{CC2} , Max)	
K6L1016C3B-B	Commercial(0~70°C)	4.5 to 5.5V	55*/70ns	20μA	120mA	44-TSOP2-F/R
K6L1016C3B-F	Industrial(-40~85°C)		70/100ns	50μA		

1. The parameter is measured with 30pF test load.

PIN DESCRIPTION

Name	Function	Name	Function
$\overline{\text{CS}}$	Chip Select Input	Vcc	Power
$\overline{\text{OE}}$	Output Enable Input	Vss	Ground
$\overline{\text{WE}}$	Write Enable Input	$\overline{\text{LB}}$	Lower Byte (I/O ₁ ~8)
A ₀ ~A ₁₅	Address Inputs	$\overline{\text{UB}}$	Upper Byte (I/O ₉ ~16)
I/O ₁ ~16	Data Inputs/Outputs	N.C	No Connection

FUNCTIONAL BLOCK DIAGRAM

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PRODUCT LIST

Commercial Temperature Product(0~70°C)		Industrial Temperature Products(-40~85°C)	
Part Name	Function	Part Name	Function
K6L1016C3B-TB55	44-TSOP2-F, 5V, 55ns, LL-pwr	K6L1016C3B-TF70	44-TSOP2-F, 5V, 70ns, LL-pwr
K6L1016C3B-TB70	44-TSOP2-F, 5V, 70ns, LL-pwr	K6L1016C3B-TF10	44-TSOP2-F, 5V, 100ns, LL-pwr
K6L1016C3B-RB55	44-TSOP2-R, 5V, 55ns, LL-pwr	K6L1016C3B-RF70	44-TSOP2-R, 5V, 70ns, LL-pwr
K6L1016C3B-RB70	44-TSOP2-R, 5V, 70ns, LL-pwr	K6L1016C3B-RF10	44-TSOP2-R, 5V, 100ns, LL-pwr

FUNCTIONAL DESCRIPTION

$\overline{\text{CS}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	$\overline{\text{LB}}$	$\overline{\text{UB}}$	I/O ₁₋₈	I/O ₉₋₁₆	Mode	Power
H	X ¹⁾	X ¹⁾	X ¹⁾	X ¹⁾	High-Z	High-Z	Deselected	Standby
L	H	H	X ¹⁾	X ¹⁾	High-Z	High-Z	Output Disabled	Active
L	X ¹⁾	X ¹⁾	H	H	High-Z	High-Z	Output Disabled	Active
L	L	H	L	H	Dout	High-Z	Lower Byte Read	Active
L	L	H	H	L	High-Z	Dout	Upper Byte Read	Active
L	L	H	L	L	Dout	Dout	Word Read	Active
L	X ¹⁾	L	L	H	Din	High-Z	Lower Byte Write	Active
L	X ¹⁾	L	H	L	High-Z	Din	Upper Byte Write	Active
L	X ¹⁾	L	L	L	Din	Din	Word Write	Active

1. X means don't care. (Must be in low or high state)

ABSOLUTE MAXIMUM RATINGS¹⁾

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-0.5 to V _{CC} +0.5	V	-
Voltage on Vcc supply relative to Vss	V _{CC}	-0.5 to 7.0	V	-
Power Dissipation	P _D	1.0	W	-
Storage temperature	T _{STG}	-65 to 150	°C	-
Operating Temperature	T _A	0 to 70	°C	K6L1016C3B-B
		-40 to 85	°C	K6L1016C3B-F
Soldering temperature and time	T _{SOLDER}	260°C, 10sec(Lead Only)	-	-

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS¹⁾

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V _{CC}	4.5	5	5.5	V
Ground	V _{SS}	0	0	0	V
Input high voltage	V _{IH}	2.2	-	V _{CC} +0.5 ²⁾	V
Input low voltage	V _{IL}	-0.5 ³⁾	-	0.8	V

Note:

- Commercial Product : T_A=0 to 70°C, otherwise specified
Industrial Product : T_A=-40 to 85°C, otherwise specified
- Overshoot : V_{CC}+3.0V in case of pulse width ≤ 30ns
- Undershoot : -3.0V in case of pulse width ≤ 30ns
- Overshoot and undershoot are sampled, not 100% tested.

CAPACITANCE¹⁾(f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C _{IN}	V _{IN} =0V	-	6	pF
Input/Output capacitance	C _{IO}	V _{IO} =0V	-	8	pF

- Capacitance is sampled, not 100% tested

DC AND OPERATING CHARACTERISTICS

Item	Symbol	Test Conditions	Min	Typ	Max	Unit
Input leakage current	I _{LI}	V _{IN} =V _{SS} to V _{CC}	-1	-	1	μA
Output leakage current	I _{LO}	$\overline{CS}=V_{IH}$ or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$, V _{IO} =V _{SS} to V _{CC}	-1	-	1	μA
Operating power supply	I _{CC}	I _{IO} =0mA, $\overline{CS}=V_{IL}$, V _{IN} =V _{IL} or V _{IH} , Read	-	-	10	mA
Average operating current	I _{CC1}	Cycle time=1μs, 100% duty, I _{IO} =0mA $\overline{CS} \leq 0.2V$, V _{IN} ≤0.2V or V _{IN} ≥V _{CC} -0.2V	Read	-	-	15
			Write	-	-	40
	I _{CC2}	Cycle time=Min, 100% duty, I _{IO} =0mA, $\overline{CS}=V_{IL}$, V _{IN} =V _{IL} or V _{IH}	-	-	120	mA
Output low voltage	V _{OL}	I _{OL} =2.1mA	-	-	0.4	V
Output high voltage	V _{OH}	I _{OH} =-1.0mA	2.4	-	-	V
Standby Current(TTL)	I _{SB}	$\overline{CS}=V_{IH}$, Other inputs=V _{IL} or V _{IH}	-	-	3	mA
Standby Current(CMOS)	I _{SB1}	$\overline{CS} \geq V_{CC}-0.2V$, Other inputs=0~V _{CC}	-	-	20 ¹⁾	μA

- Industrial Product = 50μA

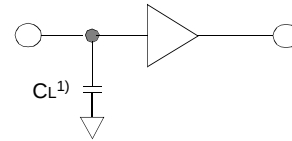
AC OPERATING CONDITIONS

TEST CONDITIONS (Test Load and Test Input/Output Reference)

Input pulse level : 0.8 to 2.4V

Input rising and falling time : 5ns

Input and output reference voltage : 1.5V

Output load (See right) : $C_L=100\text{pF}+1\text{TTL}$ $C_L=30\text{pF}+1\text{TTL}$ 

1. Including scope and jig capacitance

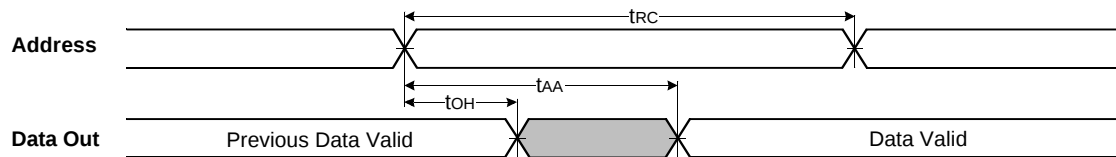
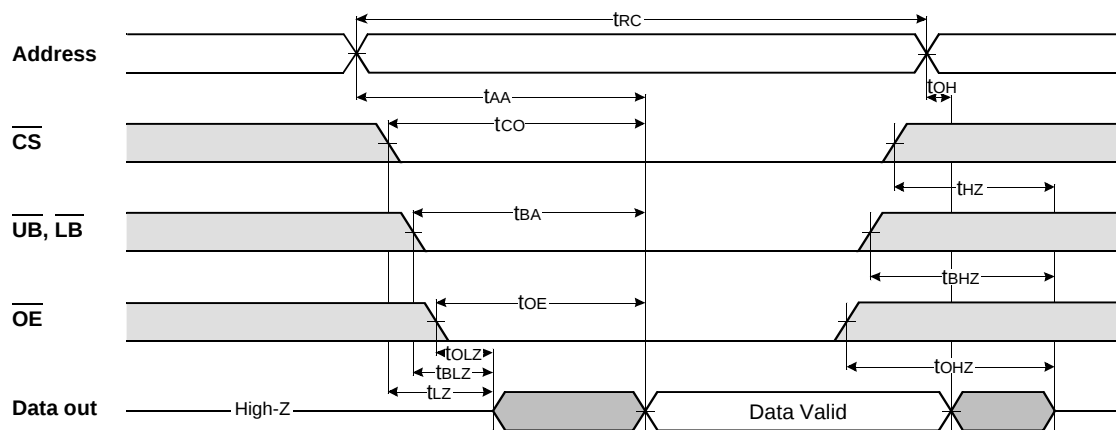
AC CHARACTERISTICS

Parameter List		Symbol	Speed Bins						Units
			55ns		70ns		100ns		
			Min	Max	Min	Max	Min	Max	
Read	Read cycle time	t _{RC}	55	-	70	-	100	-	ns
	Address access time	t _{AA}	-	55	-	70	-	100	ns
	Chip select to output	t _{CO}	-	55	-	70	-	100	ns
	Output enable to valid output	t _{OE}	-	25	-	35	-	50	ns
	$\overline{\text{UB}}, \overline{\text{LB}}$ Access Time	t _{BA}	-	25	-	35	-	50	ns
	Chip select to low-Z output	t _{LZ}	10	-	10	-	10	-	ns
	$\overline{\text{UB}}, \overline{\text{LB}}$ enable to low-Z output	t _{BLZ}	5	-	5	-	5	-	ns
	Output enable to low-Z output	t _{OLZ}	5	-	5	-	5	-	ns
	Chip disable to high-Z output	t _{HZ}	0	20	0	25	0	30	ns
	$\overline{\text{UB}}, \overline{\text{LB}}$ disable to high-Z output	t _{BHZ}	0	20	0	25	0	30	ns
	Output disable to high-Z output	t _{OHZ}	0	20	0	25	0	30	ns
	Output hold from address change	t _{OH}	10	-	15	-	15	-	ns
Write	Write cycle time	t _{WC}	55	-	70	-	100	-	ns
	Chip select to end of write	t _{CW}	45	-	60	-	80	-	ns
	Address set-up time	t _{AS}	0	-	0	-	0	-	ns
	Address valid to end of write	t _{AW}	45	-	60	-	80	-	ns
	Write pulse width	t _{WP}	40	-	50	-	70	-	ns
	$\overline{\text{UB}}, \overline{\text{LB}}$ valid to end of write	t _{BW}	45	-	60	-	80	-	ns
	Write recovery time	t _{WR}	0	-	0	-	0	-	ns
	Write to output high-Z	t _{WHZ}	0	25	0	30	0	35	ns
	Data to write time overlap	t _{DW}	25	-	30	-	40	-	ns
	Data hold from write time	t _{DH}	0	-	0	-	0	-	ns
	End write to output low-Z	t _{OW}	5	-	5	-	5	-	ns

DATA RETENTION CHARACTERISTICS

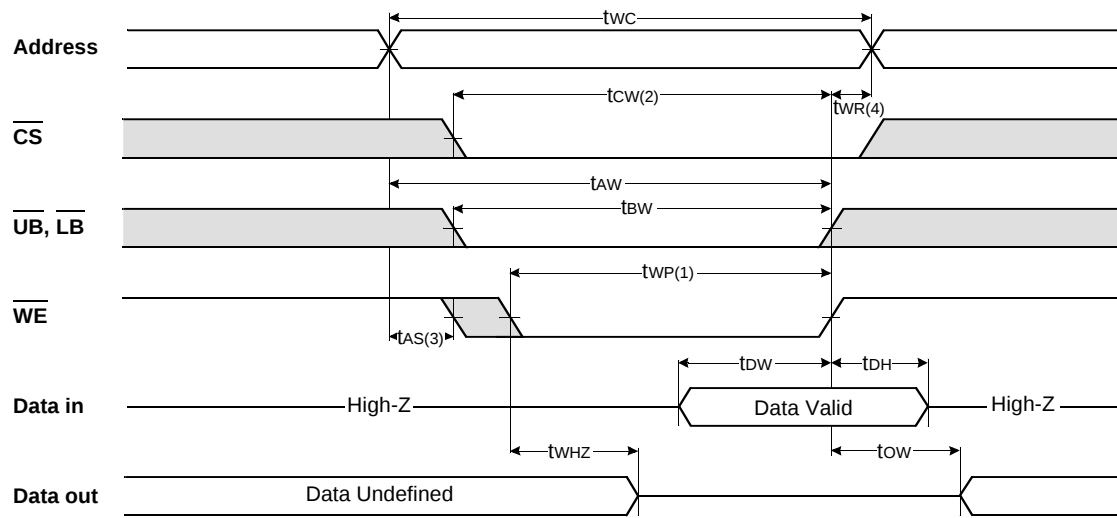
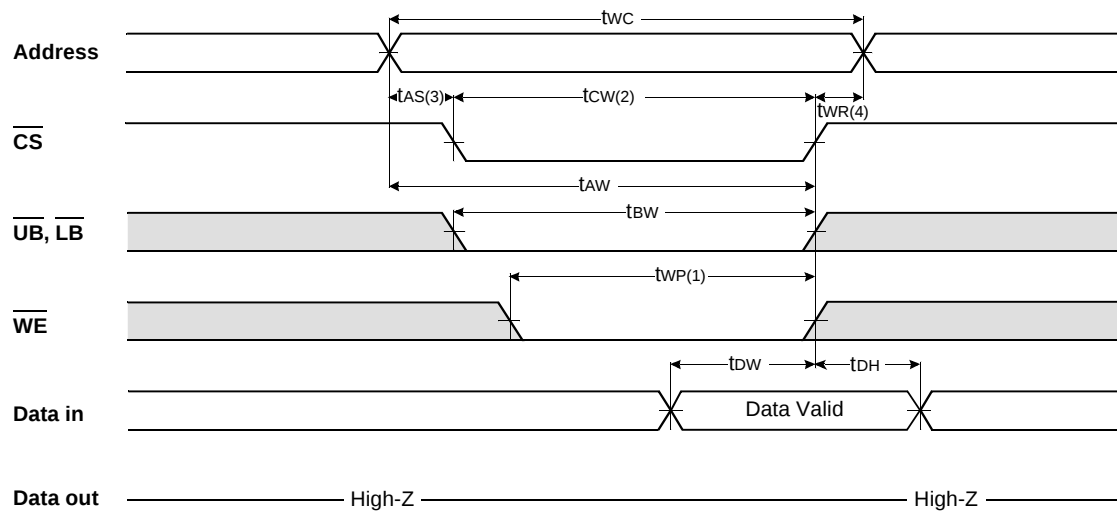
Item	Symbol	Test Condition	Min	Typ	Max	Unit
V _{CC} for data retention	V _{DR}	$\overline{\text{CS}} \geq V_{\text{CC}} - 0.2\text{V}$	2.0	-	5.5	V
Data retention current	I _{DR}	$V_{\text{CC}} = 3.0\text{V}, \overline{\text{CS}} \geq V_{\text{CC}} - 0.2\text{V}$	-	-	15	μA
Data retention set-up time	t _{SDR}	See data retention waveform	0	-	-	ms
Recovery time	t _{RDR}		5	-	-	

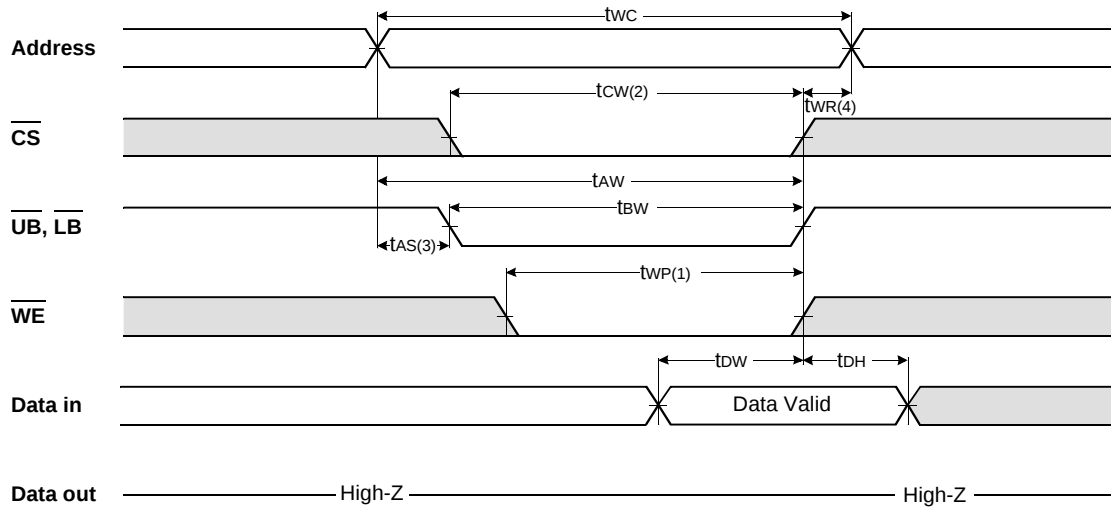
TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}=\overline{OE}=V_{IL}$, $\overline{WE}=V_{IH}$, $\overline{UB}$ or/and $\overline{LB}=V_{IL}$)TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}=V_{IH}$)

NOTES (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, $t_{HZ}(\text{Max.})$ is less than $t_{LZ}(\text{Min.})$ both for a given device and from device to device interconnection.

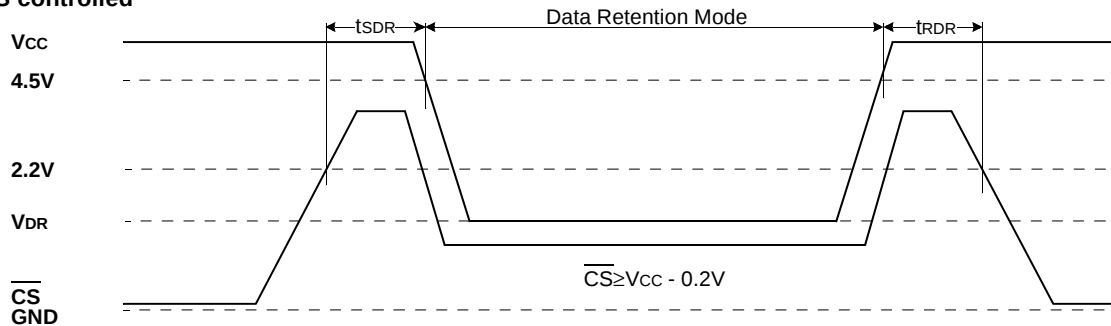
TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{\text{WE}}$ Controlled)TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{\text{CS}}$ Controlled)

TIMING WAVEFORM OF WRITE CYCLE(3) ($\overline{UB}$, $\overline{LB}$ Controlled)

NOTES (WRITE CYCLE)

1. A write occurs during the overlap(t_{WP}) of low $\overline{CS}$ and low $\overline{WE}$. A write begins when $\overline{CS}$ goes low and $\overline{WE}$ goes low with asserting $\overline{UB}$ or $\overline{LB}$ for single byte operation or simultaneously asserting $\overline{UB}$ and $\overline{LB}$ for double byte operation. A write ends at the earliest transition when $\overline{CS}$ goes high and $\overline{WE}$ goes high. The t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the $\overline{CS}$ going low to end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{CS}$ or $\overline{WE}$ going high.

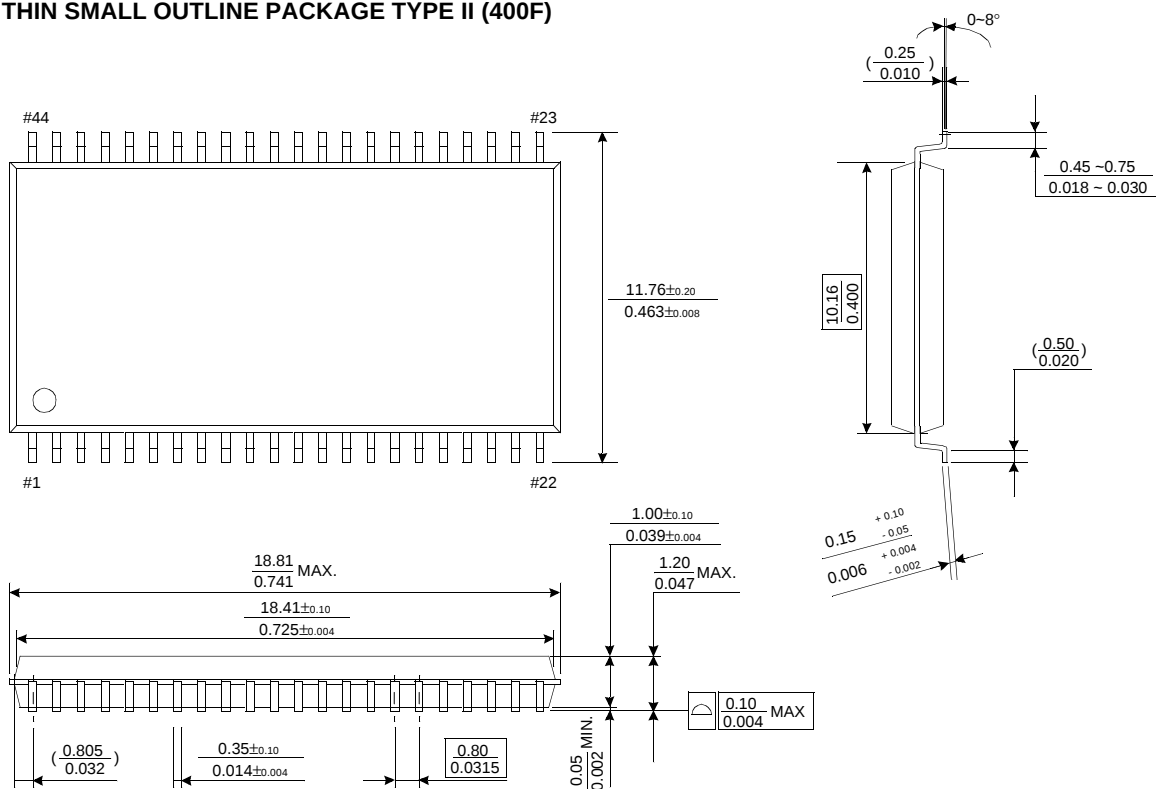
DATA RETENTION WAVE FORM

 $\overline{CS}$ controlled

PACKAGE DIMENSIONS

Unit: millimeter(inch)

44 PIN THIN SMALL OUTLINE PACKAGE TYPE II (400F)



44 PIN THIN SMALL OUTLINE PACKAGE TYPE II (400R)

