ocument Title

128K x16 bit Super Low Power and Low Voltage Full CMOS Static RAM

Revision History

Revision No.	History	Draft Date	Remark
0.0	Design target	October 2, 1996	Advance
0.1	Initial draft - Add KM616FV2000 Family - Erase KM616FU1000 Family and KM616FS1000 Family supprot 2.3~3.3V operating Vcc. - Concept change high power version to low low power version I_{SB1}=10µA(Max) - Add super low power version with special handling I_{SB1}=2.0µA(Max) - Reduce Icc & Icc1 Write : 25mA to 20mA at Vcc=3.6V(Max)	December 1, 1996	Preliminary
1.0	Finalize - Change datasheet format - Erase reverse type package	March 4, 1998	Final
2.0	Revise - Add 48-µBGA type package	May 3, 1999	Final

128Kx16 bit Super Low Power and Low Voltage Full CMOS Static RAM

FEATURES

- Process Technology: Full CMOS
- Organization: 128Kx16
- Power Supply Voltage
  K6F2016V3M Family: 3.0V ~ 3.6V
  K6F2016S3M Family: 2.3V ~ 3.3V
  K6F2016R3M Family: 1.8V ~ 2.7V
- Low Data Retention Voltage: 1.5V(Min)
- Three state output status and TTL Compatible
- Package Type: 44-TSOP2-400F, 48-µBGA-6.20x13.75

GENERAL DESCRIPTION

The K6F2016V3M, K6F2016S3M and K6F2016R3M families are fabricated by SAMSUNG′s advanced Full CMOS process technology. The families support various operating temperature ranges for user flexibility of system design. The families also support low data retention voltage for battery back-up operation with low data retention current.

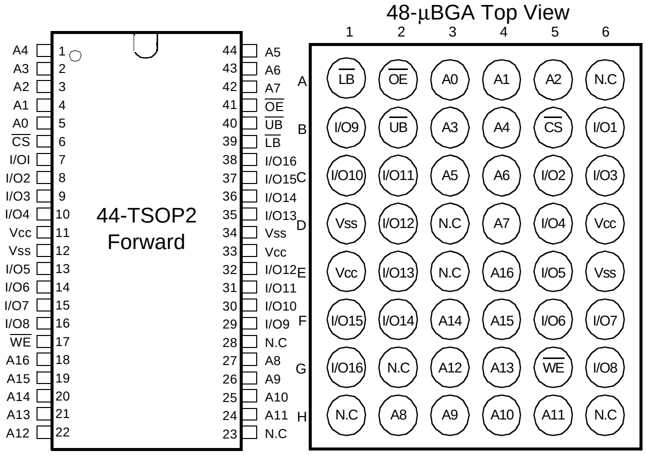
PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed(ns)	Power Dissipation		PKG Type
				Standby (I_{SB1}, Max)	Operating (I_{CC2}, Max)	
K6F2016V3M-C	Commercial(0~70°C)	3.0~3.6V	70[1]/85@V_{CC}=3.3±0.3V	10µA[2]	80mA	44-TSOP2-Forward
K6F2016S3M-C		2.3~3.3V	85@V_{CC}=3.0±0.3V		80mA	
			120[1]/150@V_{CC}=2.5±0.2V		50mA	
K6F2016R3M-C		1.8~2.7V	300[1]@V_{CC}=2.0±0.2V		20mA	
K6F2016V3M-I	Industrial(-40~85°C)	3.0~3.6V	70[1]/85@V_{CC}=3.3±0.3V		80mA	
K6F2016S3M-I		2.3~3.3V	85@V_{CC}=3.0±0.3V		80mA	44-TSOP2 Forward 48-µBGA[3]
			120[1]/150@V_{CC}=2.5±0.2V		50mA	
K6F2016R3M-I		1.8~2.7V	300[1]@V_{CC}=2.0±0.2V		20mA	

1. The parameter is measured with 30pF test load.
2. Super low power product=2µA with special handling.
3. Availiable parts are 100ns@V_{CC}=3.0±0.3V, 150ns@V_{CC}=2.5±0.2V and 300ns@V_{CC}=2.0±0.2V with 30pF test load.

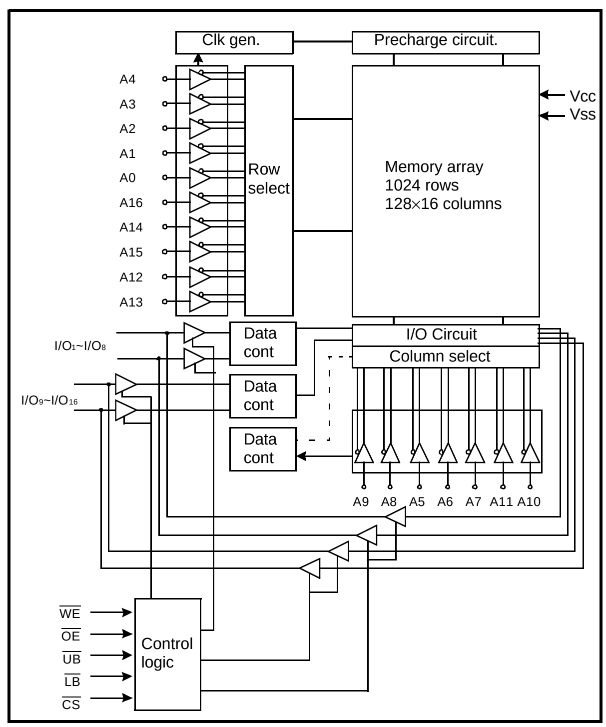
PIN DESCRIPTION

48-µBGA Top View



Name	Function	Name	Function
$\overline{CS}$	Chip Select Input	$\overline{LB}$	Lower Byte(I/O1~8)
$\overline{OE}$	Output Enable Input	$\overline{UB}$	Upper Byte(I/O9~16)
$\overline{WE}$	Write Enable Input	Vcc	Power
A_0~A_{16}	Address Inputs	Vss	Ground
I/O_1~I/O_{16}	Data Inputs/Outputs	N.C.	No Connection

FUNCTIONAL BLOCK DIAGRAM



PRODUCT LIST

Commercial Temperature Products(0~70°C)		Industrial Temperature Products(-40~85°C)	
Part Name	**Function**	**Part Name**	**Function**
K6F2016V3M-TC70	44-TSOP2 F, 70ns, 3.3V, LL	K6F2016V3M-TI70	44-TSOP2 F, 70ns, 3.3V, LL
K6F2016V3M-TC85	44-TSOP2 F, 85ns, 3.3V, LL	K6F2016V3M-TI85	44-TSOP2 F, 85ns, 3.3V, LL
K6F2016S3M-TC12	44-TSOP2 F, 120/85ns, 2.5/3.0V, LL	K6F2016S3M-TI12	44-TSOP2 F, 120/85ns, 2.5/3.0V, LL
K6F2016S3M-TC15	44-TSOP2 F, 150/85ns, 2.5/3.0V, LL	K6F2016S3M-TI15	44-TSOP2 F, 150/85ns, 2.5/3.0V, LL
		K6F2016S3M-ZI15	48-µBGA, 2.5V/3.0V, 150/100ns
K6F2016R3M-TC30	44-TSOP2 F, 300ns, 2.0/2.5V, LL		
		K6F2016R3M-TI30	44-TSOP2 F, 300ns, 2.0/2.5V, LL
		K6F2016R3M-ZI30	48-µBGA, 1.8V/2.5V, 300ns

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	$I/O_{1\sim8}$	$I/O_{9\sim16}$	Mode	Power
H	X[1]	X[1]	X[1]	X[1]	High-Z	High-Z	Deselected	Standby
L	H	H	X[1]	X[1]	High-Z	High-Z	Output Disabled	Active
L	X[1]	X[1]	H	H	High-Z	High-Z	Output Disabled	Active
L	L	H	L	H	Dout	High-Z	Lower Byte Read	Active
L	L	H	H	L	High-Z	Dout	Upper Byte Read	Active
L	L	H	L	L	Dout	Dout	Word Read	Active
L	X[1]	L	L	H	Din	High-Z	Lower Byte Write	Active
L	X[1]	L	H	L	High-Z	Din	Upper Byte Write	Active
L	X[1]	L	L	L	Din	Din	Word Write	Active

1. X means don′t care. (Must be in low or high state)

ABSOLUTE MAXIMUM RATINGS[1]

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	V_{IN},V_{OU}	-0.2 to 3.6V[2]	V	-
Voltage on Vcc supply relative to Vss	V_{CC}	-0.2 to 4.0V[3]	V	-
Power Dissipation	P_D	1.0	W	-
Storage temperature	T_{STG}	-55 to 150	°C	-
Operating Temperature	T_A	0 to 70	°C	K6F2016V3M-C, K6F2016S3M-C, K6F2016R3M-C
		-40 to 85	°C	K6F2016V3M-I, K6F2016S3M-I, K6F2016R3M-I
Soldering temperature and time	T_{SOLDER}	260°C, 5sec (Lead Only)	-	-

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{IN}/V_{OUT}=-0.2 to 3.9V for K6F2016V3M Family.
3. V_{CC}=-0.2 to 4.6V for K6F2016V3M Family

RECOMMENDED DC OPERATING CONDITIONS[1)]

Item	Symbol	Product		Min	Typ	Max	Unit
Supply voltage	Vcc	K6F2016V3M Family		3.0	3.3	3.6	V
		K6F2016S3M Family		2.3	2.5/3.0	3.3	
		K6F2016R3M Family		1.8	2.0/2.5	2.7	
Ground	Vss	All Family		0	0	0	V
Input high voltage	V_{IH}	K6F2016V3M Family	Vcc=3.3±0.3V	2.2	-	Vcc+0.2[2)]	V
		K6F2016S3M Family	Vcc=3.0±0.3V	2.2			
			Vcc=2.5±0.2V	2.0			
		K6F2016R3M Family	Vcc=2.5±0.2V	2.0			
			Vcc=2.0±0.2V	1.6			
Input low voltage	V_{IL}	All Family		-0.2[3)]	-	0.4	V

Note
1 Commercial Product : T_A=0 to 70°C, unless otherwise specified
Industrial Product : T_A=-40 to 85°C, unless otherwise specified
2. Overshoot : Vcc + 1.0V in case of pulse width ≤20ns
3. Undershoot : -1.0V in case of pulse width ≤20ns
4. Overshoot and undershoot are sampled, not 100% tested.

CAPACITANCE[1)] (f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C_{IN}	V_{IN}=0V	-	8	pF
Input/Output capacitance	C_{IO}	V_{IO}=0V	-	10	pF

1. Capacitance is sampled, not 100% tested

DC AND OPERATING CHARACTERISTICS

Item	Symbol	Test Conditions		Min	Typ	Max	Unit
Input leakage current	I_{LI}	V_{IN}=Vss to Vcc		-1	-	1	μA
Output leakage current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, V_{IO}=Vss to Vcc		-1	-	1	μA
Operating power supply current	I_{CC}	I_{IO}=0mA, $\overline{CS}$=V_{IL}, V_{IN}=V_{IL} or V_{IH}, Read		-	-	3	mA
Average operating current	I_{CC1}	Cycle time=1μs, 100% duty, I_{IO}=0mA, $\overline{CS}$≤0.2V, V_{IN}≤0.2V or V_{IN}≥V_{CC}-0.2V	Read	-	-	7	mA
			Write	-	-	20	
	I_{CC2}	Cycle time=Min, 100% duty, I_{IO}=0mA, $\overline{CS}$=V_{IL}, V_{IN}=V_{IL} or V_{IH}	Vcc=3.3V@70ns	-	-	70	mA
			Vcc=2.7V@120ns	-	-	60	
			Vcc=2.2V@300ns	-	-	20	
Output low voltage	V_{OL}	I_{OL}	2.1mA at Vcc=3.0/3.3V	-	-	0.4	V
			0.5mA at Vcc=2.5V	-	-	0.4	
			0.33mA at Vcc=2.0V	-	-	0.4	
Output high voltage	V_{OH}	I_{OH}	-1.0mA at Vcc=3.0/3.3V	2.4	-	-	V
			-0.5mA at Vcc=2.5V	2.0	-	-	
			-0.44mA at Vcc=2.0V	1.6	-	-	
Standby Current(TTL)	I_{SB}	$\overline{CS}$=V_{IH}, Other inputs=V_{IL} or V_{IH}		-	-	0.3	mA
Standby Current(CMOS)	I_{SB1}	$\overline{CS}$≥Vcc-0.2V, Other inputs=0~Vcc		-	-	10[1)]	μA

1. Super low power product=2μA with special handling.

AC OPERATING CONDITIONS

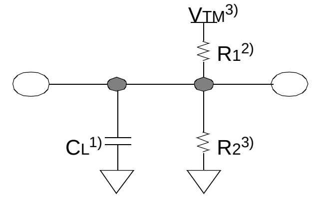
TEST CONDITIONS (Test Load and Test Input/Output Reference)

Input pulse level : 0.4 to 2.2V for Vcc=3.3V, 3.0V, 2.5V
0.4 to 1.8V for Vcc=2.0V

Input rising and falling time : 5ns

Input and output reference voltage : 1.5V for Vcc=3.3V, 3.0V
1.1V for Vcc=2.5V
0.9V for Vcc=2.0V

Output load (See right) : C_L=100pF+1TTL
C_L=30pF+1TTL



1. Including scope and jig capacitance
2. R_1=3070Ω, R_2=3150Ω
3. V_{TM} =2.8V for V_{CC}=3.0/3.3V
=2.3V for V_{CC}=2.5V
=1.8V for V_{CC}=2.0V

AC CHARACTERISTICS

(Commercial product :T_A=0 to 70°C, Industrial product : T_A=-40 to 85°C
K6F2016V3M Family : Vcc=3.0~3.6V, K6F2016S3M Family : Vcc=2.3~3.3V,
K6F2016R3M Family : Vcc=1.8~2.7V)

Parameter List		Symbol	Speed Bins												Units
			70ns		85ns		100ns		120ns		150ns		300ns		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Read	Read cycle time	t_{RC}	70	-	85	-	100	-	120	-	150	-	300	-	ns
	Address access time	t_{AA}	-	70	-	85	-	100	-	120	-	150	-	300	ns
	Chip select to output	t_{CO}	-	70	-	85	-	100	-	120	-	150	-	300	ns
	Output enable to valid output	t_{OE}	-	35	-	45	-	50	-	60	-	75	-	150	ns
	$\overline{UB}$, $\overline{LB}$ Access Time	t_{BA}	-	35	-	45	-	50	-	60	-	75	-	150	ns
	Chip select to low-Z output	t_{LZ}	10	-	10	-	10	-	20	-	20	-	50	-	ns
	Output enable to low-Z output	t_{OLZ}, t_{BLZ}	5	-	5	-	5	-	20	-	20	-	30	-	ns
	Chip disable to high-Z output	t_{HZ}	0	25	0	25	0	30	0	35	0	40	0	60	ns
	Output disable to high-Z output	t_{OHZ}, t_{BHZ}	0	25	0	25	0	30	0	35	0	40	0	60	ns
	Output hold from address change	t_{OH}	10	-	15	-	15	-	15	-	15	-	30	-	ns
Write	Write cycle time	t_{WC}	70	-	85	-	100	-	120	-	150	-	300	-	ns
	Chip select to end of write	t_{CW}	65	-	70	-	80	-	100	-	120	-	300	-	ns
	Address set-up time	t_{AS}	0	-	0	-	0	-	0	-	0	-	0	-	ns
	Address valid to end of write	t_{AW}	65	-	70	-	80	-	100	-	120	-	300	-	ns
	Write pulse width	t_{WP}	55	-	60	-	70	-	80	-	100	-	200	-	ns
	$\overline{UB}$, $\overline{LB}$ Valid to End of Write	t_{BW}	65	-	70	-	80	-	100	-	120	-	300	-	ns
	Write recovery time	t_{WR}	0	-	0	-	0	-	0	-	0	-	0	-	ns
	Write to output high-Z	t_{WHZ}	0	25	0	25	0	30	0	35	0	40	0	60	ns
	Data to write time overlap	t_{DW}	30	-	35	-	40	-	50	-	60	-	120	-	ns
	Data hold from write time	t_{DH}	0	-	0	-	0	-	0	-	0	-	0	-	ns
	End write to output low-Z	t_{OW}	5	-	5	-	5	-	5	-	5	-	20	-	ns

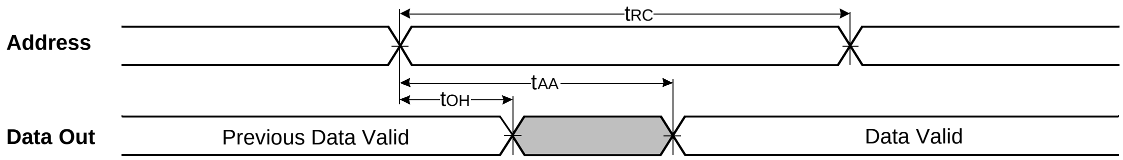
DATA RETENTION CHARACTERISTICS

Item	Symbol	Test Condition	Min	Typ	Max	Unit
Vcc for data retention	V_{DR}	$\overline{CS}$≥Vcc-0.2V	1.5	-	3.6	V
Data retention current	I_{DR}	Vcc=3.0V, $\overline{CS}$≥Vcc-0.2V	-	-	10[1]	µA
Data retention set-up time	t_{SDR}	See data retention waveform	0	-	-	ns
Recovery time	t_{RDR}		t_{RC}	-	-	

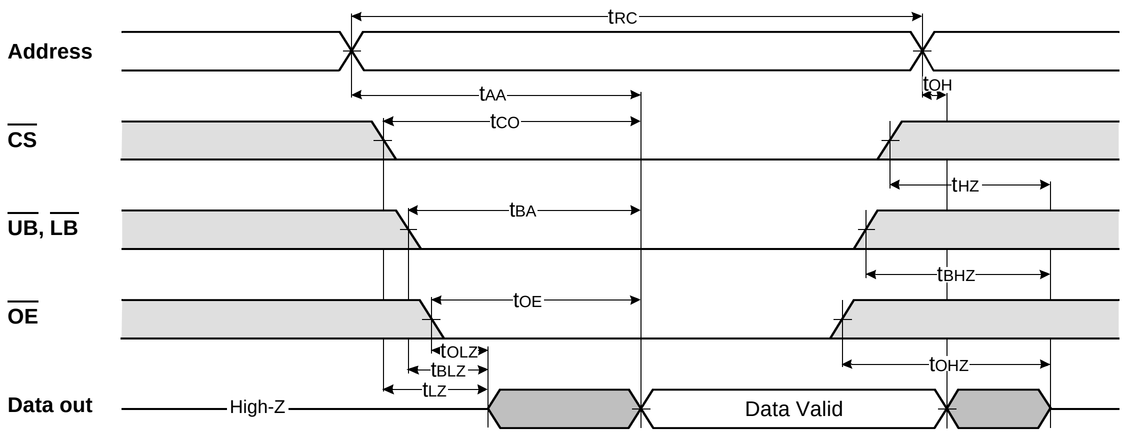
1. Super low power product=2µA with special handling.

TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}=\overline{OE}=V_{IL}$, $\overline{WE}=V_{IH}$, $\overline{UB}$ or/and $\overline{LB}=V_{IL}$)



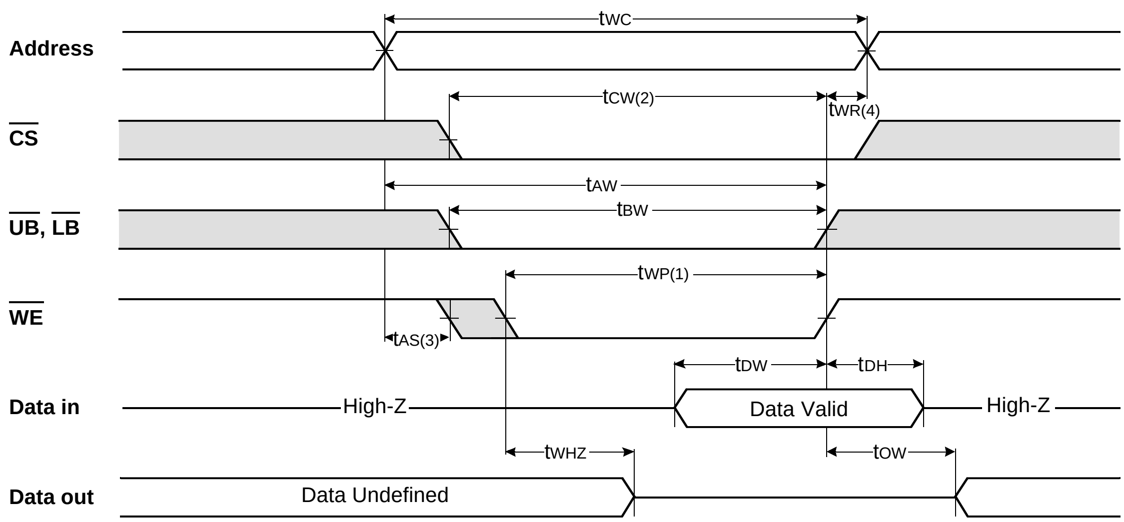
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}=V_{IH}$)



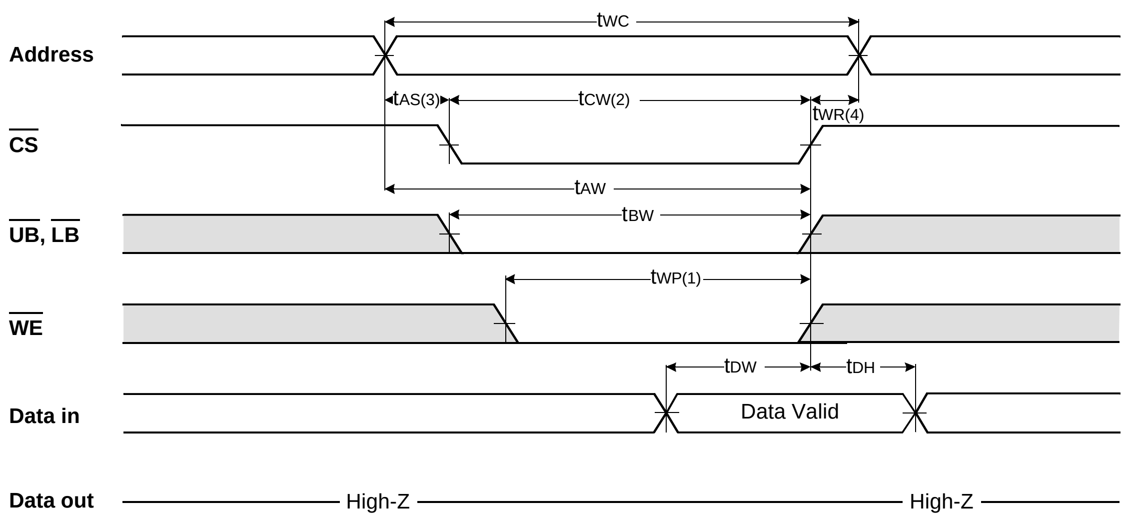
NOTES (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, t_{HZ}(Max.) is less than t_{LZ}(Min.) both for a given device and from device to device interconnection.

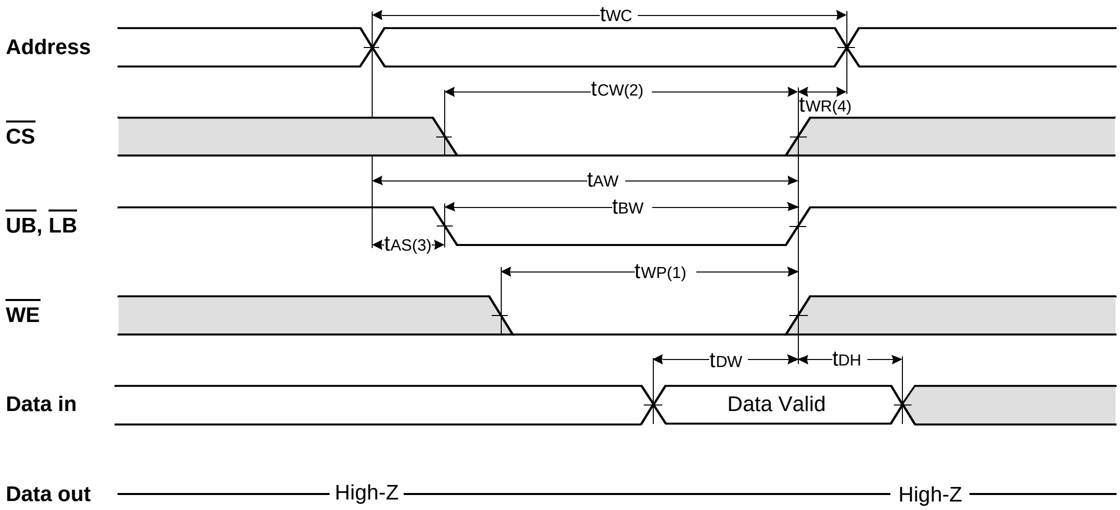
TIMING WAVEFORM OF WRITE CYCLE(1) (WE Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) (CS Controlled)



TIMING WAVEFORM OF WRITE CYCLE(3) ($\overline{UB}$, $\overline{LB}$ Controlled)

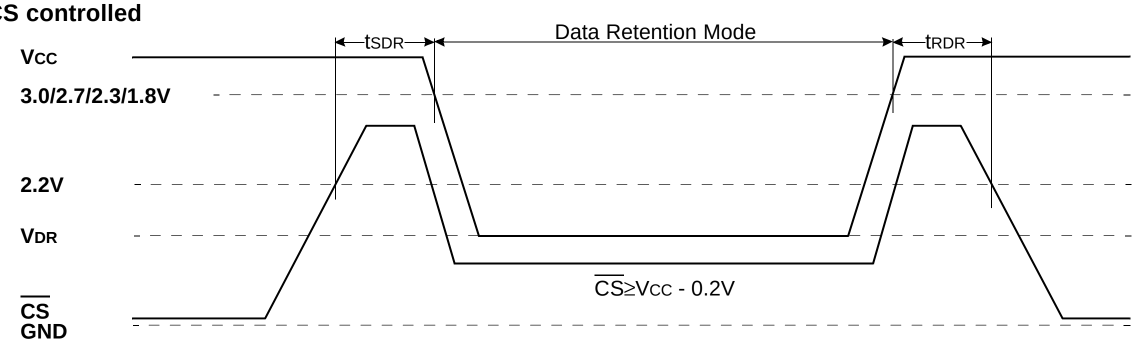


NOTES (WRITE CYCLE)

1. A write occurs during the overlap(t_{WP}) of low $\overline{CS}$ and low $\overline{WE}$. A write begins when $\overline{CS}$ goes low and $\overline{WE}$ goes low with asserting $\overline{UB}$ or $\overline{LB}$ for single byte operation or simultaneously asserting $\overline{UB}$ and $\overline{LB}$ for double byte operation. A write ends at the earliest transition when $\overline{CS}$ goes high and $\overline{WE}$ goes high. The t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the $\overline{CS}$ going low to end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end or write to the address change. t_{WR} applied in case a write ends as $\overline{CS}$ or $\overline{WE}$ going high.

DATA RETENTION WAVE FORM

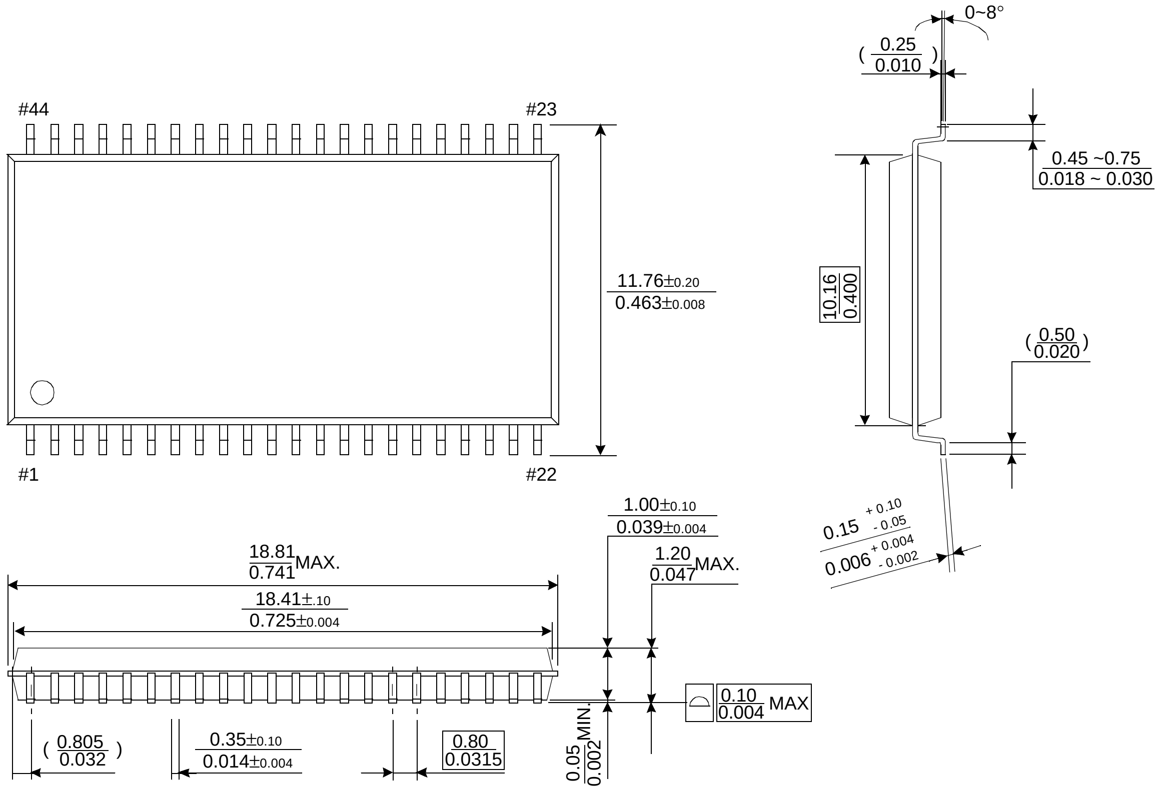
$\overline{CS}$ controlled



PACKAGE DIMENSIONS

Units: millimeters(inches)

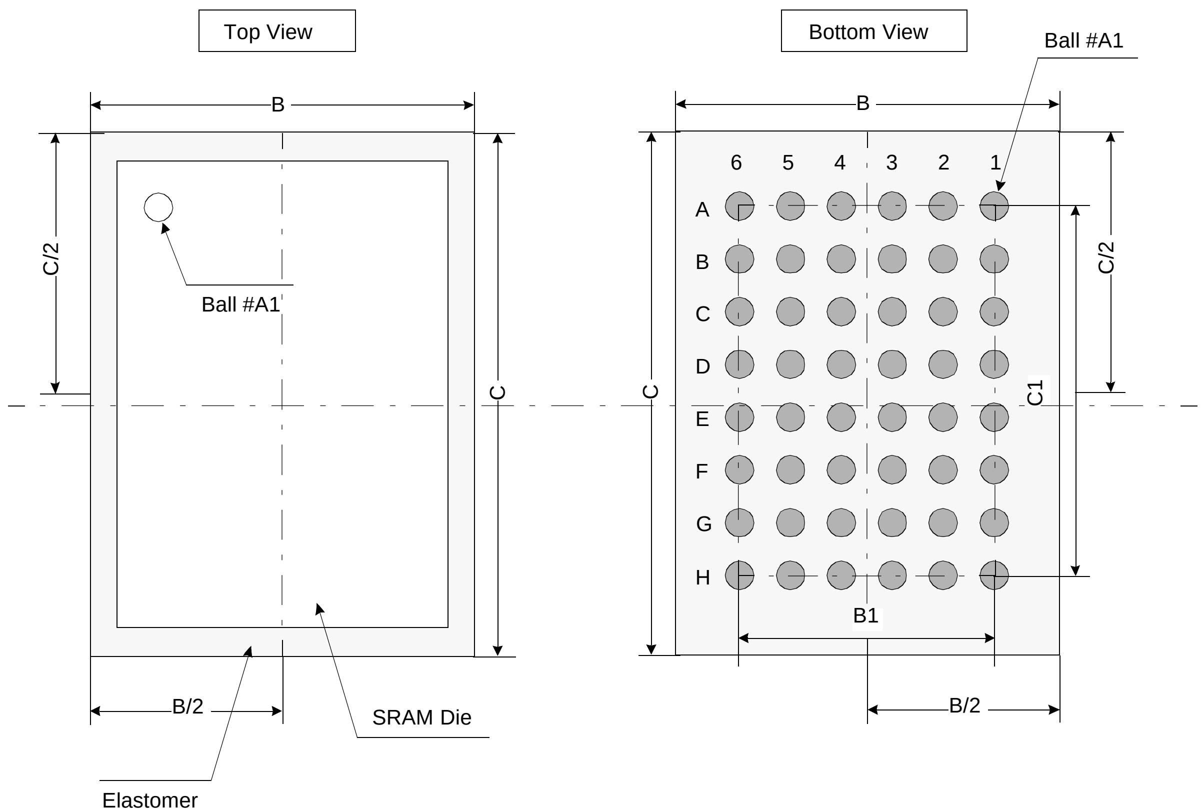
44 PIN THIN SMALL OUTLINE PACKAGE TYPE II (400F)

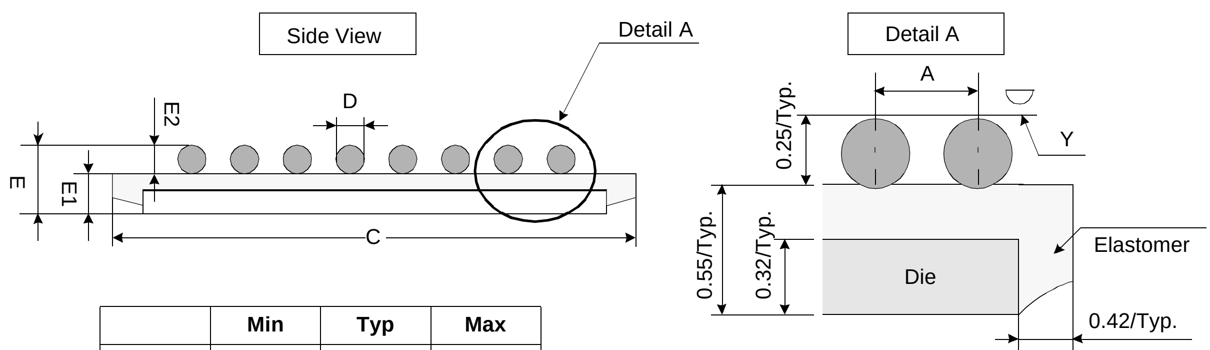


PACKAGE DIMENSIONS

Units: millimeters

48 BALL MICRO BALL GRID ARRAY- 0.75mm ball pitch





	Min	Typ	Max
A	-	0.75	-
B	5.90	6.20	6.10
B1	-	3.75	-
C	7.90	13.75	8010
C1	-	5.25	-
D	0.30	0.35	0.40
E	-	0.80	0.81
E1	-	0.55	-
E2	-	0.25	-
Y	-	-	0.08

<u>Notes.</u>

1. Bump counts: 48(8row x 6column)
2. Bump pitch: (x,y)=(0.75 x 0.75)(typ.)
3. All tolerence are +/-0.050 unless otherwise specified.
4. Typ: Typical
5. Y is coplanarity: 0.08(Max)