

Document Title**64Kx4 Bit (with OE) High Speed Static RAM(5V Operating).****Revision History**

<u>RevNo.</u>	<u>History</u>	<u>Draft Data</u>	<u>Remark</u>
Rev. 0.0	Initial release with Preliminary.	Aug. 1. 1998	Preliminary
Rev. 1.0	Release to Final Data Sheet.	Nov. 2. 1998	Final

The attached data sheets are prepared and approved by SAMSUNG Electronics. SAMSUNG Electronics CO., LTD. reserve the right to change the specifications. SAMSUNG Electronics will evaluate and reply to your requests and questions on the parameters of this device. If you have any questions, please contact the SAMSUNG branch office near your office, call or contact Headquarters.

FEATURES

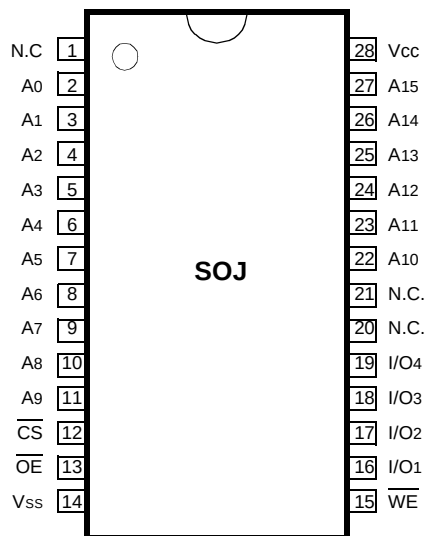
- Fast Access Time 10,12,15ns(Max.)
- Low Power Dissipation
 - Standby (TTL) : 20mA(Max.)
 - (CMOS) : 2mA(Max.)
 - Operating K6E0804C1E-10 : 70mA(Max.)
 - K6E0804C1E-12 : 70mA(Max.)
 - K6E0804C1E-15 : 70mA(Max.)
- Single 5.0V±10% Power Supply
- TTL Compatible Inputs and Outputs
- I/O Compatible With 3.3V Device
- Fully Static Operation
 - No Clock or Refresh required
- Three State Outputs
- Standard Pin Configuration
 - K6E0804C1E-J : 28-SOJ-300

The K6E0804C1E is a 262,144-bit high-speed Static Random Access Memory organized as 65,536 words by 4 bits. The K6E0804C1E uses 4 common input and output lines and has an output enable pin which operates faster than address access time at read cycle. The device is fabricated using SAM-SUNG's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The K6E0804C1E is packaged in a 300 mil 28-pin plastic SOJ.

PIN CONFIGURATION_(Top View)

The diagram illustrates a DRAM architecture with the following components and connections:

- Row Select:** Receives address inputs A_0 through A_8 and is connected to the **Memory Array**.
- Memory Array:** A 512 Rows by 128x4 Columns array.
- Pre-Charge-Circuit:** Connected to the top of the Memory Array.
- Data Cont.:** Connected to the Memory Array and the **I/O Circuit**.
- I/O Circuit:** Contains a **Column Select** block and is connected to the Memory Array and the **Data Cont.**
- CLK Gen.:** Two clock generators are present. One is connected to the **Row Select** and the **Data Cont.**. The other is connected to the **I/O Circuit** and the **Data Cont.**.
- Control Signals:** $\overline{CS}$, $\overline{WE}$, and $\overline{OE}$ are inputs. $\overline{CS}$ and $\overline{WE}$ are connected to an AND gate. $\overline{WE}$ and $\overline{OE}$ are connected to another AND gate. The output of the first AND gate is connected to the **Row Select**. The output of the second AND gate is connected to the **I/O Circuit**.



Pin Name	Pin Function
A ₀ - A ₁₅	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
I/O ₁ ~ I/O ₄	Data Inputs/Outputs
V _{CC}	Power(+5.0V)
V _{SS}	Ground
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	V _{IN} , V _{OUT}	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss	V _{CC}	-0.5 to 7.0	V
Power Dissipation	P _D	1.0	W
Storage Temperature	T _{STG}	-65 to 150	°C
Operating Temperature	T _A	0 to 70	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS(T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{CC}	4.5	5.0	5.5	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.2	-	V _{CC} +0.5**	V
Input Low Voltage	V _{IL}	-0.5*	-	0.8	V

* V_{IL}(Min) = -2.0(Pulse Width ≤ 7ns) for I ≤ 20mA

** V_{IH}(Max) = V_{CC}+2.0V(Pulse Width ≤ 7ns) for I ≤ 20mA

DC AND OPERATING CHARACTERISTICS(T_A=0 to 70°C, V_{CC}=5.0V±10% unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	I _{LI}	V _{IN} = V _{SS} to V _{CC}		-2	2	μA
Output Leakage Current	I _{LO}	$\overline{CS}=V_{IH}$ or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$ V _{OUT} = V _{SS} to V _{CC}		-2	2	μA
Operating Current	I _{CC}	Min. Cycle, 100% Duty $\overline{CS}=V_{IL}$, V _{IN} = V _{IH} or V _{IL} , I _{OUT} =0mA	10ns	-	70	mA
			12ns	-	70	
			15ns	-	70	
Standby Current	I _{SB}	Min. Cycle, $\overline{CS}=V_{IH}$		-	20	mA
	I _{SB1}	f=0MHz, $\overline{CS} \geq V_{CC}-0.2V$, V _{IN} ≥V _{CC} -0.2V or V _{IN} ≤0.2V		-	2	mA
Output Low Voltage Level	V _{OL}	I _{OL} =8mA		-	0.4	V
Output High Voltage Level	V _{OH}	I _{OH} =-4mA		2.4	-	V
	V _{OH1} *	I _{OH1} =0.1mA		-	3.95	V

* V_{CC}=5.0V±5%, Temp.=25°C

CAPACITANCE*(T_A=25°C, f=1.0MHz)

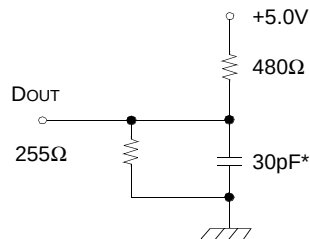
Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	C _{I/O}	V _{I/O} =0V	-	8	pF
Input Capacitance	C _{IN}	V _{IN} =0V	-	7	pF

* Capacitance is sampled and not 100% tested.

AC CHARACTERISTICS($T_A=0$ to 70°C , $V_{CC}=5.0\text{V}\pm 10\%$, unless otherwise noted.)**TEST CONDITIONS**

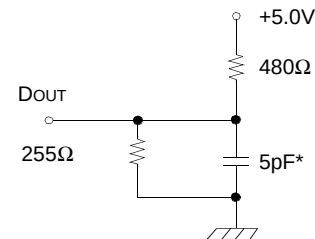
Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

Output Loads(A)



Output Loads(B)

for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ



* Including Scope and Jig Capacitance

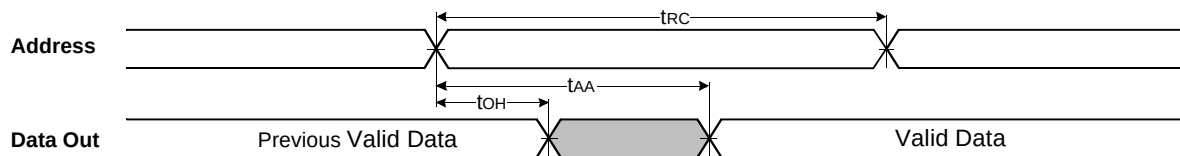
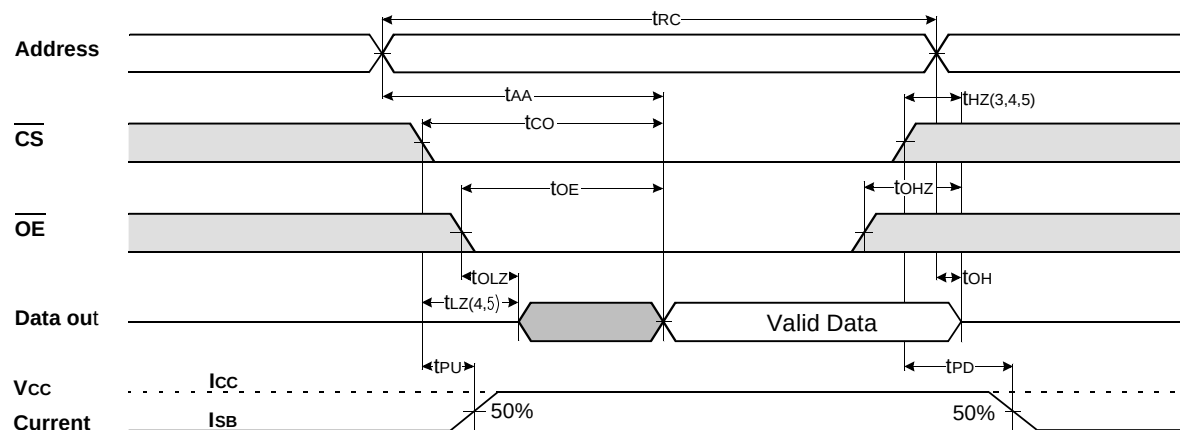
READ CYCLE

Parameter	Symbol	K6E0804C1E-10		K6E0804C1E-12		K6E0804C1E-15		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t _{RC}	10	-	12	-	15	-	ns
Address Access Time	t _{AA}	-	10	-	12	-	15	ns
Chip Select to Output	t _{CO}	-	10	-	12	-	15	ns
Output Enable to Valid Output	t _{OE}	-	5	-	6	-	7	ns
Chip Enable to Low-Z Output	t _{LZ}	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	t _{OLZ}	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	t _{HZ}	0	5	0	6	0	7	ns
Output Disable to High-Z Output	t _{OHZ}	0	5	0	6	0	7	ns
Output Hold from Address Change	t _{OH}	3	-	3	-	3	-	ns
Chip Selection to Power Up Time	t _{PU}	0	-	0	-	0	-	ns
Chip Selection to Power DownTime	t _{PD}	-	10	-	12	-	15	ns

WRITE CYCLE

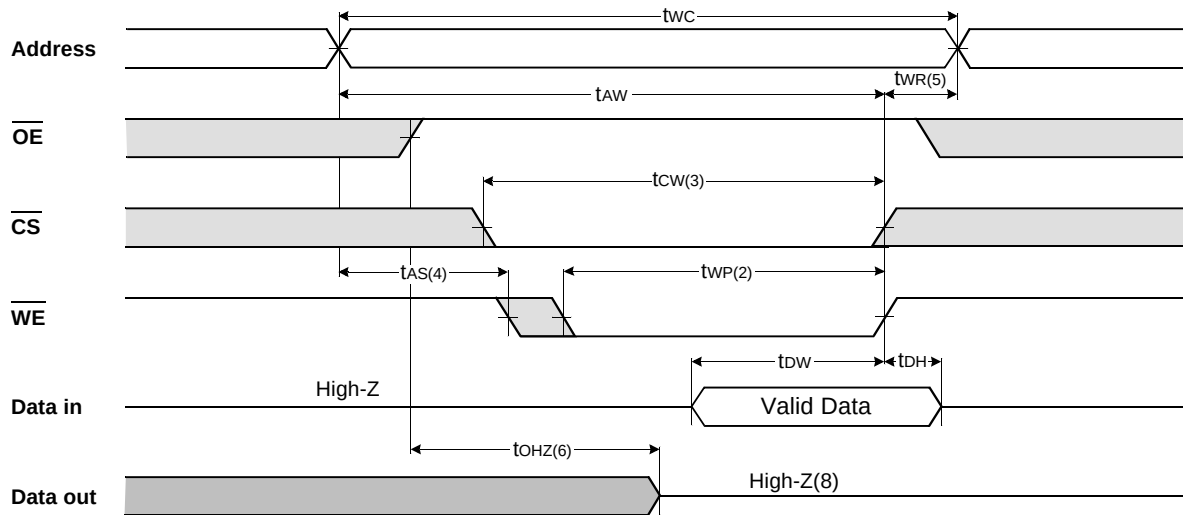
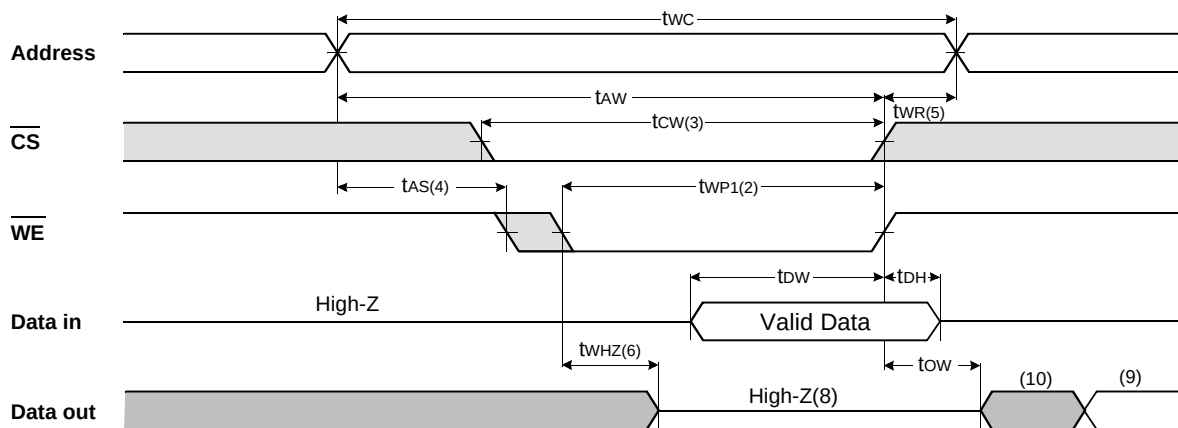
Parameter	Symbol	K6E0804C1E-10		K6E0804C1E-12		K6E0804C1E-15		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t _{WC}	10	-	12	-	15	-	ns
Chip Select to End of Write	t _{CW}	8	-	9	-	10	-	ns
Address Setup Time	t _{AS}	0	-	0	-	0	-	ns
Address Valid to End of Write	t _{AW}	8	-	9	-	10	-	ns
Write Pulse Width($\overline{\text{OE}}$ High)	t _{WP}	8	-	9	-	10	-	ns
Write Pulse Width($\overline{\text{OE}}$ Low)	t _{WP1}	10	-	12	-	15	-	ns
Write Recovery Time	t _{WR}	0	-	0	-	0	-	ns
Write to Output High-Z	t _{WHZ}	0	5	0	6	0	7	ns
Data to Write Time Overlap	t _{DW}	5	-	6	-	7	-	ns
Data Hold from Write Time	t _{DH}	0	-	0	-	0	-	ns
End Write to Output Low-Z	t _{OW}	0	-	0	-	0	-	ns

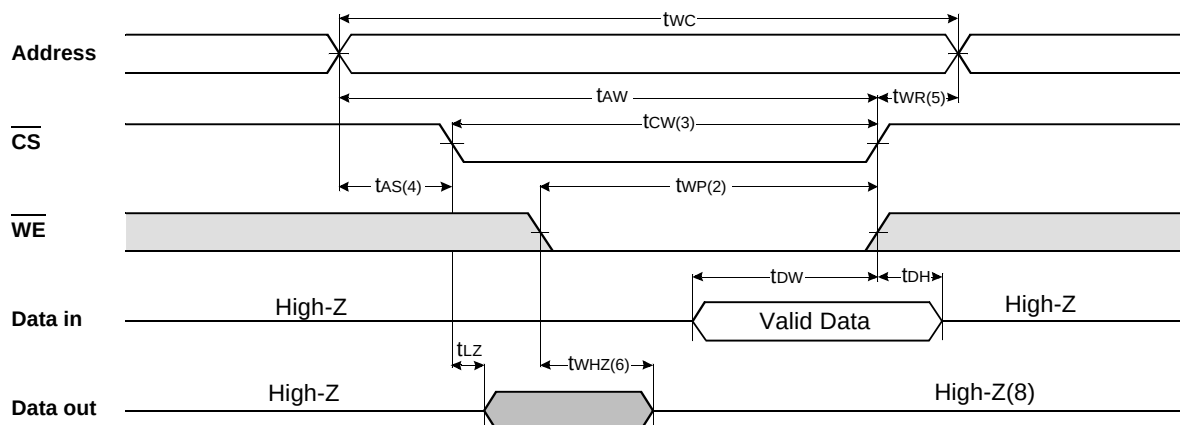
TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{\text{CS}}=\overline{\text{OE}}=V_{\text{IL}}$, $\overline{\text{WE}}=V_{\text{IH}}$)TIMING WAVEFORM OF READ CYCLE(2) ($\overline{\text{WE}}=V_{\text{IH}}$)

NOTES(READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referenced to V_{OH} or V_{OL} levels.
4. At any given temperature and voltage condition, $t_{HZ}(\text{Max.})$ is less than $t_{LZ}(\text{Min.})$ both for a given device and from device to device.
5. Transition is measured $\pm 200\text{mV}$ from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}=V_{IL}$.
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{OE}$ = Clock)TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{OE}$ =Low Fixed)

TIMING WAVEFORM OF WRITE CYCLE(3) ($\overline{\text{CS}}$ =Controlled)

NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{\text{CS}}$ and $\overline{\text{WE}}$. A write begins at the latest transition $\overline{\text{CS}}$ going low and $\overline{\text{WE}}$ going low; A write ends at the earliest transition $\overline{\text{CS}}$ going high or $\overline{\text{WE}}$ going high. t_{WP} is measured from the beginning of write to the end of write.
3. t_{CW} is measured from the later of $\overline{\text{CS}}$ going low to end of write.
4. t_{AS} is measured from the address valid to the beginning of write.
5. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{\text{CS}}$ or $\overline{\text{WE}}$ going high.
6. If $\overline{\text{OE}}$, $\overline{\text{CS}}$ and $\overline{\text{WE}}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{\text{CS}}$ goes low simultaneously with $\overline{\text{WE}}$ going or after $\overline{\text{WE}}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{\text{CS}}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

$\overline{\text{CS}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	Mode	I/O Pin	Supply Current
H	X	X*	Not Select	High-Z	I_{SB} , I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	DOUT	I_{CC}
L	L	X	Write	DIN	I_{CC}

* X means Don't Care.

PACKAGE DIMENSIONS

Units: millimeters/Inches

28-SOJ-300

