KS0716

33 COM / 100 SEG DRIVER & CONTROLLER FOR STN LCD

January.2000

Ver. 3.0

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KS0716 Specification Revision History		
Version	**Content**	**Date**
0.0		
1.0	COM PAD NAME modify (reference PAD Center Coordinate) Reference voltage [V_{REF1}]: 2.0V -> 2.1V (reference DC Characteristics)	
2.0	Reference voltage is only fixed V_{REF} = 2.1V	Mar.1999
2.1	Reference voltage could be used both V_{REF} = 1.9V and V_{REF} = 2.1V	May.1999
3.0	Change VDD Range : 2.4V to 5.5V $\rightarrow$ 2.4V to 3.6V	Jan.2000

CONTENTS

INTRODUCTION

The KS0716 is a driver & controller LSI for graphic dot-matrix liquid crystal display systems. It contains 33 common and 100 segment driver circuits. This chip is connected directly to a microprocessor, accepts serial or 8-bit parallel display data and stores in an on-chip display data RAM of 65 x 132 bits. It provides a highly-flexible display section due to 1-to-1 correspondence between on-chip display data RAM bits and LCD panel pixels. And it performs display data RAM read/write operation with no external operating clock to minimize power consumption. In addition, because it contains power supply circuits necessary to drive liquid crystal, it is possible to make a display system with the fewest components.

FEATURES

Driver Output Circuits

– 33 common outputs / 100 segment outputs

On-chip Display Data RAM

– Capacity: 65 x 132 = 8,580 bits
– Bit data "1": a dot of display is illuminated
– Bit data "0": a dot of display is not illuminated

Multi-chip Operation (Master, Slave) Available

Applicable Duty-ratios

Duty ratio	Applicable LCD bias	Maximum display area
1/33	1/5 or 1/6	33 × 100

Microprocessor Interface

– 8-bit parallel bi-directional interface with 6800-series or 8080-series
– Serial interface (only write operation) available

Various Instruction Setting

On-chip Oscillator Circuit

On-chip Low Power Supply for LCD Driving Voltage Generation

– Voltage converter (x2, x3, x4)
– Voltage regulator (Temperature coefficient: -0.05%/°C, -0.2%/°C)
– Voltage follower (LCD Bias: 1/5 or 1/6)

On-chip Electronic Contrast Control Function (32 steps)

Operating Voltage Range

– Supply voltage (V_{DD}): 2.4 to 3.6 V
– LCD driving voltage (V_{LCD} = V0 - V_{SS}): 4.0 to 15.0 V

Low Power Consumption

– 100 μA Typ. (V_{DD} = 3V, x4 boosting, V0 = 8V, Internal power supply ON and display OFF)
– 10 μA Max. (standby mode)

Wide Operating Temperature Range

– Ta = -40°C to +85°C

CMOS Process

Package Type

– Bare die for COB

Series Specifications

Product code	TEMPS pin	Temp. coefficient	Package	Chip thickness
KS0716P-L3CC	0 (V_{SS} connected)	-0.05%/°C	COB	300 µm
KS0716P-H3CC	1 (V_{DD} connected)	-0.2%/°C		300 µm

BLOCK DIAGRAM

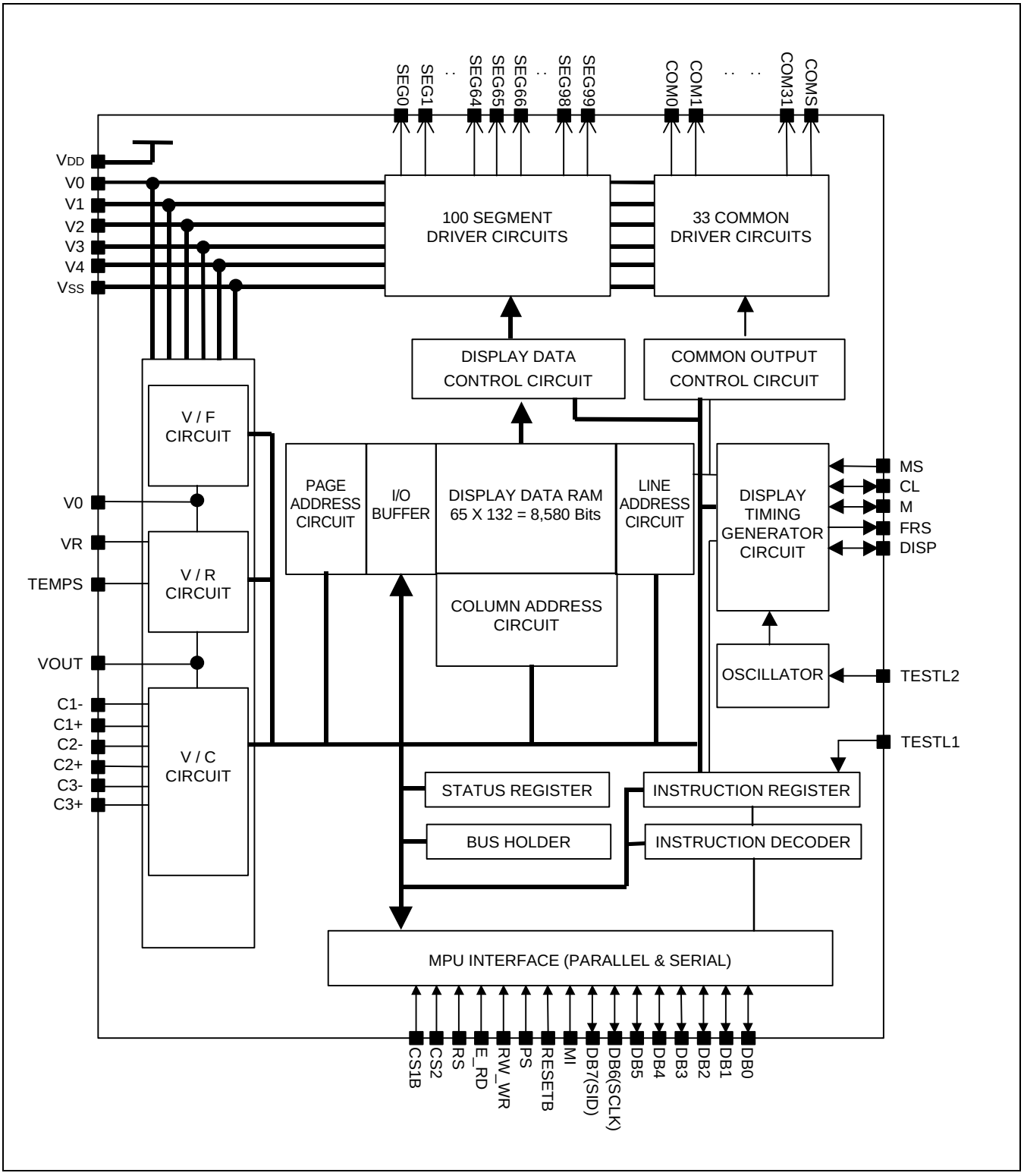

Figure 1. Block Diagram

PAD CONFIGURATION

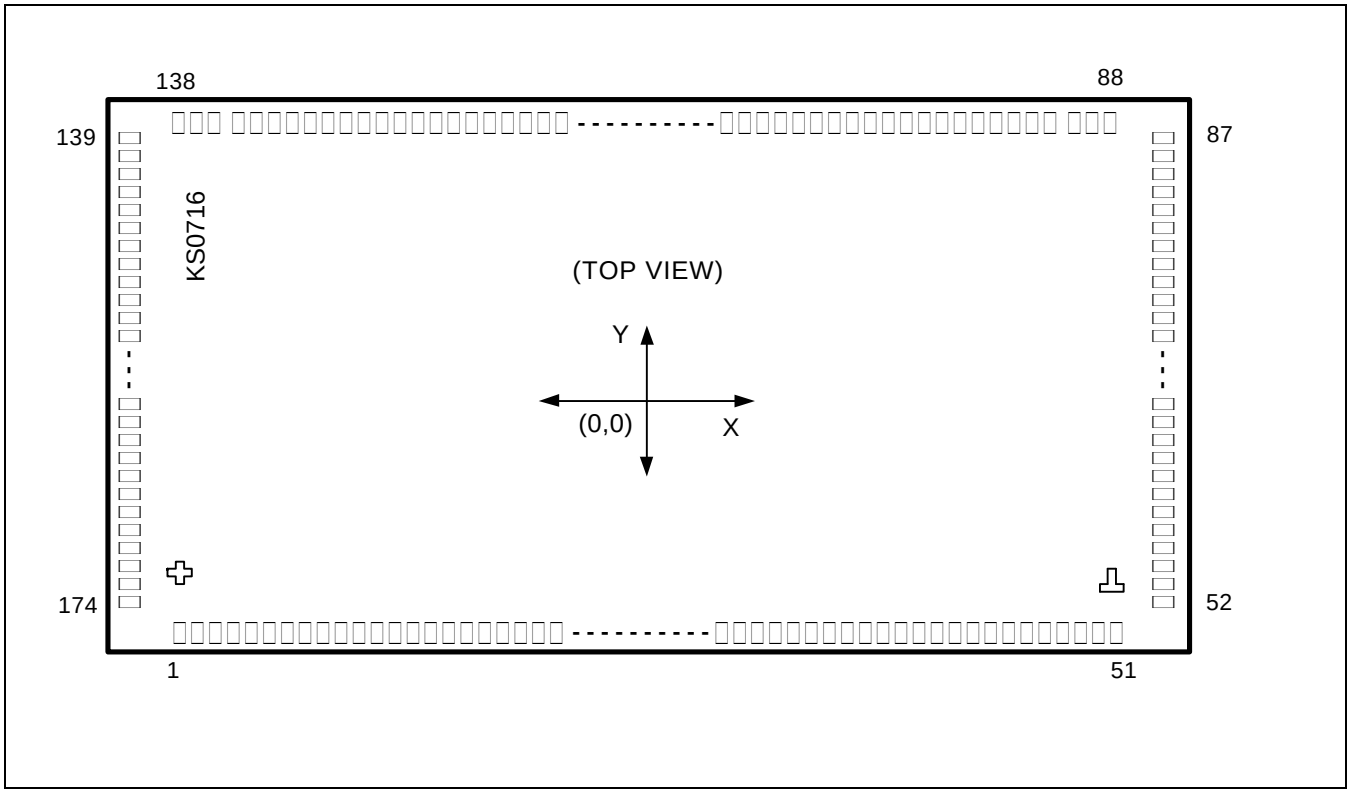

Figure 2. KS0716 Chip Configuration

Table 1. KS0716 Pad Dimensions

Item	Pad No.	Size		Unit
		X	Y	
Chip size	-	5950	4300	μm
Pad pitch	All pad	110		
Pad center size	All pad	90 x 90		
Chip thickness	-	300		

PAD CENTER COORDINATES

Table 2. Pad Center Coordinates

[Unit: μm]

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
1	COM28	-2750	-2046	51	COM11	2750	-2046	101	SEG38	1320	2046
2	COM29	-2640	-2046	52	COM10	2871	-1925	102	SEG39	1210	2046
3	COM30	-2530	-2046	53	COM9	2871	-1815	103	SEG40	1100	2046
4	COM31	-2420	-2046	54	COM8	2871	-1705	104	SEG41	990	2046
5	COMS	-2310	-2046	55	COM7	2871	-1595	105	SEG42	880	2046
6	TESTL1	-2200	-2046	56	COM6	2871	-1485	106	SEG43	770	2046
7	FRS	-2090	-2046	57	COM5	2871	-1375	107	SEG44	660	2046
8	M	-1980	-2046	58	COM4	2871	-1265	108	SEG45	550	2046
9	CL	-1870	-2046	59	COM3	2871	-1155	109	SEG46	440	2046
10	DISP	-1760	-2046	60	COM2	2871	-1045	110	SEG47	330	2046
11	MS	-1650	-2046	61	COM1	2871	-935	111	SEG48	220	2046
12	RESETB	-1540	-2046	62	COM0	2871	-825	112	SEG49	110	2046
13	PS	-1430	-2046	63	SEG0	2871	-715	113	SEG50	0	2046
14	CS1B	-1320	-2046	64	SEG1	2871	-605	114	SEG51	-110	2046
15	CS2	-1210	-2046	65	SEG2	2871	-495	115	SEG52	-220	2046
16	MI	-1100	-2046	66	SEG3	2871	-385	116	SEG53	-330	2046
17	RS	-990	-2046	67	SEG4	2871	-275	117	SEG54	-440	2046
18	RW_WR	-880	-2046	68	SEG5	2871	-165	118	SEG55	-550	2046
19	E_RD	-770	-2046	69	SEG6	2871	-55	119	SEG56	-660	2046
20	VDD	-660	-2046	70	SEG7	2871	55	120	SEG57	-770	2046
21	DB0	-550	-2046	71	SEG8	2871	165	121	SEG58	-880	2046
22	DB1	-440	-2046	72	SEG9	2871	275	122	SEG59	-990	2046
23	DB2	-330	-2046	73	SEG10	2871	385	123	SEG60	-1100	2046
24	DB3	-220	-2046	74	SEG11	2871	495	124	SEG61	-1210	2046
25	DB4	-110	-2046	75	SEG12	2871	605	125	SEG62	-1320	2046
26	DB5	0	-2046	76	SEG13	2871	715	126	SEG63	-1430	2046
27	DB6	110	-2046	77	SEG14	2871	825	127	SEG64	-1540	2046
28	DB7	220	-2046	78	SEG15	2871	935	128	SEG65	-1650	2046
29	VSS	330	-2046	79	SEG16	2871	1045	129	SEG66	-1760	2046
30	VOUT	440	-2046	80	SEG17	2871	1155	130	SEG67	-1870	2046
31	CAP3P	550	-2046	81	SEG18	2871	1565	131	SEG68	-1980	2046
32	CAP3M	660	-2046	82	SEG19	2871	1375	132	SEG69	-2090	2046
33	CAP1P	770	-2046	83	SEG20	2871	1485	133	SEG70	-2200	2046
34	CAP1M	880	-2046	84	SEG21	2871	1595	134	SEG71	-2310	2046
35	CAP2P	990	-2046	85	SEG22	2871	1705	135	SEG72	-2420	2046
36	CAP2M	1100	-2046	86	SEG23	2871	1815	136	SEG73	-2530	2046
37	V0	1210	-2046	87	SEG24	2871	1925	137	SEG74	-2640	2046
38	VR	1320	-2046	88	SEG25	2750	2046	138	SEG75	-2750	2046
39	VSS	1430	-2046	89	SEG26	2640	2046	139	SEG76	-2871	1925
40	V1	1540	-2046	90	SEG27	2530	2046	140	SEG77	-2871	1815
41	V2	1650	-2046	91	SEG28	2420	2046	141	SEG78	-2871	1705
42	V3	1760	-2046	92	SEG29	2310	2046	142	SEG79	-2871	1595
43	V4	1870	-2046	93	SEG30	2200	2046	143	SEG80	-2871	1485
44	V0	1980	-2046	94	SEG31	2090	2046	144	SEG81	-2871	1375
45	TEMPS	2090	-2046	95	SEG32	1980	2046	145	SEG82	-2871	1265
46	TESTL2	2200	-2046	96	SEG33	1870	2046	146	SEG83	-2871	1155
47	COM15	2310	-2046	97	SEG34	1760	2046	147	SEG84	-2871	1045
48	COM14	2420	-2046	98	SEG35	1650	2046	148	SEG85	-2871	935
49	COM13	2530	-2046	99	SEG36	1540	2046	149	SEG86	-2871	825
50	COM12	2640	-2046	100	SEG37	1430	2046	150	SEG87	-2871	715

Table 2. Pad Center Coordinates (Continued)

[Unit: μm]

NO.	Name	X	Y	NO.	Name	X	Y	NO.	Name	X	Y
151	SEG88	-2871	605								
152	SEG89	-2871	495								
153	SEG90	-2871	385								
154	SEG91	-2871	275								
155	SEG92	-2871	165								
156	SEG93	-2871	55								
157	SEG94	-2871	-55								
158	SEG95	-2871	-165								
159	SEG96	-2871	-275								
160	SEG97	-2871	-385								
161	SEG98	-2871	-495								
162	SEG99	-2871	-605								
163	COM16	-2871	-715								
164	COM17	-2871	-825								
165	COM18	-2871	-935								
166	COM19	-2871	-1045								
167	COM20	-2871	-1155								
168	COM21	-2871	-1265								
169	COM22	-2871	-1375								
170	COM23	-2871	-1485								
171	COM24	-2871	-1595								
172	COM25	-2871	-1705								
173	COM26	-2871	-1815								
174	COM27	-2871	-1925								

SAMSUNG ELECTRONICS

PIN DESCRIPTION

POWER SUPPLY

Table 3. Power Supply Pin Description

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>VDD</td><td>Supply</td><td>Power supply</td></tr>
<tr><td>VSS</td><td>Supply</td><td>Ground</td></tr>
<tr><td>V0
V1
V2
V3
V4</td><td>I/O</td><td>LCD driver supply voltages
The voltage determined by LCD pixel is impedance-converted by an operational amplifier for application.
Voltages should have the following relationship;
V0 ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ VSS
When the internal power circuit is active, these voltages are generated as following table according to the state of LCD Bias.
<table>
<tr><td>LCD bias</td><td>V1</td><td>V2</td><td>V3</td><td>V4</td></tr>
<tr><td>1/6 bias</td><td>(5/6) x V0</td><td>(4/6) x V0</td><td>(2/6) x V0</td><td>(1/6) x V0</td></tr>
<tr><td>1/5 bias</td><td>(4/5) x V0</td><td>(3/5) x V0</td><td>(2/5) x V0</td><td>(1/5) x V0</td></tr>
</table></td></tr>
</table>

LCD DRIVER SUPPLY

Table 4. LCD Driver Supply Pin Description

Name	I/O	Description
C1-	O	Capacitor 1 negative connection pin for voltage converter
C1+	O	Capacitor 1 positive connection pin for voltage converter
C2-	O	Capacitor 2 negative connection pin for voltage converter
C2+	O	Capacitor 2 positive connection pin for voltage converter
C3-	O	Capacitor 3 negative connection pin for voltage converter
C3+	O	Capacitor 3 positive connection pin for voltage converter
VOUT	I/O	Voltage converter input / output pin
VR	I	V0 voltage adjustment pin

SYSTEM CONTROL

Table 5. System Control Pin Description

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td rowspan="5">MS</td><td rowspan="5">I</td><td>Master / slave operation select pin
– MS = "H": master operation
– MS = "L": slave operation
The following table depends on the MS status.</td></tr>
<tr><td>
<table>
<tr><th>MS</th><th>OSC circuit</th><th>Power supply circuit</th><th>CL</th><th>M</th><th>FRS</th><th>DISP</th></tr>
<tr><td>H</td><td>Enabled</td><td>Input</td><td>Output</td><td>Output</td><td>Output</td><td>Output</td></tr>
<tr><td>L</td><td>Disabled</td><td>Disabled</td><td>Input</td><td>Input</td><td>Output</td><td>Input</td></tr>
</table>
</td></tr>
<tr><td></td></tr>
<tr><td>CL</td><td>I/O</td><td>Display clock input / output pin
When the KS0716 is used in master/slave mode (multi-chip), the CL pins must be connected each other for sync.</td></tr>
<tr><td>M</td><td>I/O</td><td>LCD AC signal input / output pin
When the KS0716 is used in master/slave mode (multi-chip), the M pins must be connected each other.
– MS = “H”: output
– MS = “L”: input</td></tr>
<tr><td>FRS</td><td>O</td><td>Static driver segment output pin
This pin is used together with the M pin.</td></tr>
<tr><td>DISP</td><td>I/O</td><td>LCD display blanking control input / output
When KS0716 is used in master/slave mode (multi-chip), the DISP pins must be connected each other.
– MS = “H”: output
– MS = “L”: input</td></tr>
<tr><td>TEMPS</td><td>I</td><td>Selects temperature coefficient of the reference voltage
– TEMPS = "L": -0.05%/°C
– TEMPS = "H": -0.2%/°C</td></tr>
</table>

MICROPROCESSOR INTERFACE

Table 6. Microprocessor Interface Pin Description

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>RESETB</td><td>I</td><td>Reset input pin
When RESETB is “L”, initialization is executed.</td></tr>
<tr><td rowspan="5">PS</td><td rowspan="5">I</td><td>Parallel / Serial data input select input
<table>
<tr><th>PS</th><th>Interface mode</th><th>Chip select</th><th>Data / instruction</th><th>Data</th><th>Read / Write</th><th>Serial clock</th></tr>
<tr><td>H</td><td>Parallel</td><td>CS1B, CS2</td><td>RS</td><td>DB0 to DB7</td><td>E_RD
RW_WR</td><td>-</td></tr>
<tr><td>L</td><td>Serial</td><td>CS1B, CS2</td><td>RS</td><td>SID (DB7)</td><td>Write only</td><td>SCLK (DB6)</td></tr>
</table></td></tr>
<tr><td>*NOTE: In serial mode, it is impossible to read data from the on-chip RAM.
And DB0 to DB5 are high impedance and E_RD and RW_WR must be fixed to either “H” or “L”.</td></tr>
<tr><td>MI</td><td>I</td><td>Microprocessor interface select input pin
– MI = "H": 6800-series MPU interface
– MI = "L": 8080-series MPU interface</td></tr>
<tr><td>CS1B
CS2</td><td>I</td><td>Chip select input pins
Data / instruction I/O is enabled only when CS1B is “L” and CS2 is “H”.
When chip select is non-active, DB0 to DB7 may be high impedance.</td></tr>
<tr><td>RS</td><td>I</td><td>Register select input pin
– RS = "H": DB0 to DB7 are display data
– RS = "L": DB0 to DB7 are control data</td></tr>
<tr><td rowspan="4">RW_WR</td><td rowspan="4">I</td><td>Read / Write execution control pin
<table>
<tr><th>MI</th><th>MPU Type</th><th>RW_WR</th><th>Description</th></tr>
<tr><td>H</td><td>6800-series</td><td>RW</td><td>Read / Write control input pin
– RW = “H”: read
– RW = “L”: write</td></tr>
<tr><td>L</td><td>8080-series</td><td>/WR</td><td>Write enable clock input pin
The data on DB0 to DB7 are latched at the rising edge of the /WR signal.</td></tr>
</table></td></tr>
<tr><td></td></tr>
</table>

Table 6. Microprocessor Interface Pin Description (Continued)

<table>
<tr><th>Name</th><th>I/O</th><th colspan="4">Description</th></tr>
<tr><td rowspan="5">E_RD</td><td rowspan="5">I</td><td colspan="4">Read / Write execution control pin</td></tr>
<tr><td>MI</td><td>MPU Type</td><td>E_RD</td><td>Description</td></tr>
<tr><td>H</td><td>6800-series</td><td>E</td><td>Read / Write control input pin
– RW = “H”: When E is “H”, DB0 to DB7 are in an output status.
– RW = “L”: The data on DB0 to DB7 are latched at the falling edge of the E signal.</td></tr>
<tr><td>L</td><td>8080-series</td><td>/RD</td><td>Read enable clock input pin
When /RD is “L”, DB0 to DB7 are in an output status.</td></tr>
<tr><td colspan="4"></td></tr>
<tr><td>DB0
to
DB7</td><td>I/O</td><td colspan="4">8-bit bi-directional data bus that is connected to the standard 8-bit microprocessor data bus. When the serial interface selected (PS = "L");
– DB0 to DB5: high impedance
– DB6: serial input clock (SCLK)
– DB7: serial input data (SID)
When chip select is not active, DB0 to DB7 may be high impedance.</td></tr>
</table>

LCD DRIVER OUTPUTS

Table 7. LCD Driver Outputs Pin Description

<table>
<tr><th>Name</th><th>I/O</th><th colspan="4">Description</th></tr>
<tr><td rowspan="9">SEG0
to
SEG99</td><td rowspan="9">O</td><td colspan="4">LCD segment driver outputs
The display data and the M signal control the output voltage of segment driver.</td></tr>
<tr><td rowspan="2">Display data</td><td rowspan="2">M</td><td colspan="2">Segment driver output voltage</td></tr>
<tr><td>Normal display</td><td>Reverse display</td></tr>
<tr><td>H</td><td>H</td><td>V0</td><td>V2</td></tr>
<tr><td>H</td><td>L</td><td>Vss</td><td>V3</td></tr>
<tr><td>L</td><td>H</td><td>V2</td><td>V0</td></tr>
<tr><td>L</td><td>L</td><td>V3</td><td>Vss</td></tr>
<tr><td colspan="2">Power save mode</td><td>Vss</td><td>Vss</td></tr>
<tr><td colspan="4"></td></tr>
<tr><td rowspan="8">COM0
to
COM31</td><td rowspan="8">O</td><td colspan="4">LCD common driver outputs
The internal scanning data and M signal control the output voltage of common driver.</td></tr>
<tr><td>Scan data</td><td>M</td><td colspan="2">Common driver output voltage</td></tr>
<tr><td>H</td><td>H</td><td colspan="2">Vss</td></tr>
<tr><td>H</td><td>L</td><td colspan="2">V0</td></tr>
<tr><td>L</td><td>H</td><td colspan="2">V1</td></tr>
<tr><td>L</td><td>L</td><td colspan="2">V4</td></tr>
<tr><td colspan="2">Power save mode</td><td colspan="2">Vss</td></tr>
<tr><td colspan="4"></td></tr>
<tr><td>COMS</td><td>O</td><td colspan="4">Common output for the icons. The output signals of two pins are same. When not used, these pins should be left open. In multi-chip (master / slave) mode, all COMS pins on both master and slave units are the same signal.</td></tr>
</table>

TEST PINS

Table 8. Test Pin Description

Name	I/O	Description
TESTL1 TESTL2	I	IC test pins with pull-up These pins should be opened (floated).

FUNCTIONAL DESCRIPTION

MICROPROCESSOR INTERFACE

Chip Select Input

There are CS1B and CS2 pins for chip selection. The KS0716 can interface with an MPU only when CS1B is “L” and CS2 is “H”. When these pins are set to any other combination, RS, E_RD, and RW_WR inputs are disabled and DB0 to DB7 are to be high impedance. And, in case of serial interface, the internal shift register and the counter are reset.

Parallel / Serial Interface

KS0716 has three types of interface with an MPU, which are one serial and two parallel interfaces. This parallel or serial interface is determined by PS pin as shown in table 9**.**

Table 9. Parallel / Serial Interface Mode.

PS	Type	CS1B	CS2	MI	Interface mode
H	Parallel	CS1B	CS2	H	6800-series MPU mode
				L	8080-series MPU mode
L	Serial	CS1B	CS2	*×	Serial-mode

*×: Don't care

Parallel Interface (PS = "H")

The 8-bit bi-directional data bus is used in parallel interface and the type of MPU is selected by MI as shown in table 10. The type of data transfer is determined by signals at RS, E_RD and RW_WR as shown in table 11.

Table 10. Microprocessor Selection for Parallel Interface

MI	CS1B	CS2	RS	E_RD	RW_WR	DB0 to DB7	MPU bus
H	CS1B	CS2	RS	E	RW	DB0 to DB7	6800-series
L	CS1B	CS2	RS	/RD	/WR	DB0 to DB7	8080-series

Table 11. Parallel Data Transfer

Common	6800-series		8080-series		Description
RS	E_RD (E)	RW_WR (RW)	E_RD (/RD)	RW_WR (/WR)	
H	H	H	L	H	Display data read out
H	H	L	H	L	Display data write
L	H	H	L	H	Register status read
L	H	L	H	L	Writes to internal register (instruction)

Serial Interface (PS = "L")

When the KS0716 is active, serial data (DB7) and serial clock (DB6) inputs are enabled. And not active, the internal 8-bit shift register and the 3-bit counter are reset. Serial data can be read on the rising edge of serial clock going into DB6 and processed as 8-bit parallel data on the eighth serial clock. Serial data input is display data when RS is high and control data when RS is low. Since the clock signal (DB6) is easy to be affected by the external noise caused by the line length, the operation check on the actual machine is recommended.

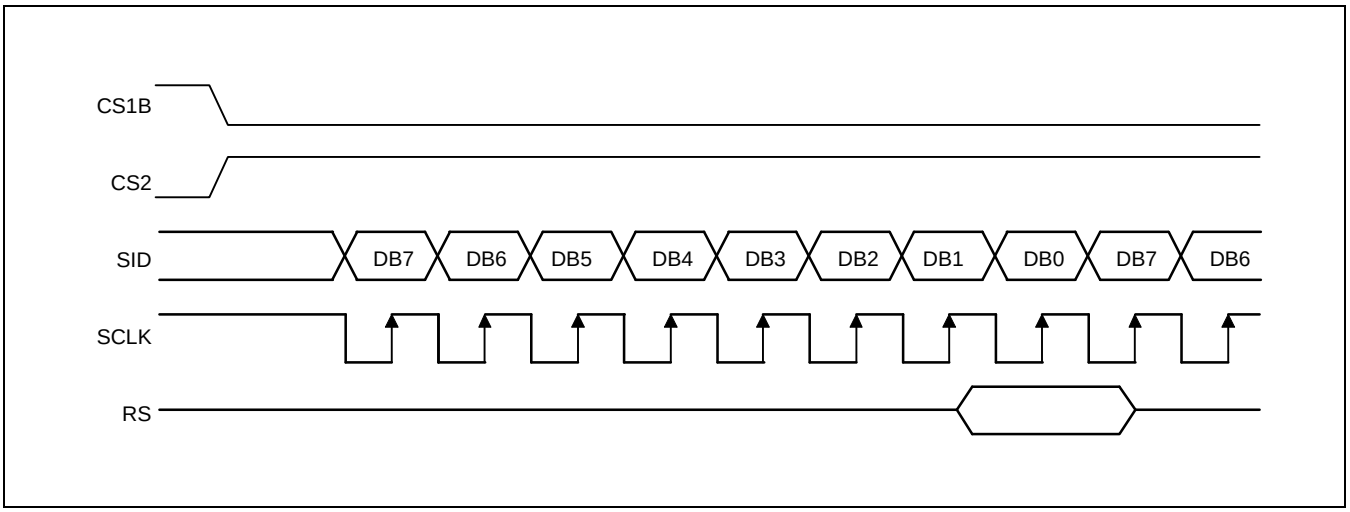

Figure 3. Serial Interface Timing

Busy Flag

The Busy Flag indicates whether the KS0716 is operating or not. When DB7 is “H” in read status operation, this device is in busy status and will accept only read status instruction. If the cycle time is correct, the microprocessor needs not to check this flag before each instruction, which improves the MPU performance.

Data Transfer

The KS0716 uses bus holder and internal data bus for Data Transfer with the MPU. When writing data from the MPU to on-chip RAM, data is automatically transferred from the bus holder to the RAM as shown in figure 4. And when reading data from on-chip RAM to the MPU, the data for the initial read cycle is stored in the bus holder (dummy read) and the MPU reads this stored data from bus holder for the next data read cycle as shown in figure 5. This means that a dummy read cycle must be inserted between each pair of address sets when a sequence of address sets is executed. Therefore, the data of the specified address cannot be output with the read display data instruction right after the address sets, but can be output at the second read of data.

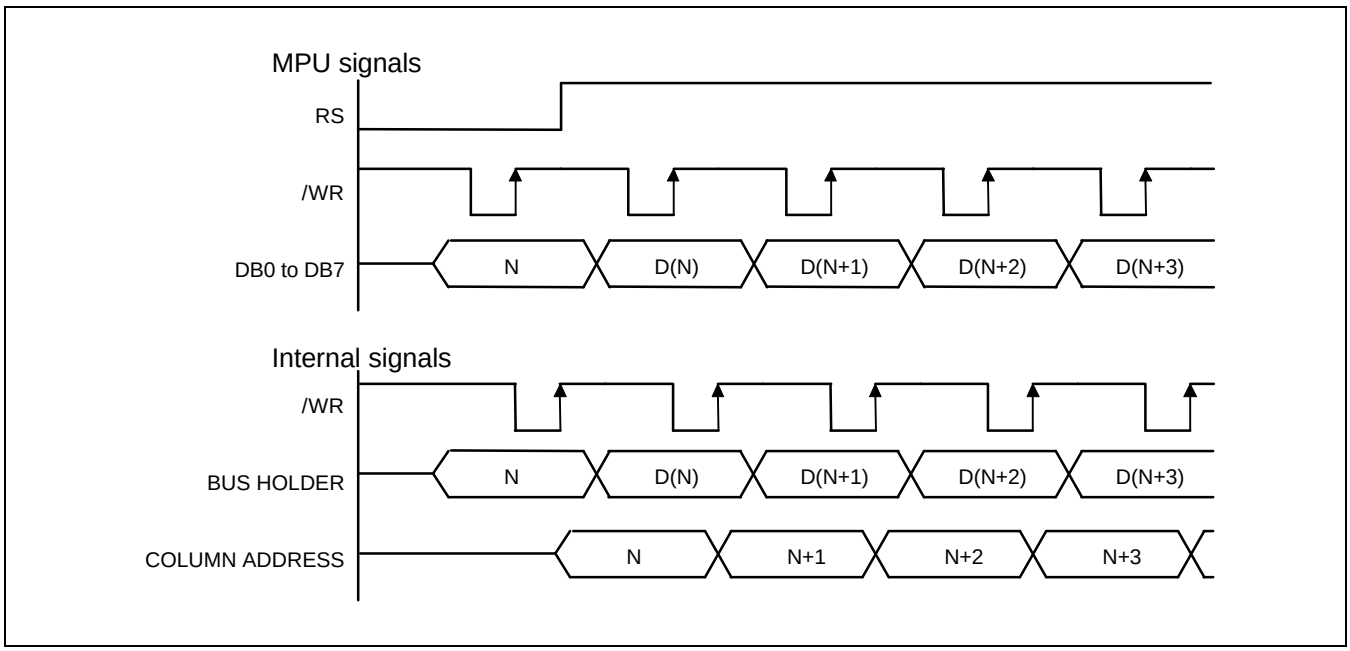

Figure 4. Write Timing

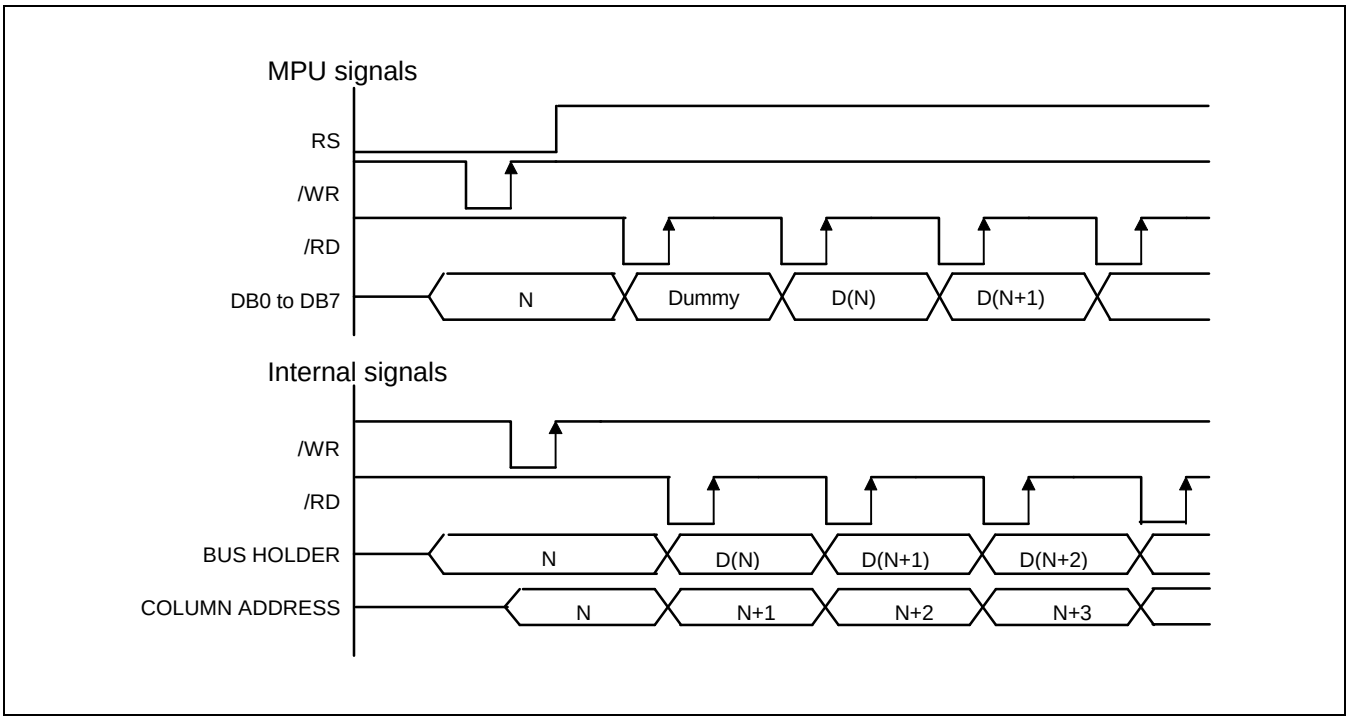

Figure 5. Read Timing

DISPLAY DATA RAM (DDRAM)

The Display Data RAM stores pixel data for the LCD. It is 65-row by 132-column addressable array. Each pixel can be selected when the page and column addresses are specified. The 65 rows are divided into 8 pages of 8 lines and the 9th page with a single line (DB0 only). Data is read from or written to the 8 lines of each page directly through DB0 to DB7. The display data of DB0 to DB7 from the microprocessor correspond to the LCD common lines as shown in figure 6. The microprocessor can read from and write to RAM through the I/O buffer. Since the LCD controller operates independently, data can be written into RAM at the same time as data is being displayed without causing the LCD flicker.

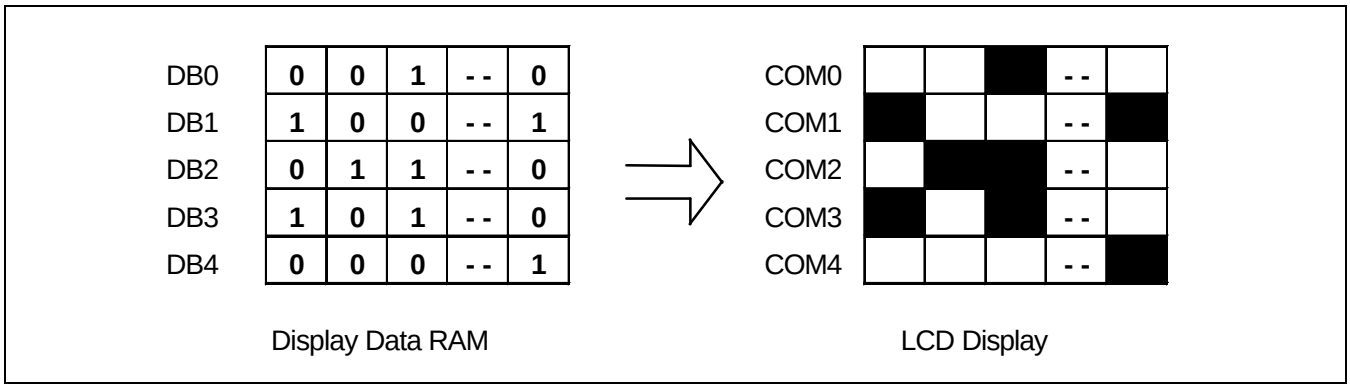

Figure 6. RAM-to-LCD Data Transfer

Page Address Circuit

This circuit is for providing a Page Address to Display Data RAM shown in figure 8. It incorporates 4-bit Page Address register changed by only the “Set Page” instruction. Page Address 8 (DB3 is “H”, but DB2, DB1 and DB0 are “L”) is a special RAM area for the icons and display data DB0 is only valid. When Page Address is above 8, it is impossible to access to on-chip RAM.

Line Address Circuit

This circuit assigns DDRAM a Line Address corresponding to the first line (COM0) of the display. Therefore, by setting Line Address repeatedly, it is possible to realize the screen scrolling and page switching without changing the contents of on-chip RAM as shown in figure 8. It incorporates 6-bit Line Address register changed by only the Initial display line instruction and 6-bit counter circuit. At the beginning of each LCD frame, the contents of register are copied to the line counter which is increased by CL signal and generates the Line Address for transferring the 132-bit RAM data to the 100 display data latch circuit. However, display data of icons are not scrolled because the MPU can not access Line Address of icons.

Column Address Circuit

Column Address circuit has a 8-bit preset counter that provides Column Address to the Display Data RAM as shown in figure 8. When set Column Address MSB / LSB instruction is issued, 8-bit [Y7:Y0] is updated. And, since this address is increased by 1 each a read or write data instruction, microprocessor can access the display data continuously. However, the counter is not increased and locked if a non-existing address above 84H. It is unlocked if a Column Address is set again by set Column Address MSB / LSB instruction. And the Column Address counter is independent of page address register.

ADC Select instruction makes it possible to invert the relationship between the column address and the segment outputs. It is necessary to rewrite the display data on built-in RAM after issuing ADC Select instruction. Refer to the following figure 7.

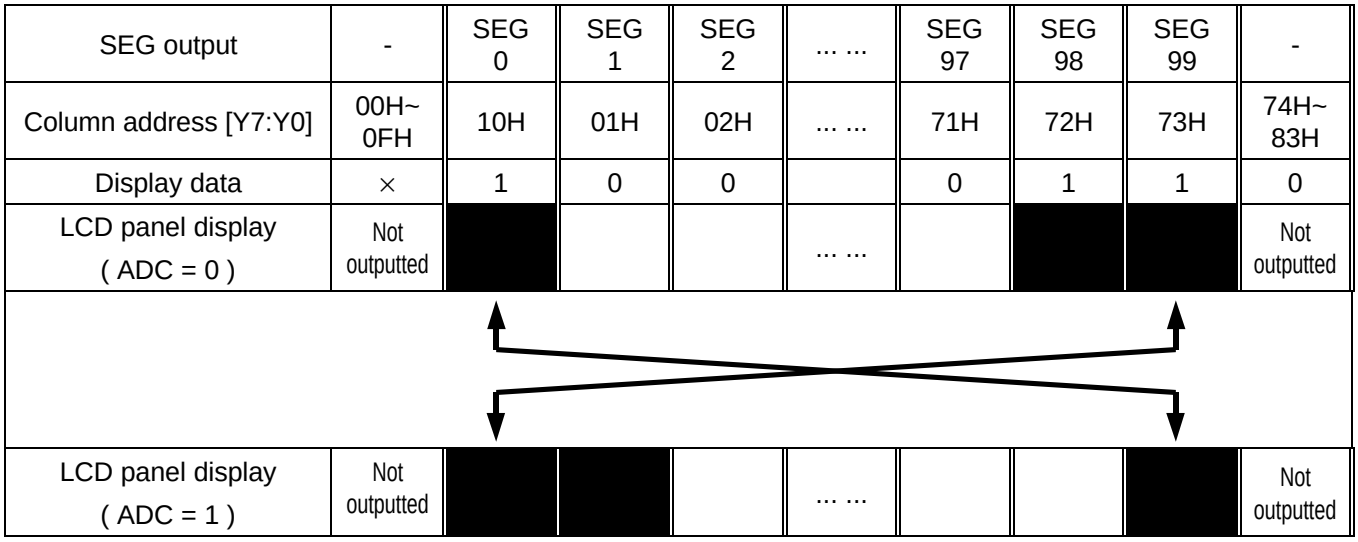

Figure 7. The Relationship between the Column Address and the Segment Outputs

Segment Control Circuit

This circuit controls the display data by the display ON / OFF, reverse display ON / OFF and entire display ON / OFF instructions without changing the data in the display data RAM.

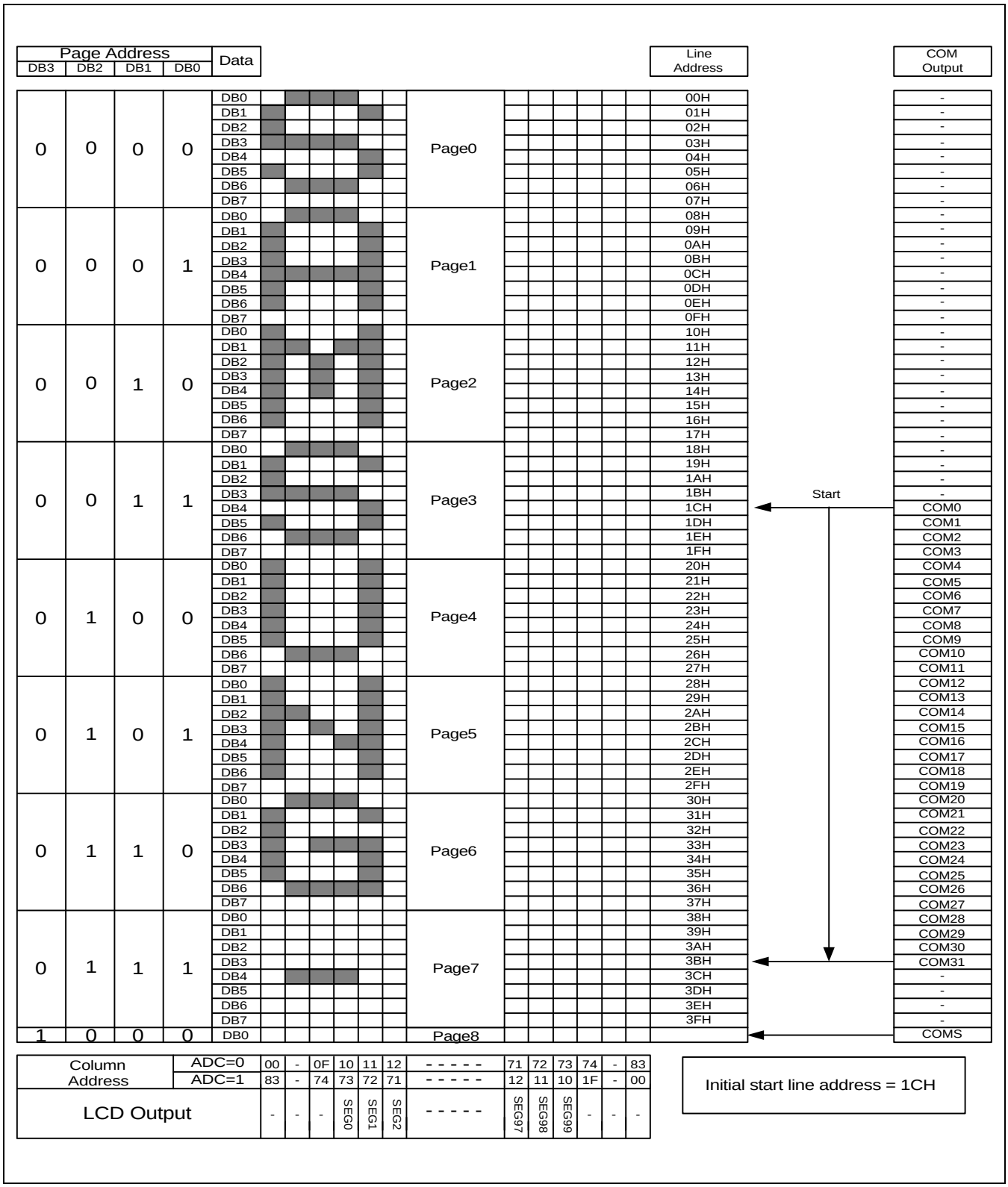

Figure 8. Display Data RAM Map

LCD DISPLAY CIRCUITS

Oscillator

This is completely on-chip oscillator and its frequency is nearly independent of V_{DD}. This oscillator signal is used in the voltage converter and display timing generation circuit.

* Test Condition: Temperature (25°C & 85°C), TEMPS="L", No Load

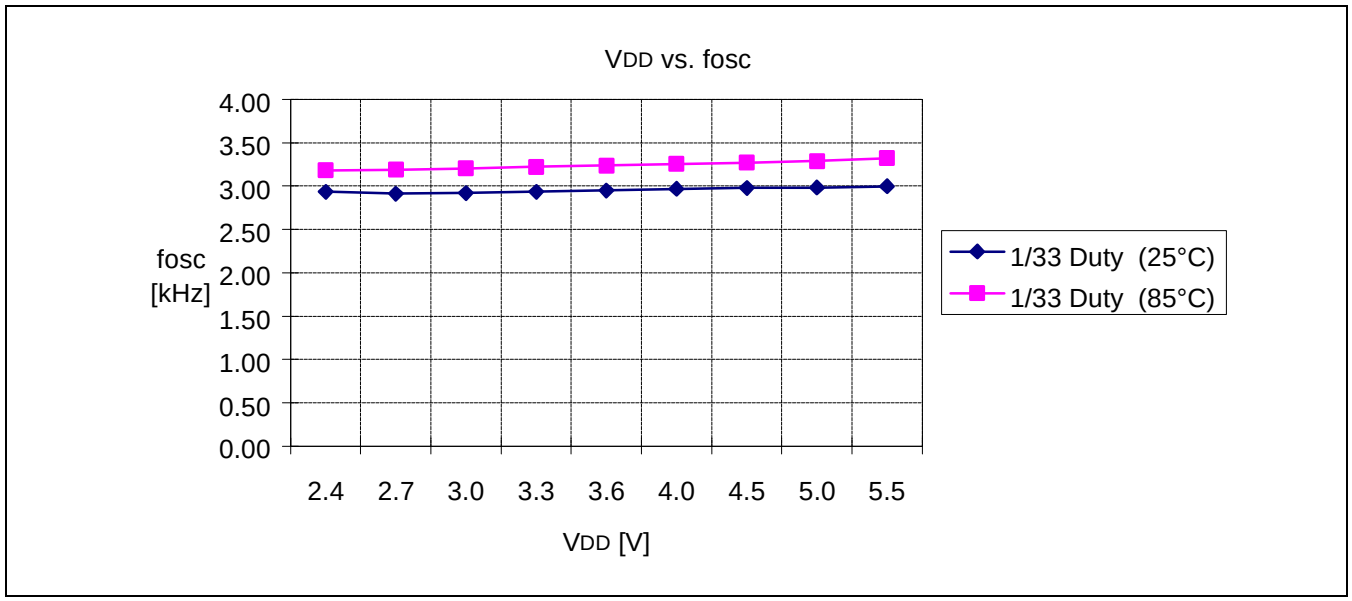

Figure 9. V_{DD} vs. fosc

Display Timing Generator Circuit

This circuit generates some signals to be used for displaying LCD. The display clock, CL, generated by oscillation clock, generates the clock for the line counter and the signal for the display data latch. The line address of on-chip RAM is generated in synchronization with the display clock (CL) and the 100-bit display data is latched by the display data latch circuit in synchronization with the display clock. The display data, which is read to the LCD driver, is completely independent of the access to the display data RAM from the microprocessor. The display clock generates an LCD AC signal (M) which enables the LCD driver to make a AC drive waveform, and also generates an internal common timing signal and start signal to the common driver. Driving 2-frame AC driver waveform and internal timing signal are shown in figure 10.

In a multiple-chip configuration, the slave chip requires the M, CL and DISP signals from the master. The table 12 shows the M, CL, and DISP status.

Table 12. Master and Slave Timing Signal Status

Operation mode	Oscillator	M	CL	DISP
Master	ON (internal clock used)	Output	Output	Output
	OFF (external clock used)	Output	Input	Output
Slave	-	Input	Input	Input

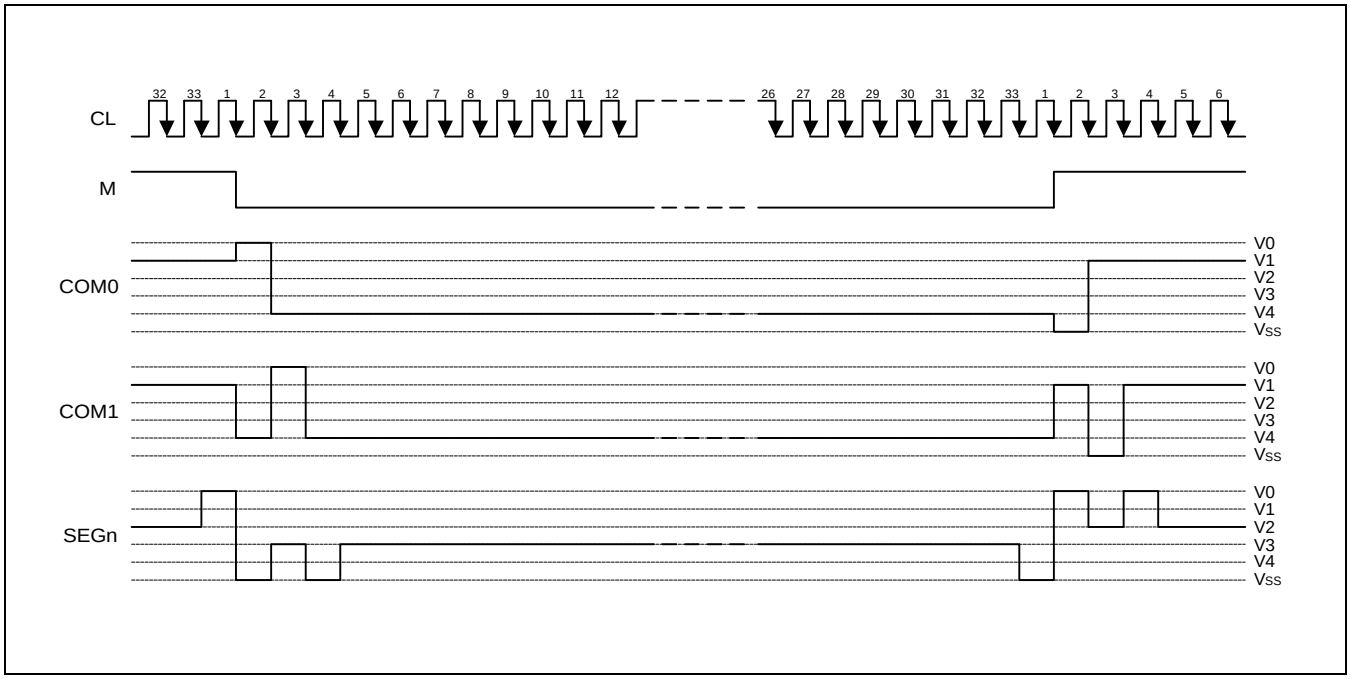

Figure 10. 2-frame AC Driving Waveform

Common Output Control Circuit

This circuit controls the relationship between the number of common output and specified duty ratio. SHL Select Instruction specifies the scanning direction of the common output pins.

Table 13. The Relationship between Duty Ratio and Common Output

Duty	SHL	Common output pins	
		COM0 to COM31	COMS
1/33	0	COM0 to COM31	COMS
	1	COM31 to COM0	

LCD DRIVER CIRCUIT

This Driver circuit is configured by 34-channel (including 2 COMS channel) common driver and 100-channel segment driver. This LCD panel driver voltage depends on the combination of display data and M signal.

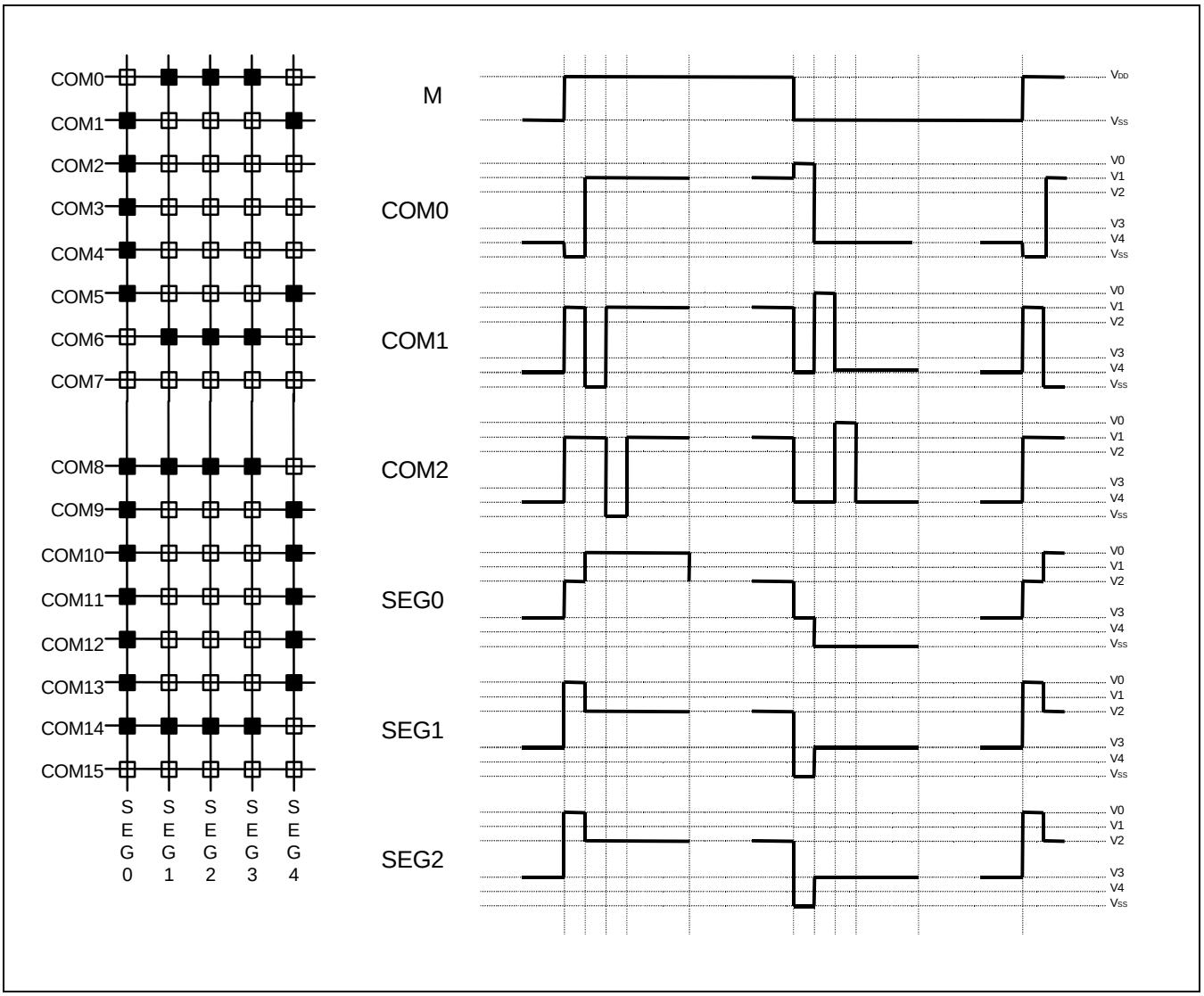

Figure 11. Segment and Common Timing

POWER SUPPLY CIRCUITS

The Power Supply circuits generate the voltage levels necessary to drive liquid crystal driver circuits with low-power consumption and the fewest components. There are voltage converter circuits, voltage regulator circuits, and voltage follower circuits. They are valid only in master operation and controlled by power control instruction. For details, refers to "Instruction Description". The table 14 shows the referenced combinations in using Power Supply circuits.

Table 14. Recommended Power Supply Combinations

User setup	Power control (VC VR VF)	V/C circuits	V/R circuits	V/F circuits	VOUT	V0	V1 to V4
Only the internal power supply circuits are used	1 1 1	ON	ON	ON	Open	Open	Open
Only the voltage regulator circuits and voltage follower circuits are used	0 1 1	OFF	ON	ON	External input	Open	Open
Only the voltage follower circuits are used	0 0 1	OFF	OFF	ON	Open	External input	Open
Only the external power supply circuits are used	0 0 0	OFF	OFF	ON	Open	External input	External input

Voltage Converter Circuits

These circuits boost up the electric potential between VDD and VSS to 2, 3 or 4 times toward positive side and boosted voltage is outputted from VOUT pin.

[C1 = 1.0 to 4.7 *m*F]

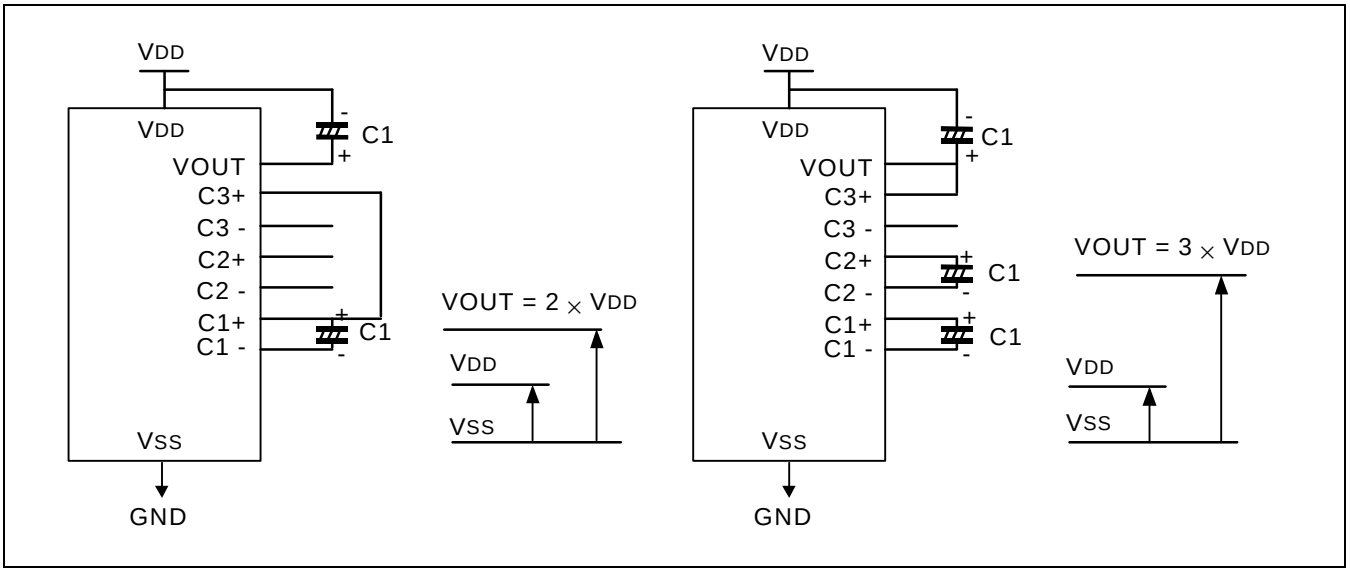

Figure 12. Two times boosting circuit

Figure 13. Three times boosting circuit

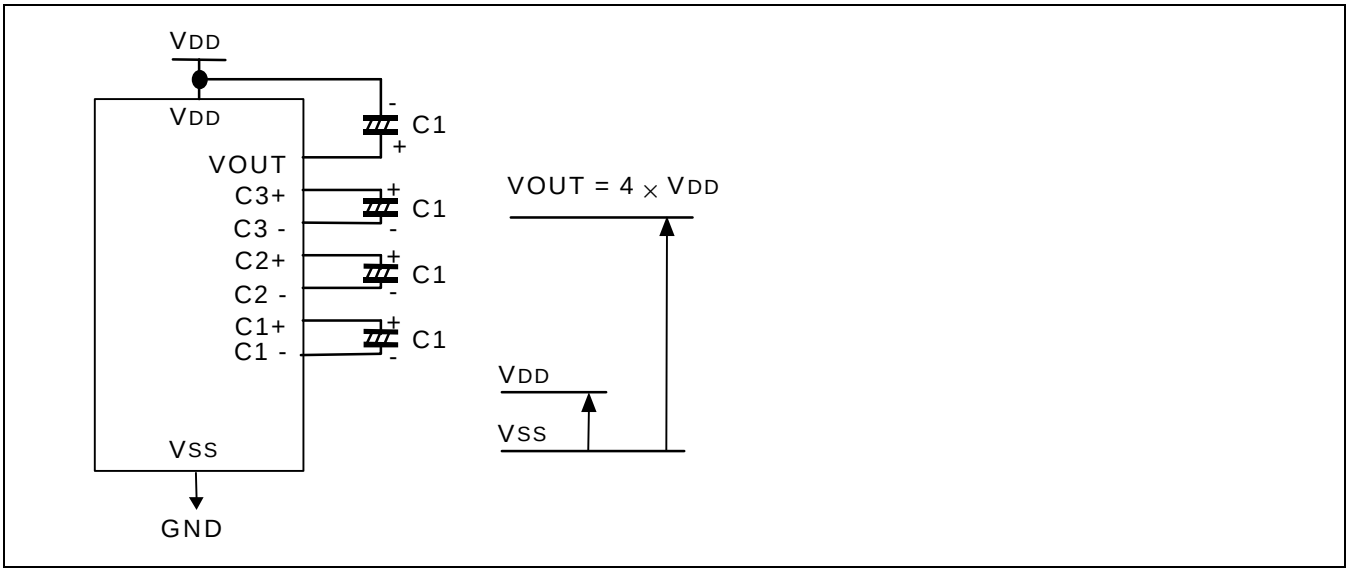

Figure 14. Four Times Boosting Circuit

Voltage Regulator Circuits

The function of the internal Voltage Regulator circuits is to determine liquid crystal operating voltage, V0, by adjusting resistors, Ra and Rb, within the range of |V0| < |VOUT|. Because VOUT is the operating voltage of operational-amplifier circuits shown in figure 15, it is necessary to be applied internally or externally.

For the Eq. 1, we determine V0 by Ra, Rb and V_{EV}. The Ra and Rb are connected internally or externally by INTRS pin. And V_{EV} called the voltage of electronic volume is determined by Eq. 2, where the parameter α is the value selected by instruction, "Set Reference Voltage Register", within the range 0 to 31. V_{REF} voltage at Ta = 25°C is shown in table 15-1.

$$V0 = \left(1 + \frac{Rb}{Ra}\right) \times V_{EV} \quad [V] \text{ ------ (Eq. 1)}$$

$$V_{EV} = \left(1 - \frac{(31 - \alpha)}{150}\right) \times V_{REF} \quad [V] \text{ ------ (Eq. 2)}$$

Table 15-1. V_{REF} Voltage at Ta = 25°C

TEMPS	Temp. Coefficient	V_{REF} [V]
L	-0.05%/ °C	1.9
H	-0.2% / °C	2.1

Table 15-2. Reference Voltage Parameter (α)

SV4	SV3	SV2	SV1	SV0	Reference voltage parameter (α)
0	0	0	0	0	0
0	0	0	0	1	1
:	:	:	:	:	:
:	:	:	:	:	:
1	1	1	1	0	30
1	1	1	1	1	31

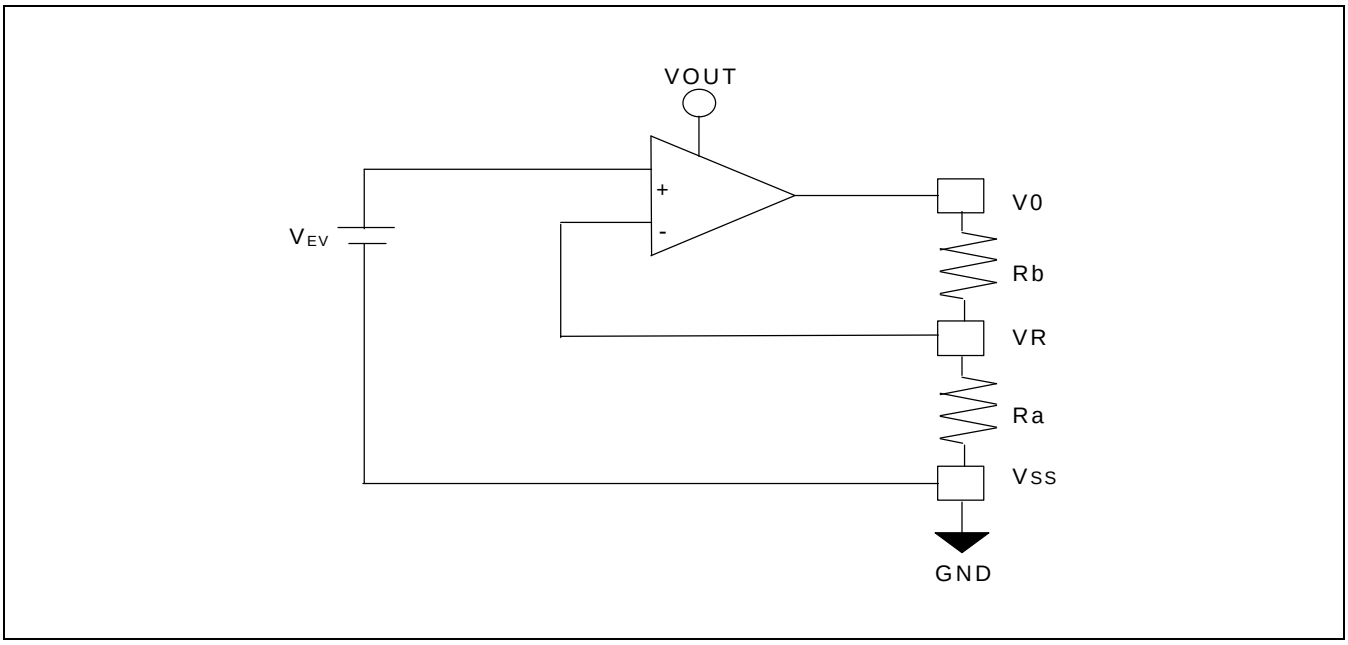

Figure 15. Internal Voltage Regulator Circuit

In Case of Using External Resistors, Ra and Rb

It is necessary to connect external regulator resistor Ra between VR and VSS, and Rb between V0 and VR.

Example: For the following requirements

1. LCD driver voltage, V0 = 8V
2. 5-bit reference voltage register = (1, 1, 1, 1, 1)
3. Maximum current flowing Ra, Rb = 1 uA

From Eq. 1

$$8 = \left(1 + \frac{Rb}{Ra}\right) \times V_{EV} \quad [V] \text{ ------ (Eq. 3)}$$

From Eq. 2

$$V_{EV} = \left(1 - \frac{(31 - 31)}{150}\right) \times 1.9 = 1.9 \quad [V] \text{ ------ (Eq. 4)}$$

From requirement 3.

$$\frac{8}{Ra + Rb} = 1 \text{ [uA]} \quad \text{------ (Eq. 5)}$$

From equations Eq. 3, 4 and 5
Ra = 1.9 [MΩ]
Rb = 6.1 [MΩ]

The following table shows the range of V0 depending on the above requirements.

Table 16. V0 depending on Electronic Volume Level

	Electronic volume level				
	0	**.....**	**16**	**.....**	**31**
V0	6.33	.....	7.19	.....	8

Voltage Follower Circuits

VLCD voltage (V0) is resistively divided into four voltage levels (V1, V2, V3 and V4) and those output impedance are converted by the Voltage Follower for increasing drive capability. The table 17 shows the relationship between V1 to V4 level and bias.

Table 17. The Relationship between V1 to V4 Level and Bias

Duty ratio	LCD bias	V1	V2	V3	V4
1/33	1/6	(5/6) x V0	(4/6) x V0	(2/6) x V0	(1/6) x V0
	1/5	(4/5) x V0	(3/5) x V0	(2/5) x V0	(1/5) x V0

REFERECE CIRCUIT EXAMPLES

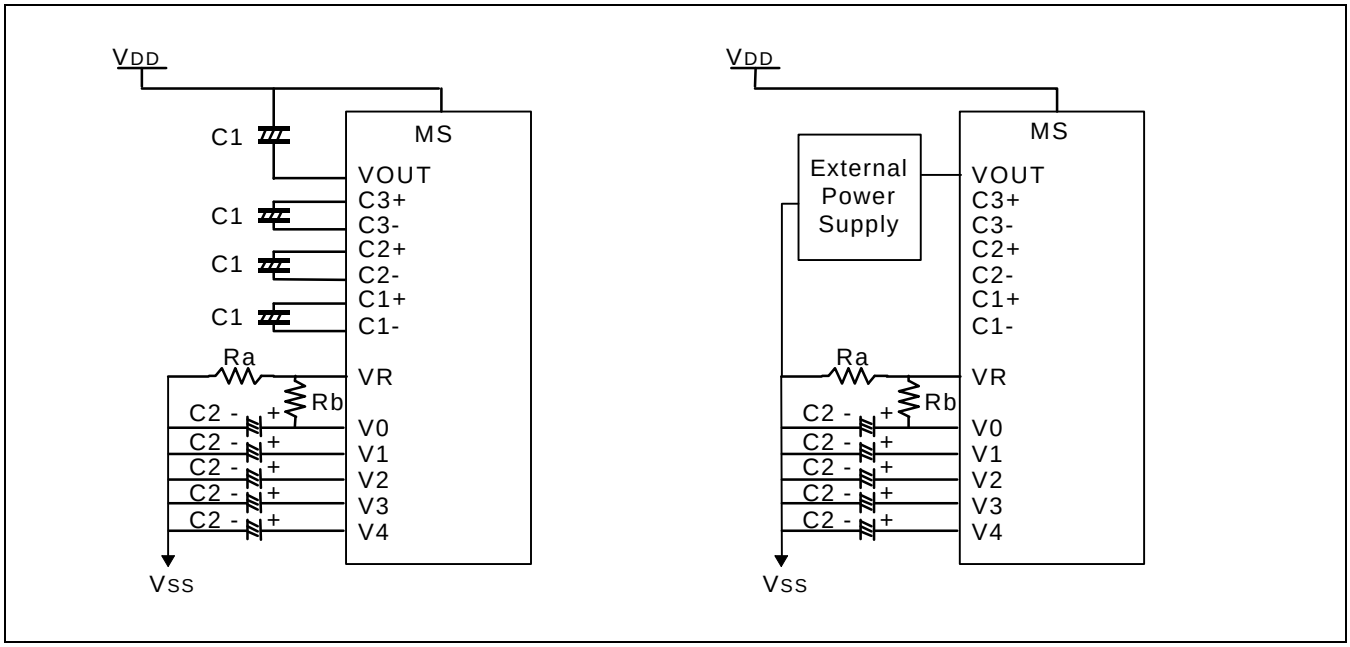

Figure 16. When Using all LCD Power Circuits (4-Time V/C: ON, V/R: ON, V/F: ON)

Figure 17. When not Using V/C Circuit

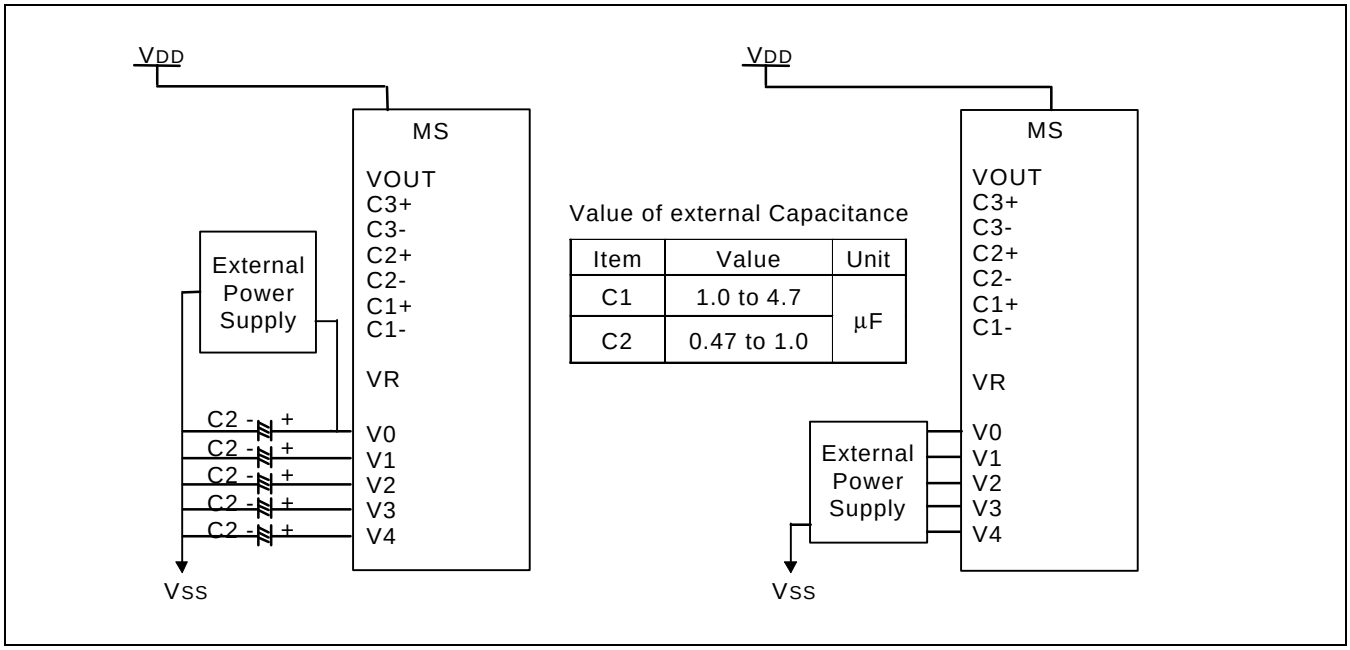

Figure 18. When Using some LCD Power Circuits (V/C: OFF, V/R: OFF, V/F: ON)

Figure 19. When not Using Internal LCD Power Supply Circuit

RESET CIRCUIT

Setting RESETB to “L” or Reset instruction can initialize internal function.
When RESETB becomes “L”, following procedure is occurred.

Display ON / OFF: OFF
Entire display ON / OFF: OFF (normal)
ADC select: OFF (normal)
Reverse display ON / OFF: OFF (normal)
Power control register (VC, VR, VF) = (0, 0, 0)
LCD bias ratio: 1/6
Read-modify-write: OFF
SHL select: OFF (normal)
Static indicator mode: OFF
Display start line: 0 (first)
Column address: 0
Page address: 0
Reference voltage set: OFF
Reference voltage control register: (SV4, SV3, SV2, SV1, SV0) = (0, 0, 0, 0, 0)

When RESET instruction is issued, following procedure is occurred.

Read-modify-write: OFF
Static indicator mode: OFF
SHL select: 0
Display start line: 0 (first)
Column address: 0
Page address: 0
Reference voltage set: OFF
Reference voltage control register: (SV4, SV3, SV2, SV1, SV0) = (0, 0, 0, 0, 0)

While RESETB is “L” or Reset instruction is executed, no instruction except read status could be accepted. Reset status appears at DB4. After DB4 becomes ”L”, any instruction can be accepted. RESETB must be connected to the reset pin of the MPU, and initialize the MPU and this LSI at the same time. The initialization by RESETB is essential before used.

INSTRUCTION DESCRIPTION

Table 18. Instruction Table

× : Don't care

Instruction	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
Read display data	1	1	Read data								Read data from DDRAM
Write display data	1	0	Write data								Write data into DDRAM
Read status	0	1	BUSY	ADC	ONOFF	RESETB	0	0	0	0	Read the internal status
Display ON / OFF	0	0	1	0	1	0	1	1	1	DON	Turn ON / OFF LCD panel When DON = 0: display OFF When DON = 1: display ON
Initial display line	0	0	0	1	ST5	ST4	ST3	ST2	ST1	ST0	Specify DDRAM line for COM1
Set Reference Voltage mode	0	0	1	0	0	0	0	0	0	1	Set reference voltage mode
Set reference voltage register	0	0	1	0	0	SV4	SV3	SV2	SV1	SV0	Set reference voltage register
Set page address	0	0	1	0	1	1	P3	P2	P1	P0	Set page address
Set column address MSB	0	0	0	0	0	1	0	Y6	Y5	Y4	Set column address MSB
Set column address LSB	0	0	0	0	0	0	Y3	Y2	Y1	Y0	Set column address LSB
ADC select	0	0	1	0	1	0	0	0	0	ADC	Select SEG output direction When ADC = 0: normal direction (SEG0→SEG99) When ADC = 1: reverse direction (SEG99→SEG0)
Reverse display ON / OFF	0	0	1	0	1	0	0	1	1	REV	Select normal / reverse display When REV = 0: normal display When REV = 1: reverse display
Entire display ON / OFF	0	0	1	0	1	0	0	1	0	EON	Select normal/ entire display ON When EON = 0: normal display. When EON = 1: entire display ON
LCD bias select	0	0	1	0	1	0	0	0	1	BIAS	Select LCD bias
Set modify-read	0	0	1	1	1	0	0	0	0	0	Set modify-read mode
Reset modify-read	0	0	1	1	1	0	1	1	1	0	release modify-read mode
Reset	0	0	1	1	1	0	0	0	1	0	Initialize the internal functions
SHL select	0	0	1	1	0	0	SHL	×	×	×	Select COM output direction When SHL = 0: normal direction (COM0→COM31) When SHL = 1: reverse direction (COM31→COM0)
Power control	0	0	0	0	1	0	1	VC	VR	VF	Control power circuit operation
Set static indicator register	0	0	1	0	1	0	1	1	0	SI	Set static indicator register SI = 0 (OFF), SI = 1 (ON)
Power save	-	-	-	-	-	-	-	-	-	-	Compound instruction of display OFF and entire display ON
Test instruction	0	0	1	1	1	1	×	×	×	×	***Don't use this instruction.***

SAMSUNG ELECTRONICS

Read Display Data

8-bit data from display data RAM specified by the column address and page address could be read by this instruction. As the column address is increased by 1 automatically after each this instruction, the micro-processor can continuously read data from the addressed page. A dummy read is required after loading an address into the column address register. Display data cannot be read through the serial interface.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	Read data							

Write Display Data

8-bit data of display data from the microprocessor can be written to the RAM location specified by the column address and page address. The column address is increased by 1 automatically so that the microprocessor can continuously write data to the addressed page.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	Write data							

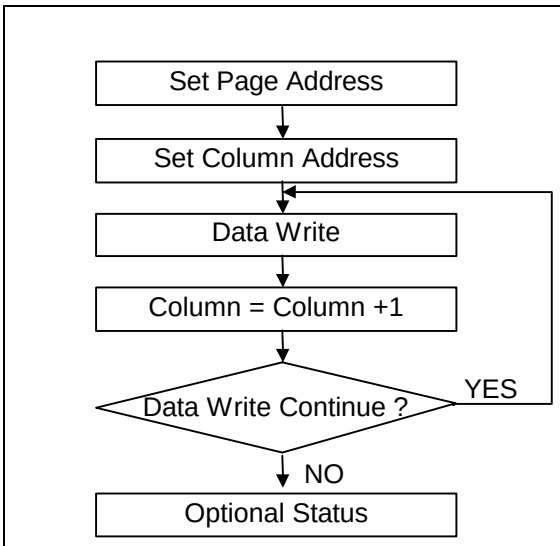

Figure 20. Sequence for Writing Display Data

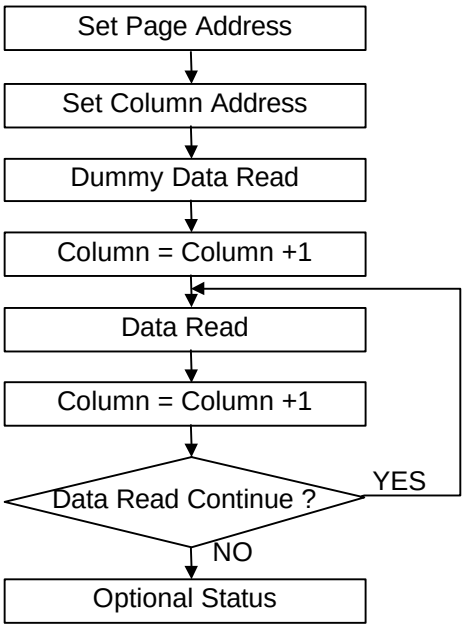

Figure 21. Sequence for Reading Display Data

Read Status

Indicates the internal status of the KS0716.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	BUSY	ADC	ON/OFF	RESETB	0	0	0	0

Flag	Description
BUSY	The device is busy when internal operation or reset. Any instruction is rejected until BUSY goes low. 0: chip is active, 1: chip is being busy
ADC	Indicates the relationship between RAM column address and segment driver. 0: reverse direction (SEG99 → SEG0), 1: normal direction (SEG0 → SEG99)
ON/OFF	Indicates display ON / OFF status. 0: display ON, 1: display OFF
RESETB	Indicates the initialization is in progress by RESETB signal. 0: chip is active, 1: chip is being reset

Display ON / OFF

Turns the Display ON or OFF

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	1	1	DON

DON = 1: display ON
DON = 0: display OFF

Initial Display Line

Sets the line address of display RAM to determine the Initial Display Line. The RAM display data is displayed at the top row (COM0 when SHL = L, COM31 when SHL = H) of LCD panel.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	ST5	ST4	ST3	ST2	ST1	ST0

ST5	ST4	ST3	ST2	ST1	ST0	Line address
0	0	0	0	0	0	0
0	0	0	0	0	1	1
:	:	:	:	:	:	:
1	1	1	1	1	0	62
1	1	1	1	1	1	63

Reference Voltage Select

Consists of 2-byte instruction
The 1st instruction sets reference voltage mode, the 2nd one updates the contents of reference voltage register. After second instruction, reference voltage mode is released.

The 1st Instruction: Set Reference Voltage Select Mode

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	0	0	0	0	1

The 2nd Instruction: Set Reference Voltage Register

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	SV4	SV3	SV2	SV1	SV0

SV4	SV3	SV2	SV1	SV0	Reference voltage parameter (α)
0	0	0	0	0	0
0	0	0	0	1	1
:	:	:	:	:	:
:	:	:	:	:	:
1	1	1	1	0	30
1	1	1	1	1	31

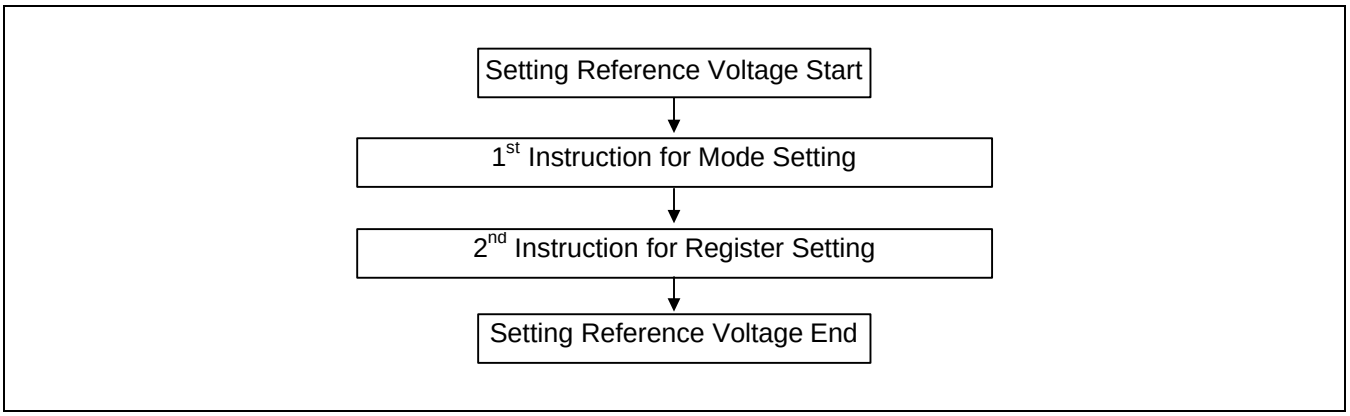

Figure 22. Sequence for Setting the Reference Voltage

Set Page Address

Sets the Page Address of display data RAM from the microprocessor into the Page Address register. Any RAM data bit can be accessed when its Page Address and column address are specified. Along with the column address, the Page Address defines the address of the display RAM to write or read display data. Changing the Page Address doesn't effect to the display status.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	1	P3	P2	P1	P0

P3	P2	P1	P0	Page
0	0	0	0	0
0	0	0	1	1
:	:	:	:	:
0	1	1	1	7
1	0	0	0	8

Set Column Address

Sets the Column Address of display RAM from the microprocessor into the column address register. Along with the Column Address, the Column Address defines the address of the display RAM to write or read display data. When the microprocessor reads or writes display data to or from display RAM, Column Addresses are automatically increased.

Set Column Address MSB

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	0	Y6	Y5	Y4

Set Column Address LSB

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	Y3	Y2	Y1	Y0

Y6	Y5	Y4	Y3	Y2	Y1	Y0	Column address
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
:	:	:	:	:	:	:	:
1	1	0	0	0	1	0	98
1	1	0	0	0	1	1	99

ADC Select

Changes the relationship between RAM column address and segment driver. The direction of segment driver output pins could be reversed by software. This makes IC layout flexible in LCD module assembly.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	0	0	ADC

ADC = 0: Normal Direction (SEG0 → SEG99)
ADC = 1: Reverse Direction (SEG99 → SEG0)

Reverse Display ON / OFF

Reverses the display status on LCD panel without rewriting the contents of the display data RAM.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	1	1	REV

REV	RAM bit data = "1"	RAM bit data = "0"
0 (normal)	LCD pixel is illuminated	LCD pixel is not illuminated
1 (reverse)	LCD pixel is not illuminated	LCD pixel is illuminated

Entire Display ON / OFF

Forces the whole LCD points to be turned ON regardless of the contents of the display data RAM. At this time, the contents of the display data RAM are held. This instruction has priority over the reverse display ON / OFF instruction.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	1	0	EON

EON = 0: Normal Display
EON = 1: Entire Display ON

Select LCD Bias

Selects LCD Bias ratio of the voltage required for driving the LCD.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	0	1	Bias

Duty Ratio	LCD Bias	
	Bias = 0	Bias = 1
1/33	1/6	1/5

Set Modify-Read

This instruction stops the automatic increment of the column address by the read display data instruction, but the column address is still increased by the write display data instruction. And it reduces the load of microprocessor when the data of a specific area is repeatedly changed during cursor blinking or others. This mode is canceled by the reset Modify-read instruction.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	0	0

Reset Modify-Read

This instruction cancels the Modify-read mode, and makes the column address return to its initial value just before the set Modify-read instruction is started.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	1	1	1	0

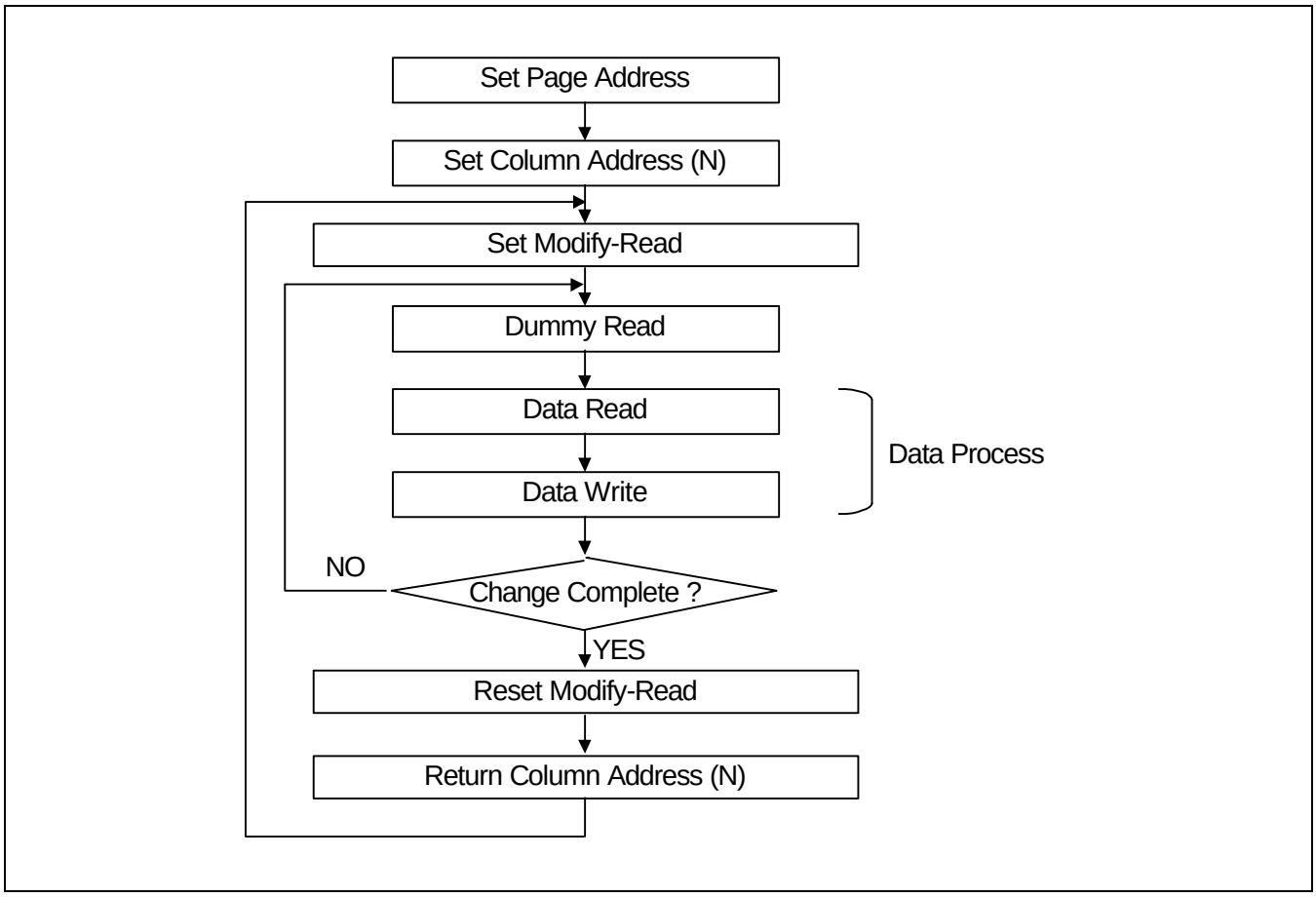

Figure 23. Sequence for Cursor Display

Reset

This instruction resets initial display line, column address, page address, and common output status select to their initial status, but dose not affect the contents of display data RAM. This instruction cannot initialize the LCD power supply, which is initialized by the RESETB pin.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	1	0

SHL Select

COM output scanning direction is selected by this instruction which determines the LCD driver output status.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	0	0	SHL	×	×	×

× : Don't care

SHL = 0: normal direction (COM0 → COM31)
SHL = 1: reverse direction (COM31 → COM0)

Power Control

Selects one of eight power circuit functions by using 3-bit register. An external power supply and part of internal power supply functions can be used simultaneously.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	0	1	VC	VR	VF

VC	VR	VF	Status of internal power supply circuits
0 1			Internal voltage converter circuit is OFF Internal voltage converter circuit is ON
	0 1		Internal voltage regulator circuit is OFF Internal voltage regulator circuit is ON
		0 1	Internal voltage follower circuit is OFF Internal voltage follower circuit is ON

Set Static Indicator State

This instruction sets the Static Indicator on/OFF. When it is ON, the static indicator operates and blinks at an interval of approximately 1 second.

Set Static Indicator Register

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	1	0	SI

SI	Status of Static Indicator Output
0	OFF
1	ON (about 1 second blinking)

Power Save (Compound Instruction)

If the entire display ON / OFF instruction is issued during the display OFF state, KS0716 enters the Power Save status to reduce the power consumption to the static power consumption value. According to the status of static indicator mode, power save is entered to one of two modes (sleep and standby mode). When static indicator mode is ON, standby mode is issued, when OFF, sleep mode is issued. Power Save mode is released by the display ON & entire display OFF instruction.

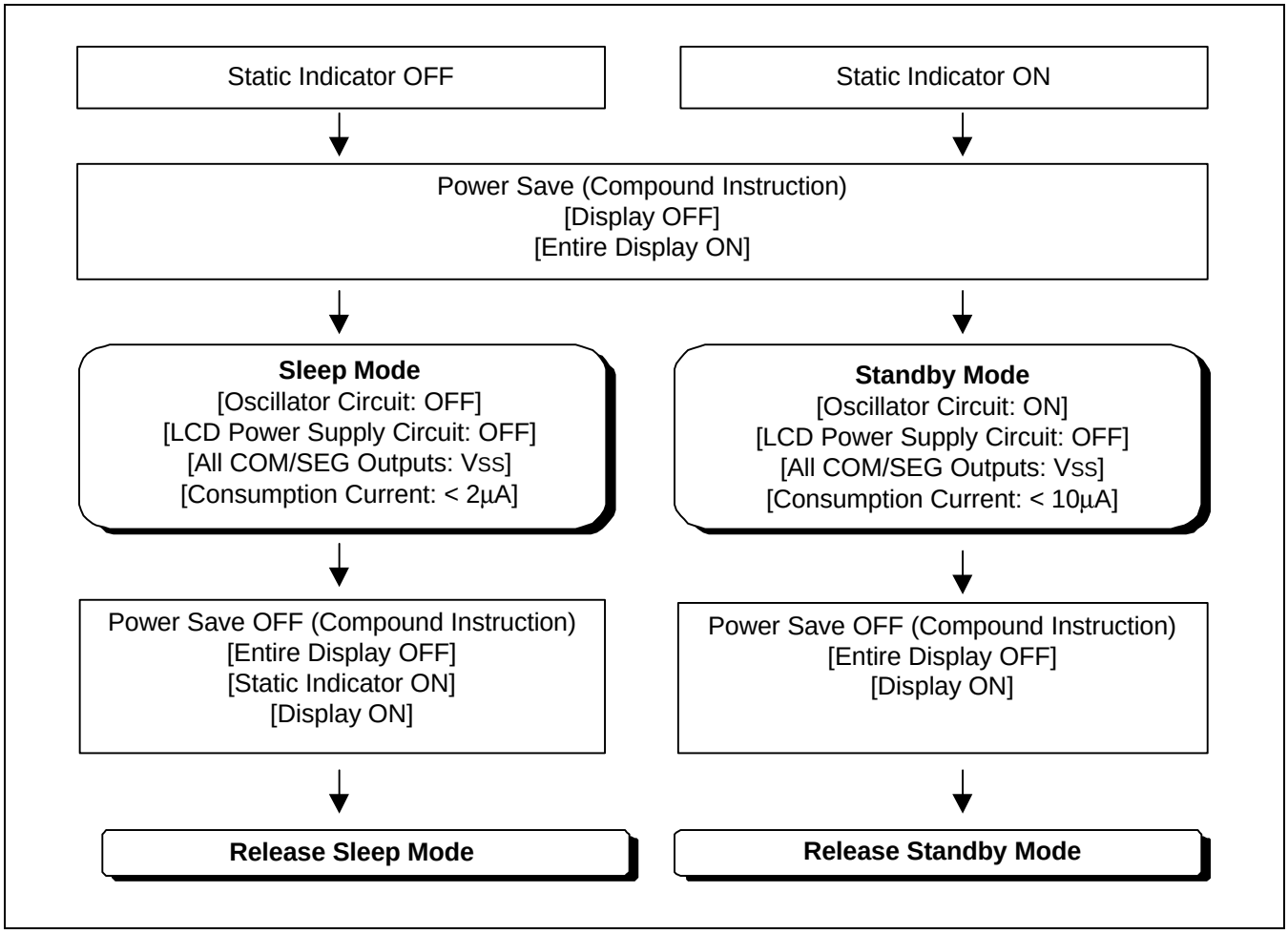

Figure 24. Power Save Routine

Referential Instruction Setup Flow (1)

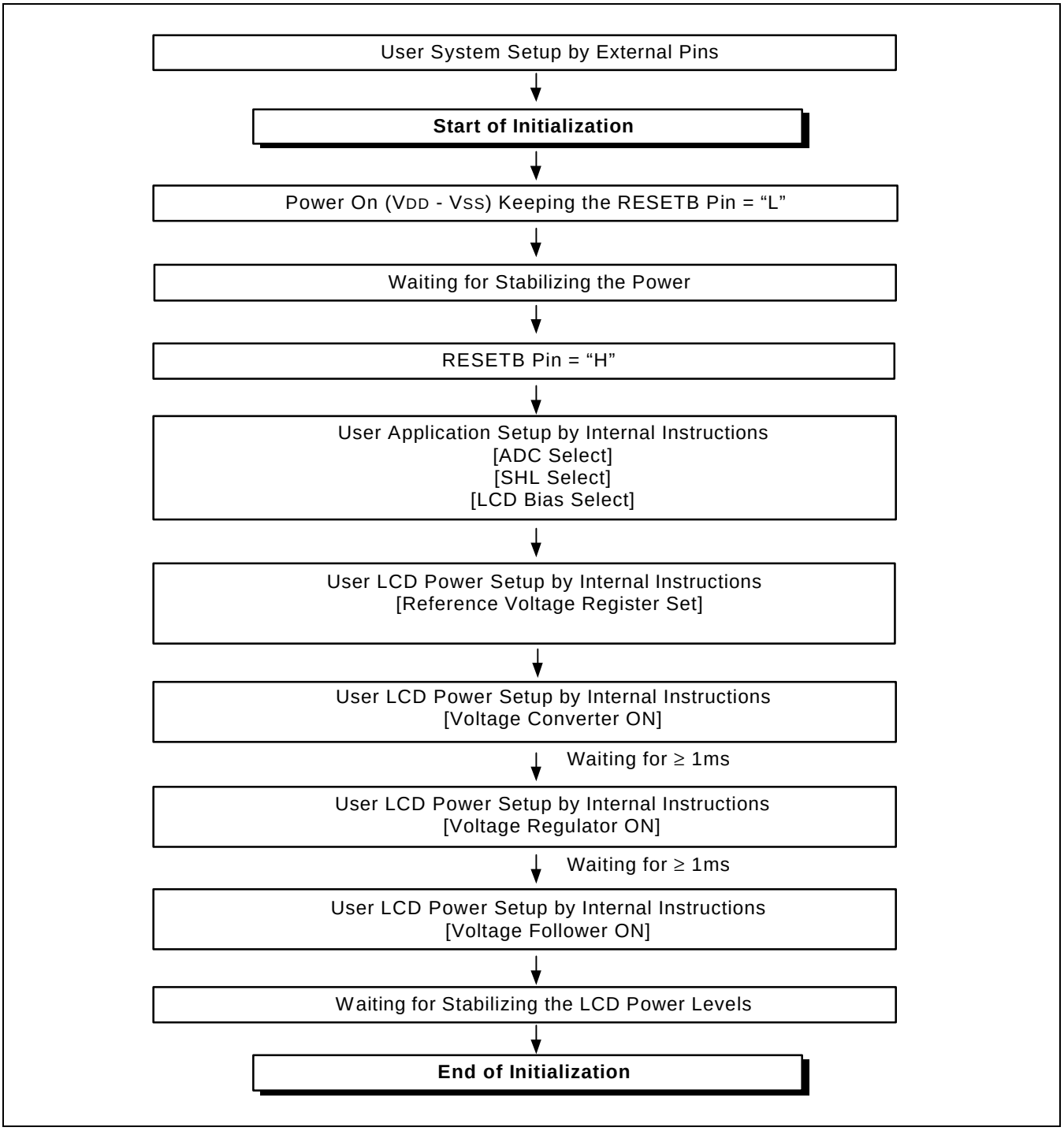

Figure 25. Initializing with the Built-in Power Supply Circuits

Referential Instruction Setup Flow (2)

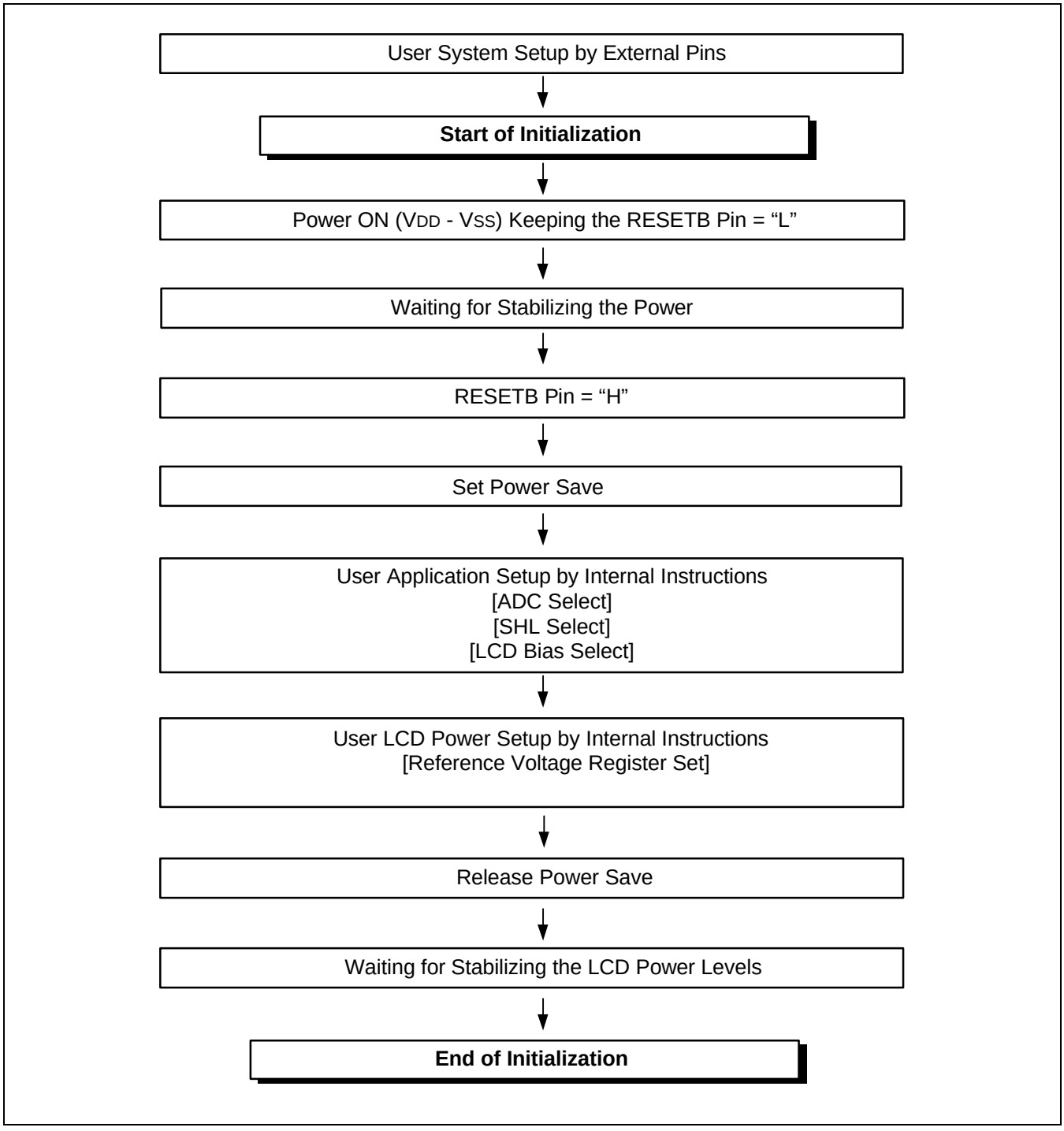

Figure 26. Initializing without the Built-in Power Supply Circuits

Referential Instruction Setup Flow (3)

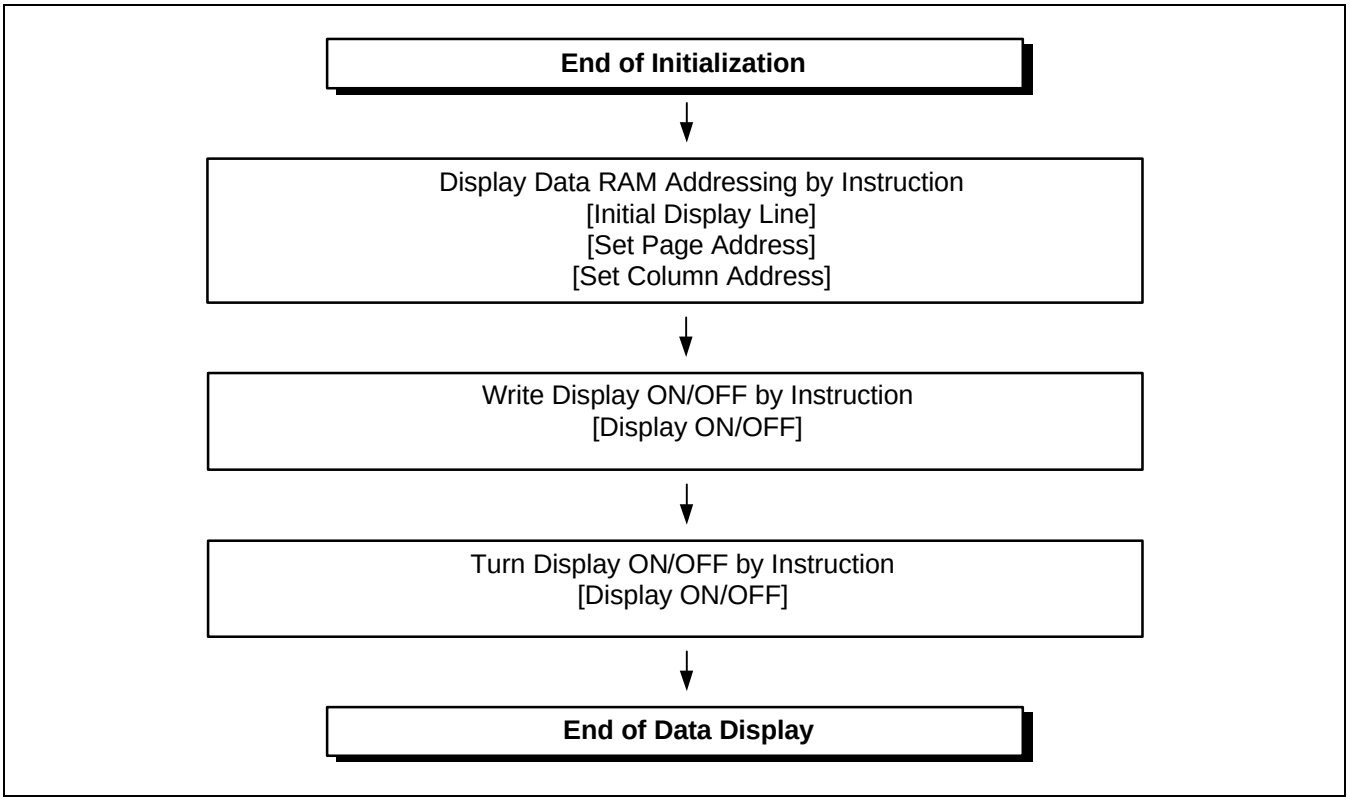

Figure 27. Data Displaying

Referential Instruction Setup Flow (4)

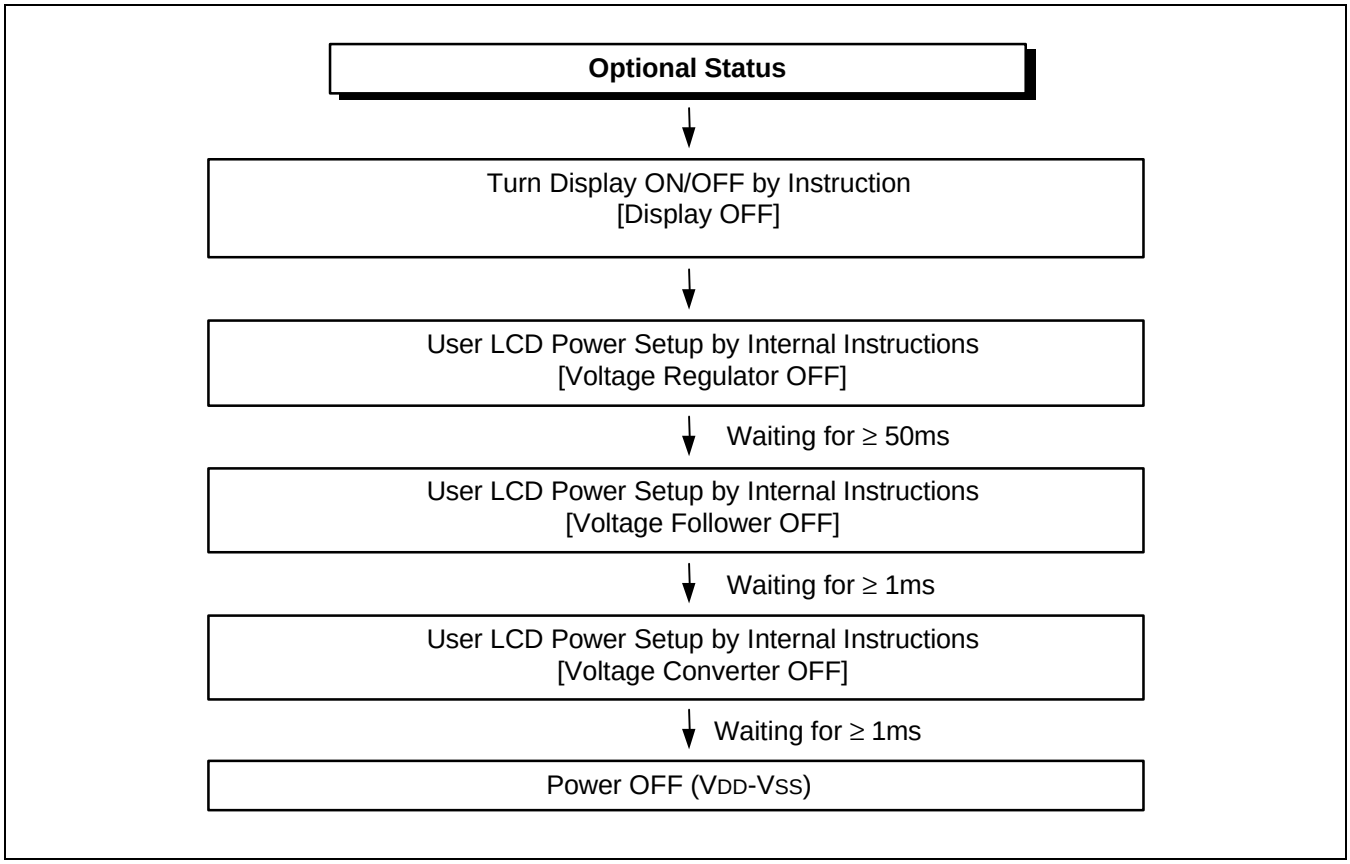

Figure 28. Power OFF

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Table 19. Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{DD}	-0.3 to +7.0	V
	V_{LCD}	-0.3 to +17.0	V
Input voltage range	V_{IN}	-0.3 to V_{DD} +0.3	V
Operating temperature range	T_{OPR}	-40 to +85	°C
Storage temperature range	T_{STR}	-55 to +125	°C

NOTES:

1. V_{DD} and V_{LCD} are based on V_{SS} = 0V.
2. Voltages V0 ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ V_{SS} must always be satisfied. (V_{LCD} = V0 – V_{SS})
3. If supply voltage exceeds its absolute maximum range, this LSI may be damaged permanently. It is desirable to use this LSI under electrical characteristic conditions during general operation. Otherwise, this LSI may malfunction or reduced LSI reliability may result.

DC CHARACTERISTICS

Table 20. DC Characteristics

(V_{SS} = 0V, V_{DD} = 2.4 to 3.6V, Ta = -40 to 85°C)

Item		Symbol	Condition		Min	Typ	Max	Unit	Pin used
Operating voltage (1)		V_{DD}			2.4	-	3.6	V	VDD *1
Operating voltage (2)		V0			4.0	-	15.0	V	V0 *2
Input voltage	High	V_{IH}			0.8V_{DD}	-	V_{DD}	V	*3
	Low	V_{IL}			V_{SS}	-	0.2V_{DD}		
Output voltage	High	V_{OH}	I_{OH} = -0.5mA		0.8V_{DD}	-	V_{DD}	V	*4
	Low	V_{OL}	I_{OL} = 0.5mA		V_{SS}	-	0.2V_{DD}		
Input leakage current		I_{IL}	V_{IN} = V_{DD} or V_{SS}		- 1.0	-	+ 1.0	µA	*5
Output leakage current		I_{OZ}	V_{IN} = V_{DD} or V_{SS}		- 3.0	-	+ 3.0	µA	*6
LCD driver ON resistance		R_{ON}	Ta = 25°C, V0 = 8V		-	2.0	3.0	kΩ	SEGn COMn *7
Oscillator frequency(1)	Internal	f_{OSC}	Ta = 25°C		17	22.5	27	kHz	CL *8
	External	f_{CL}			2.13	2.81	3.37		
Voltage converter input voltage		V_{DD}	× 2		2.4	-	3.6	V	VDD
			× 3		2.4	-	3.6		
			× 4		2.4	-	3.6		
Voltage converter output voltage		V_{OUT}	×2 / ×3 / ×4 voltage conversion (no-load)		95	99	-	%	VOUT
Voltage regulator operating voltage		V_{OUT}			4.0	-	15.0	V	VOUT
Voltage follower operating voltage		V0			4.0	-	15.0	V	V0 *9
Reference voltage		V_{REF0}	Ta = 25°C	-0.05%/°C	1.84	1.9	1.96	V	*10
		V_{REF1}	Ta = 25°C	-0.2%/°C	2.04	2.1	2.16		

Dynamic Current Consumption (1) when the Built-in Power Circuit is OFF (At Operate Mode)

(Ta = 25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Dynamic current consumption (1)	I_{DD1}	V_{DD} = 3.0V V0 – V_{SS} = 8.0V Display OFF	-	5	20	μA	*11

Dynamic Current Consumption (2) when the Built-in Power Circuit is ON (At Operate Mode)

(Ta = 25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Dynamic current consumption (2)	I_{DD2}	V_{DD} = 3.0V, Quad boosting, V0 – V_{SS} = 8.0V, Display OFF Normal power mode	-	47	70	μA	*12
		V_{DD} = 3.0V, Quad boosting, V0 – V_{SS} = 8.0V, Display ON, checker pattern Normal power mode	-	75	100		

Current Consumption during Power Save mode

(Ta = 25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Sleep mode	I_{DDS1}	During sleep	-	-	2.0	μA	
Standby mode	I_{DDS2}	During standby	-	-	10.0	μA	

Table 21. The Relationship between Oscillation Frequency and Frame Frequency

Duty Ratio	Item	f_{CL}	f_M
1/33	On-chip oscillator circuit is used	$\frac{f_{OSC}}{8}$	$\frac{f_{OSC}}{16 \times 33}$
	On-chip oscillator circuit is not used	External input (f_{CL})	$\frac{f_{OSC}}{2 \times 33}$

(f_{OSC}: oscillation frequency, f_{CL}: display clock frequency, f_M: LCD AC signal frequency)

[* Remark Solves]
*1. Though the wide range of operating voltages is guaranteed, a spike voltage change may affect the voltage assurance during access from the MPU.
*2. In case of external power supply is applied.
*3. CS1B, CS2, RS, DB0 to DB7, E_RD, RW_WR, RESETB, MS, MI, PS, TEMPS, CL, M, DISP pins.
*4. DB0 to DB7, M, FRS, DISP, CL pins.
*5. CS1B, CS2, RS, DB[7:0], E_RD, RW_WR, RESETB, MS, MI, PS, TEMPS, CL, M, DISP pins.
*6. Applies when the DB[7:0], M, DISP, and CL pins are in high impedance.
*7. Resistance value when ± 0.1[mA] is applied during the ON status of the output pin SEGn or COMn.
RON= ΔV / 0.1 [kΩ] (ΔV: voltage change when ± 0.1[mA] is applied in the ON status.)
*8. See table 21 for the relationship between oscillation frequency and frame frequency.
*9. The voltage regulator circuit adjusts V0 within the voltage follower operating voltage range
*10. On-chip reference voltage source of the voltage regulator circuit to adjust V0.
*11,12. Applies to the case where the on-chip oscillation circuit is used and no access is made from the MPU.
The current consumption, when the built-in power supply circuit is ON or OFF.
The current flowing through voltage regulation resistors (Ra and Rb) is not included.
It does not include the current of the LCD panel capacity, wiring capacity, etc

REFERENCE DATA

I_{DD1} vs. V_{DD}

* Test Condition: Temperature (25°C & 85°C), V0 = 8V(External), TEMPS = 'L', 1/33 Duty, Ra = 1 [MΩ], Rb = 3 [MΩ], Normal Power Mode

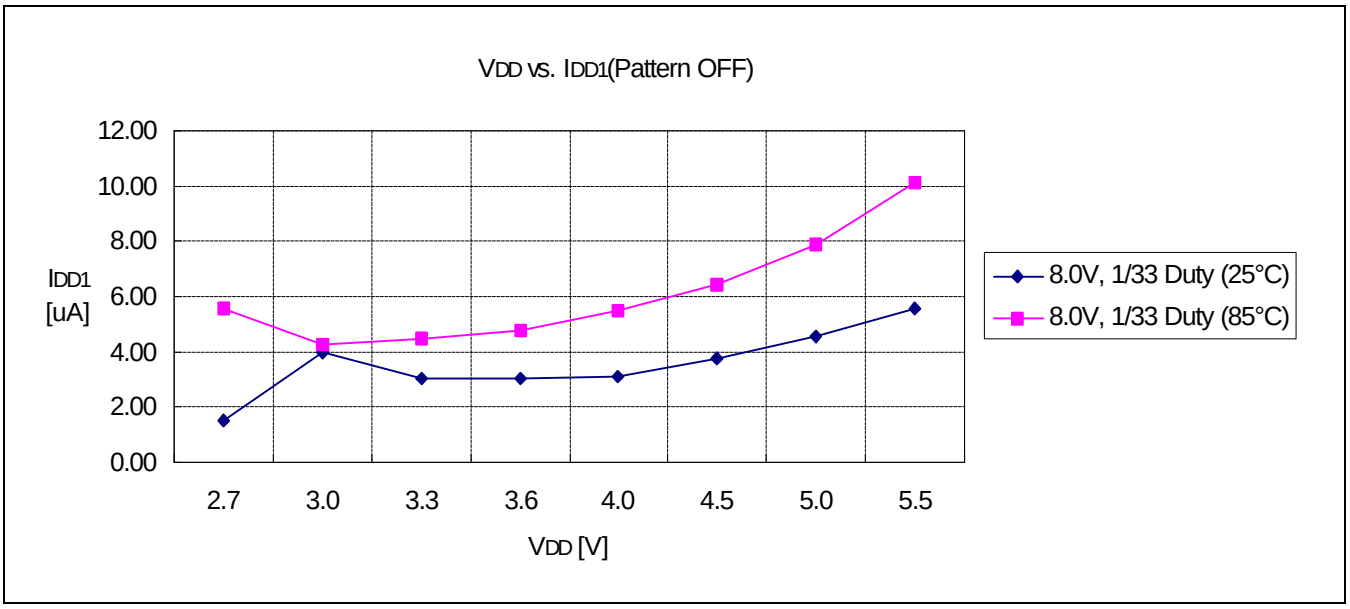

Figure 29. Display Pattern is OFF

IDD2 vs. VDD

Test Condition: Temperature (25°C & 85°C), Quad Boosting, RR=6, EV=32, TEMPS = 'L', 1/33 Duty,
Ra = 1 [MΩ], Rb = 3 [MΩ], Normal Power Mode

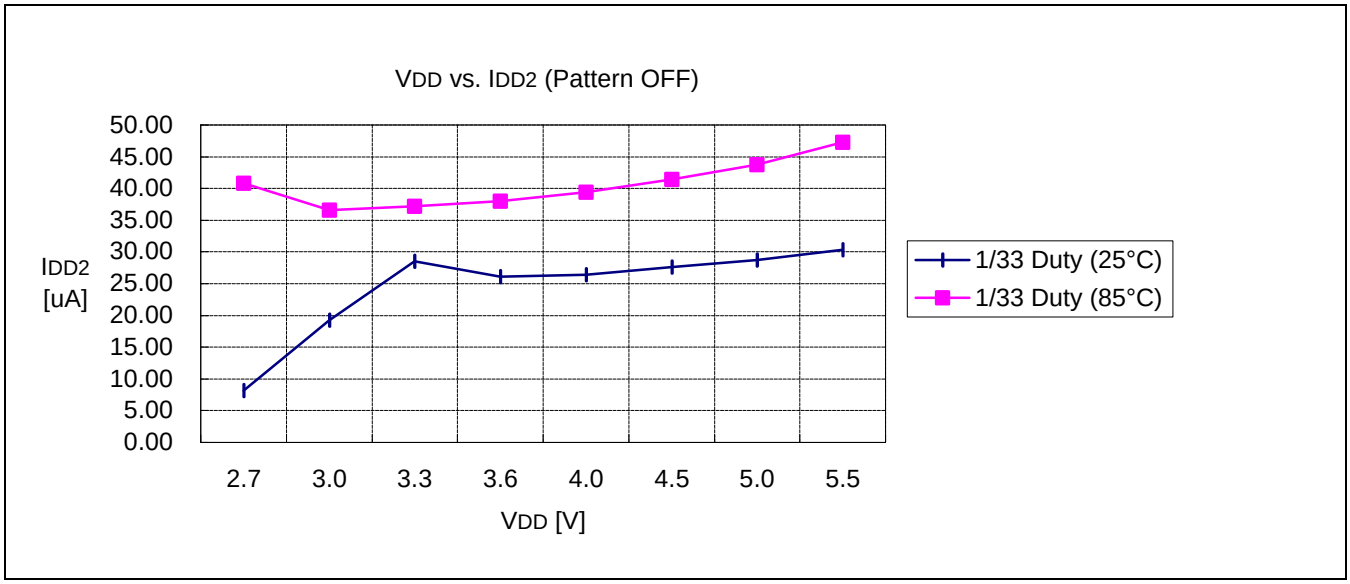

Figure 30. Display Pattern is OFF

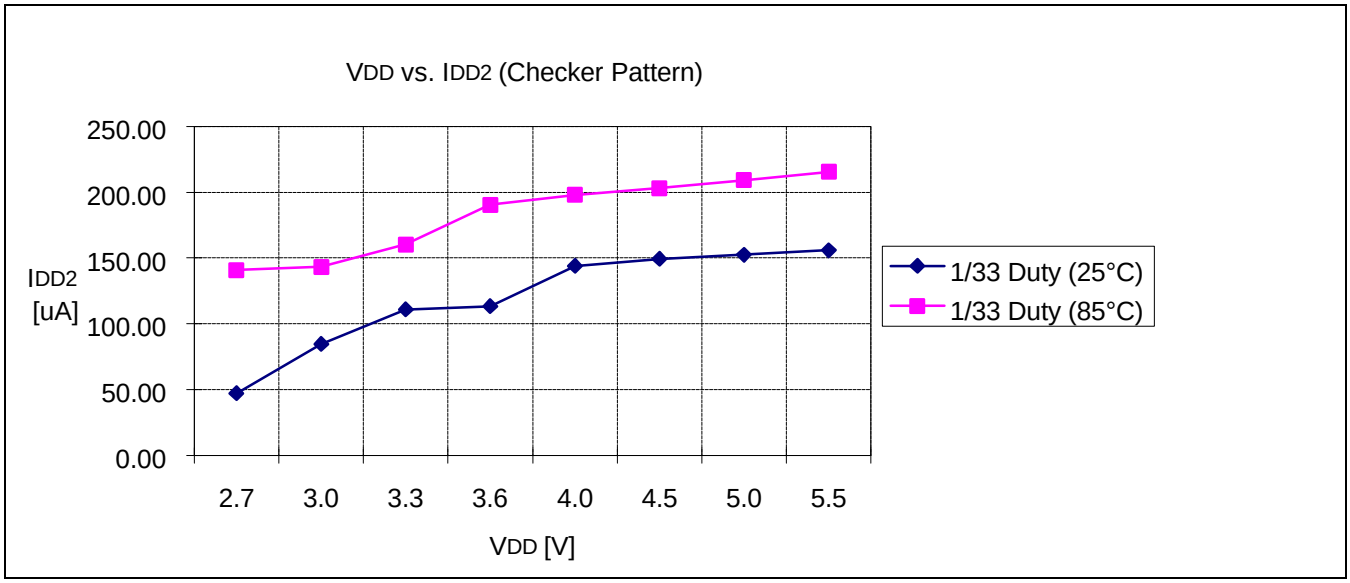

Figure 31. Display Pattern is Checker

AC CHARACTERISTICS

Read / Write Characteristics (8080-series MPU)

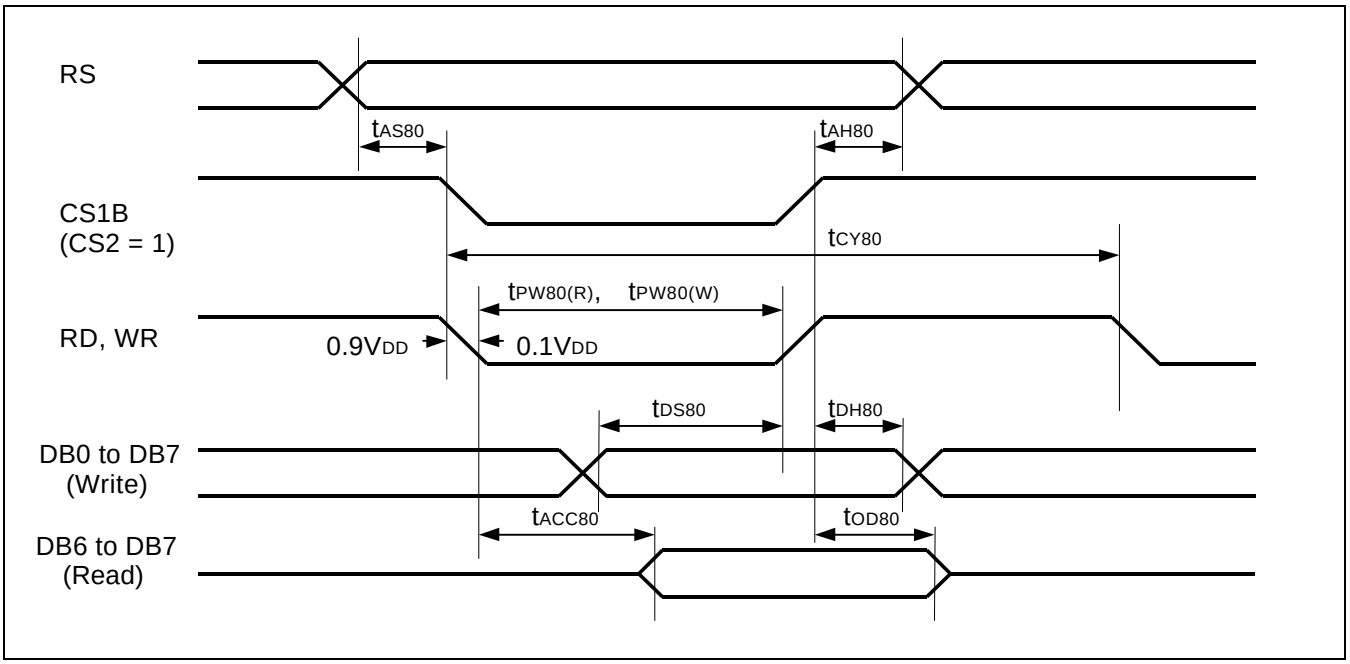

Figure 32. Read / Write Characteristics (8080-series MPU)

(V_{DD} = 2.4 to 3.6V, Ta = -40 to +85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Address setup time Address hold time	RS	t_{AS80} t_{AH80}	13 17	-	-	ns	
System cycle time	RS	t_{CY80}	400	-	-	ns	
Pulse width(WR)	RW_WR	$t_{PW80(W)}$	55	-	-	ns	
Pulse width(RD)	E_RD	$t_{PW80(R)}$	125	-	-	ns	
Data setup time Data hold time	DB7 to DB0	t_{DS80} t_{DH80}	35 13	-	-	ns	
Read access time Output disable time	DB7 to DB0	t_{ACC80} t_{OD80}	- 10	-	125 90	ns	C_L = 100 pF

Read / Write Characteristics (6800-series Microprocessor)

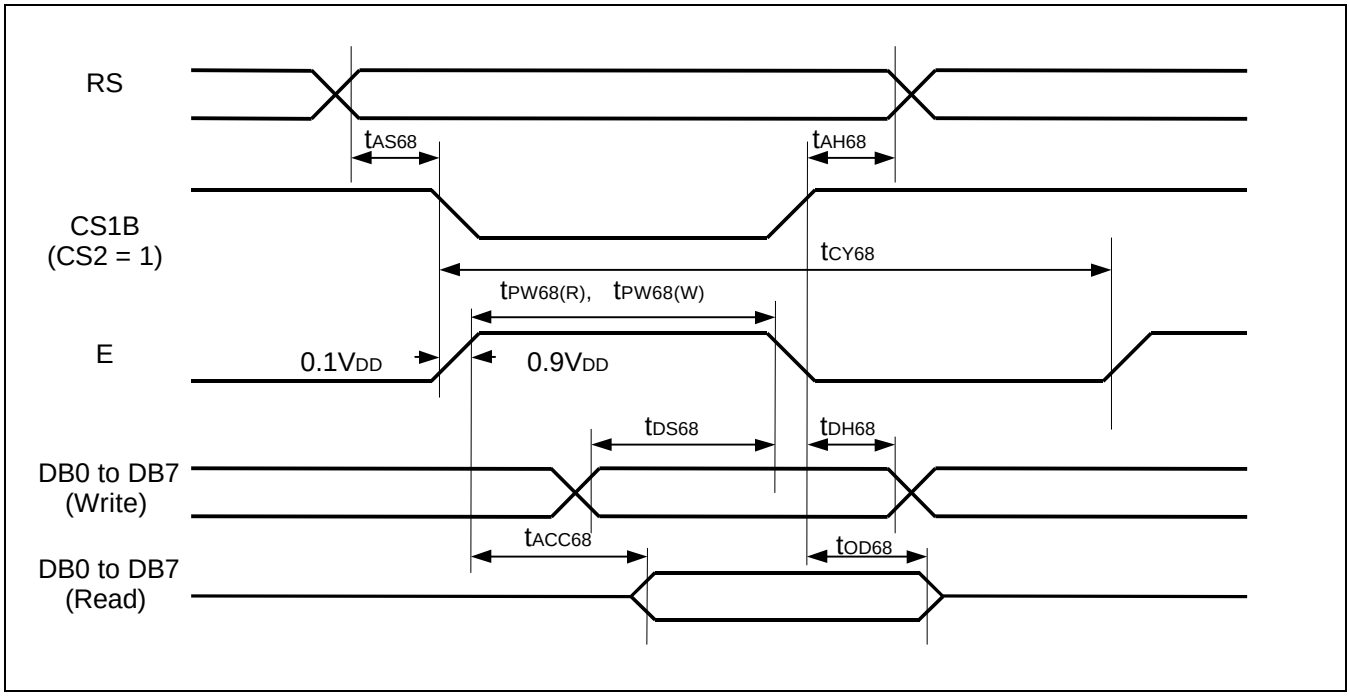

Figure 33. Read / Write Characteristics (6800-series Microprocessor)

(V_{DD} = 2.4 to 3.6V, Ta = -40 to +85°C)

Item		Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Address setup time Address hold time		RS	t_{AS68} t_{AH68}	13 17	-	-	ns	
System cycle time		RS	t_{CY68}	400	-	-	ns	
Data setup time Data hold time		DB7 to DB0	t_{DS68} t_{DH68}	35 13	-	-	ns	
Access time Output disable time			t_{ACC68} t_{OD68}	- 10	-	125 90	ns	C_L = 100 pF
Enable pulse width	Read Write	E_RD	$t_{PW68(R)}$ $t_{PW68(W)}$	125 55	-	-	-	

Serial Interface Characteristics

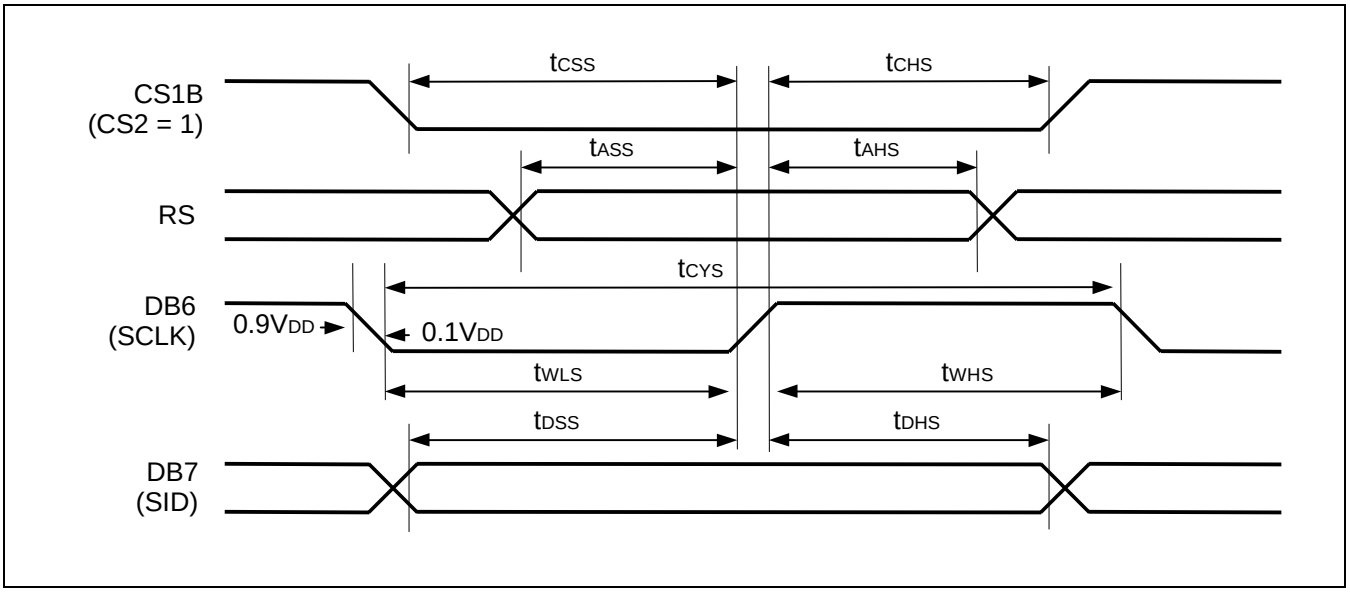

Figure 34. Serial Interface Characteristics

(V_{DD} = 2.4 to 3.6V, Ta = -40 to +85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Serial clock cycle SCLK high pulse width SCLK low pulse width	DB6 (SCLK)	t_{CYS} t_{WHS} t_{WLS}	450 180 135	- - -	- - -	ns	
Address setup time Address hold time	RS	t_{ASS} t_{AHS}	90 360	- -	- -	ns	
Data setup time Data hold time	DB7 (SID)	t_{DSS} t_{DHS}	90 90	- -	- -	ns	
CS1B setup time CS1B hold time	CS1B	t_{CSS} t_{CHS}	55 180	- -	- -	ns	

Reset Input Timing

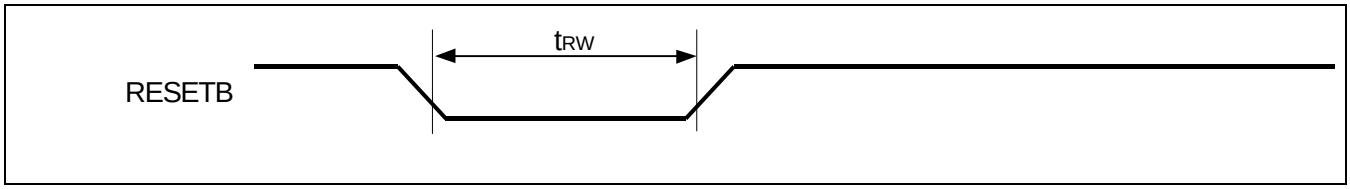

Figure 35. Reset Input Timing

(V_{DD} = 2.4 to 3.6V, Ta = -40 to +85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Reset low pulse width	RESETB	t_{RW}	900	-	-	ns	

Display Control Output Timing

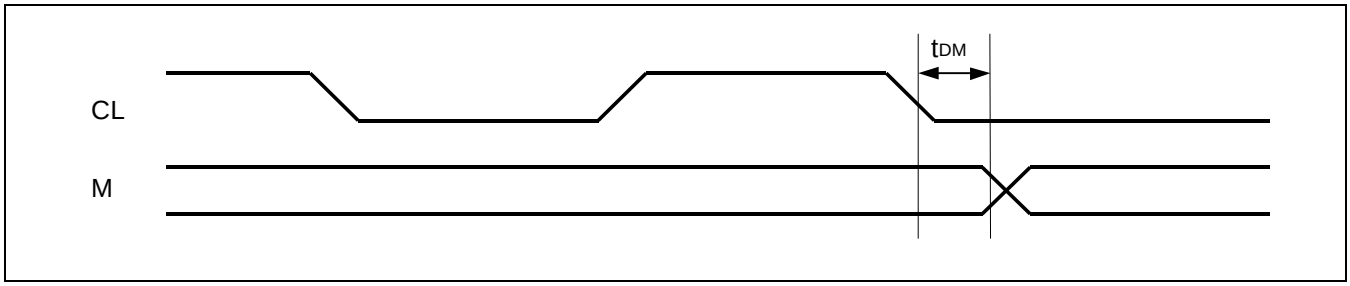

Figure 36. Display Control Output Timing

(V_{DD} = 2.4 to 3.6V, Ta = -40 to +85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
M delay time	M	t_{DM}	-	13	70	ns	

REFERENCE APPLICATIONS

MICROPROCESSOR INTERFACE

In Case of Interfacing with 6800-series (PS = “H”, MI = “H”)

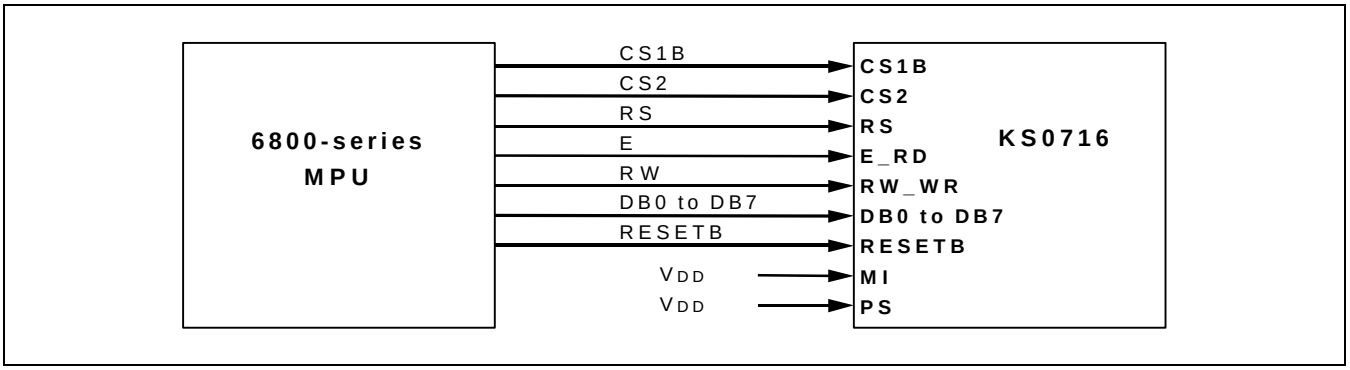

Figure 37. Interfacing with 6800-series (PS = “H”, MI = “H”)

In Case of Interfacing with 8080-series (PS = “H”, MI = “L”)

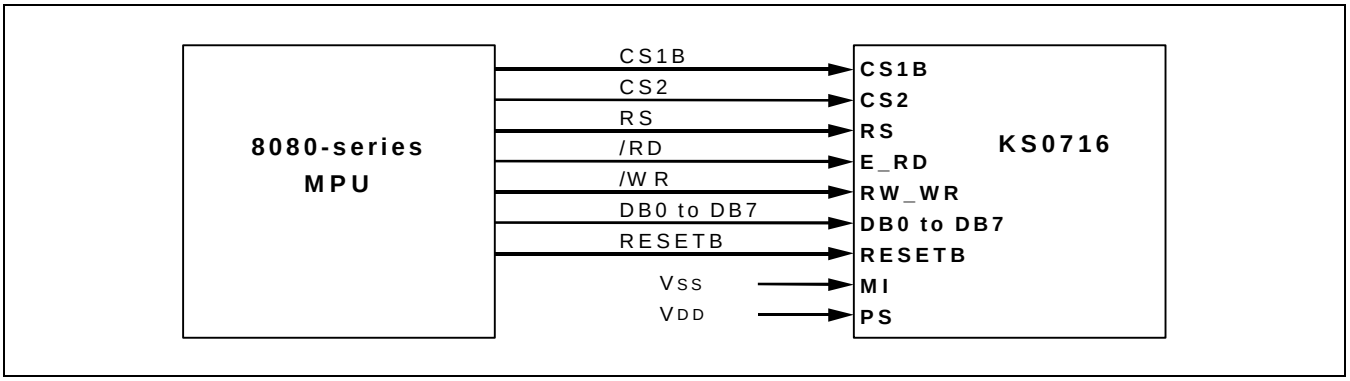

Figure 38. Interfacing with 8080-series (PS = “H”, MI = “L”)

In Case of Serial Interface (PS = “L”, MI = “H/L”)

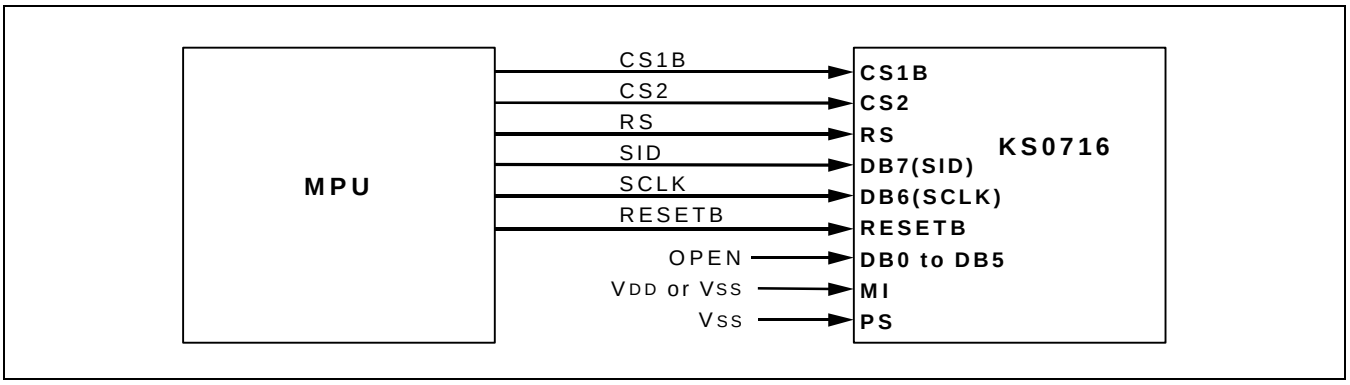

Figure 39. Serial Interface (PS = “L”, MI = “H/L”)