Document Title

64Kx18-Bit Synchronous Burst SRAM, 5V Power
Data Sheets for 52 PLCC

Revision History

Rev.No.	History	Draft Date	Remark
Rev. 1.0	- Final specification release		Final
Rev. 1.1	- Change specification format. No change was made in parameters.	April, 1997	Final

64Kx18-Bit Synchronous Burst SRAM

FEATURES

- Synchronous Operation.
- On-Chip Address Counter.
- Self-Timed Write Cycle.
- On-Chip Address and Control Registers.
- Single 5V±5% Power Supply.
- Byte Writable Function.
- Asynchronous Output Enable Control.
- ADSP, ADSC, ADV Burst Control Pins.
- TTL-Level Three-State Output.
- 3.3V I/O Compatible.
- 52-Pin PLCC Package.

FAST ACCESS TIMES

Parameter	Symbol	-8	-9	-10	-12	Unit
Cycle Time	t_{CYC}	15	15	17	20	ns
Clock Access Time	t_{CD}	8	9	10	12	ns
Output Enable Access	t_{OE}	5	5	5	6	ns

GENERAL DESCRIPTION

The KM718B86 is a 1,179,648 bits Synchronous Static Random Access Memory designed to support 66MHz of Intel secondary caches.

It is organized as 65,536 words of 18bits and integrates address and control registers, a 2-bit burst address counter and high output drive circuitry onto a single integrated circuit for reduced components count implementations of high performance cache RAM applications.

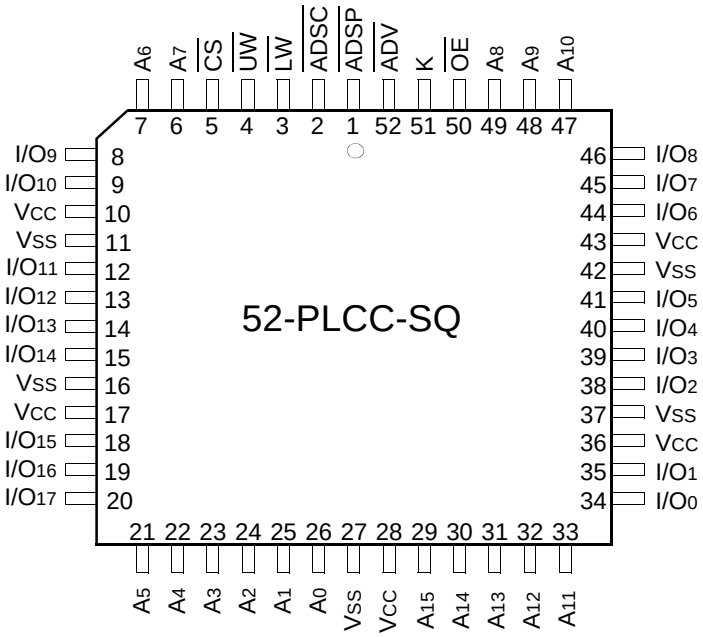
Write cycles are internally self-timed and synchronous.

The self-timed write feature eliminates complex off chip write pulse shaping logic, simplifying the cache design and further reducing the component count.

Burst cycle can be initiated with either the address status processor($\overline{ADSP}$) or address status cache controller($\overline{ADSC}$) inputs. Subsequent burst addresses are generated internally in the system′s burst sequence and are controlled by the burst address advance($\overline{ADV}$) input.

The KM718B86 is implemented with SAMSUNG′s high performance BiCMOS technology and is available in a 52pin PLCC package. Multiple power and ground pins are utilized to minimize ground bounce.

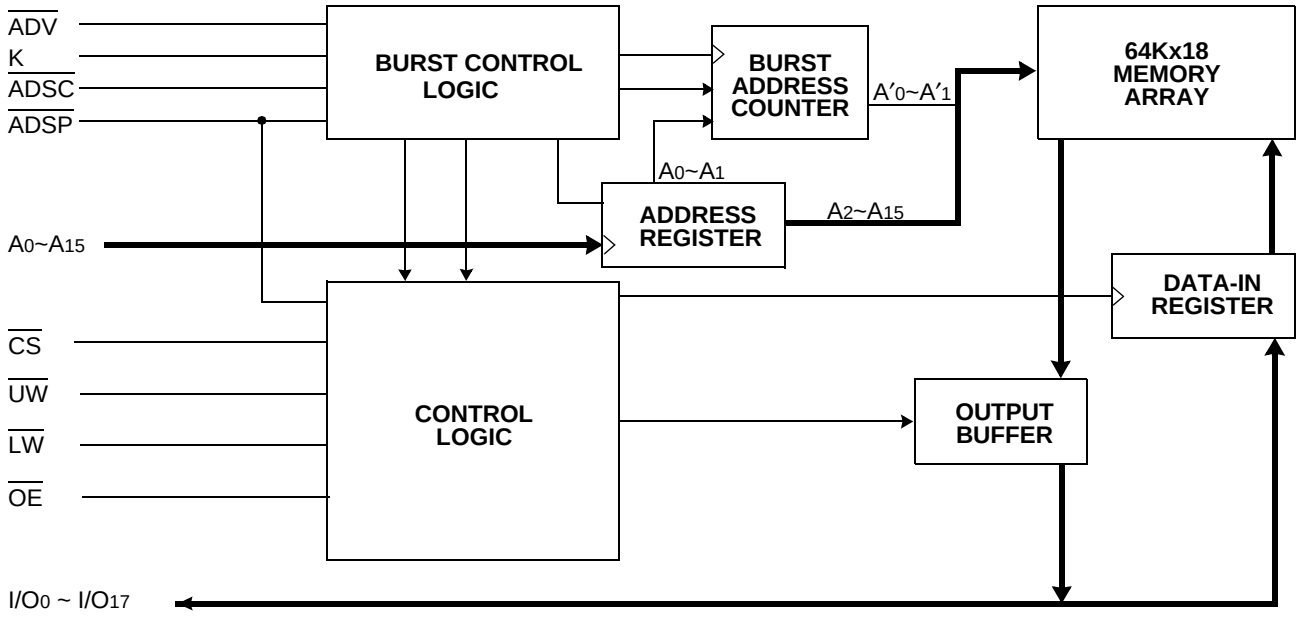
PIN CONFIGURATION(TOP VIEW)



PIN NAME

Pin Name	Pin Function
A_0 - A_{15}	Address Inputs
K	Clock
$\overline{LW}$, $\overline{UW}$	Write Enable
$\overline{CS}$	Chip Selects
$\overline{OE}$	Output Enable
$\overline{ADV}$	Burst Address Advance
$\overline{ADSP}$, $\overline{ADSC}$	Address Status
I/O_0~I/O_{17}	Data Inputs/Outputs
V_{CC}	+5V Power Supple
V_{SS}	Ground

LOGIC BLOCK DIAGRAM



FUNCTION DESCRIPTION

The KM718B86 is a synchronous SRAM designed to support the burst address accessing sequence of the Power microprocessor. All inputs(with the exception of OE) are sampled on rising clock edges. The start and duration of the burst access is controlled by ADSP and ADSC. The accesses are enabled with the chip select signals and output enable. Wait states are inserted into the access with ADV.

Read cycles are initiated with ADSP(regardless of LW, UW and ADSC) using the new external address clocked into the on-chip address register whenever ADSP is sample low, The chip selects are sampled active, and the output buffer is enabled with OE, ADV is ignored on the clock edge that samples ADSP asserted, but is sampled on the next and subsequent clock edges. The address is increased internally for the next access of the burst when LW, UW is sampled HIGH and ADV is sampled low.

Write cycles are performed by disabling the output buffers with OE and asserting LW, UW. LW, UW is ignored on the clock edge that sampled ADSP low, but is sampled on the next and subsequent clock edges. The output buffers are disabled when LW, UW is sampled low (regardless of OE). Data is clocked into the input register when LW, UW is sampled low. The address increases internally to the next address of burst, if both LW, UW and ADV are sampled Low. Individual byte write cycles are performed sampling low only one byte write enable signals(LW or LU)and LW controls I/O0~I/O7 and UW controls I/O8~I/O17.
Read or write cycles (depending on LW, LU)may also be initiated with ADSC, instead of ADSP. The differences between cycles initiated with ADSC and ADSP are as follows;

ADSP must be sampled high when ADSC is sampled low to initiate a cycle with ADSC.
LW, UW is sampled on the same clock edge that sampled ADSC low(and ADSP high).

Addresses are generated for the burst accesses as shown below. The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion.

BURST SEQUENCE TABLE

(Interleaved Burst)

	Case 1		Case 2		Case 3		Case 4	
	A1	**A0**	**A1**	**A0**	**A1**	**A0**	**A1**	**A0**
First Address	0	0	0	1	1	0	1	1
	0	1	0	0	1	1	1	0
	1	0	1	1	0	0	0	1
Fourth Address	1	1	1	0	0	1	0	0

TRUTH TABLES

SYNCHRONOUS TRUTH TABLE(See Notes 1 and 2)

$\overline{CS}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{LW}$/$\overline{UW}$	K	Address Accessed	Operation
H	L	X	X	X	↑	N/A	Not Selected
H	X	L	X	X	↑	N/A	Not Selected
L	L	X	X	X	↑	External Address	Begin Burst Read Cycle
L	H	L	X	H	↑	External Address	Begin Burst Read Cycle
X	H	H	L	H	↑	Next Address	Continue Burst Read Cycle
X	H	H	H	H	↑	Current Address	Suspend Burst Read Cycle
L	H	L	X	L	↑	External Address	Begin Burst Write Cycle
X	H	H	L	L	↑	Next Address	Continue Burst Write Cycle
X	H	H	H	L	↑	Current Address	Suspend Burst Write Cycle

NOTE1 : X means "Don't Care".

NOTE2 : The rising edge of clock is symbolized by ↑.

ASYNCHRONOUS TRUTH TABLE(See Notes 1 and 2)

$\overline{OE}$	Operation
L	Read I/O_0~I/O_{17}
H	Output High-Z
X	Not Selected, Outputs High-Z

NOTE1 : X means "Don't Care".

NOTE2 : For write cycles that following read cycles, the output buffers must be disabled with OE, otherwise data bus contention will occur.

ABSOLUTE MAXIMUM RATING*

Parameter	Symbol	Rating	Unit
Voltage on V_{DD} Supply Relative to V_{SS}	V_{CC}	-0.5 to 7.0	V
Voltage on Any Other Pin Relative to V_{SS}	V_{IN}	-0.5 to 7.0	V
Power Dissipation	P_D	1.2	W
Storage Temperature	T_{STG}	-65 to 150	°C
Operating Temperature	T_{OPR}	0 to 70	°C
Storage Temperature Range Under Bias	T_{BIAS}	-10 to 85	°C

*NOTE : Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING CONDITIONS($0°C \leq T_A \leq 70°C$)

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
Ground	V_{SS}	0	0	0	V

CAPACITANCE*(T_A=25°C, f=1MHz)

Parameter	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	5	pF
Output Capacitance	C_{OUT}	V_{OUT}=0V	-	8	pF

*NOTE : Sampled not 100% tested.

TEST CONDITIONS(T_A= 0 to 70°C, V_{DD}=5V±5%, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time(Measured at 0.3V and 2.7V)	2ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig. 1

DC ELECTRICAL CHARACTERISTICS(T_A=0 to 70°C, V_{DD}=3.3V±5%)

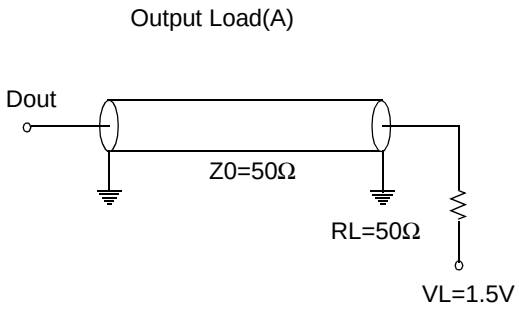
Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current(except ZZ)	I_{IL}	V_{DD}=Max ; V_{IN}=V_{SS} to V_{CC}		-2	+2	µA
Output Leakage Current	I_{OL}	Output Disabled		-2	+2	µA
Operating Current	I_{CC}	V_{CC}=Max I_{OUT}=0mA Cycle Time≥t_{CYC} min	15ns	-	270	mA
			17ns	-	260	
			20ns	-	250	
Standby Current	I_{SB}	Device deselected, I_{OUT}=0mA, Min Cycle All Inputs=V_{IH} and V_{IL}, V_{IH}≥3V and V_{IL}=0V		-	90	mA
Output Low Voltage	V_{OL}	I_{OL}=8.0mA		-	0.4	V
Output High Voltage	V_{OH}	I_{OH}=-4.0mA		2.4	3.3	V
Input Low Voltage	V_{IL}			-0.5*	0.8	V
Input High Voltage	V_{IH}			2.2	Vcc+0.5	V

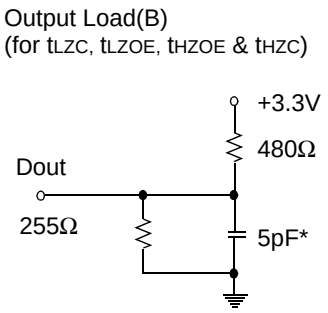
* V_{IL}(Min)=-3.0(Pulse Width≤20ns)

AC TIMING CHARACTERISTICS(T_A=0 to 70°C, V_{CC}=5V±5%)

Parameter	Symbol	KM718B86-8		KM718B86-9		KM718B86-10		KM718B86-12		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Cycle Time	t_{CYC}	15	-	15	-	17	-	20	-	ns
Clock Access Time	t_{CD}	-	8	-	9	-	10	-	12	ns
Output Enable to Data Valid	t_{OE}	-	5	-	5	-	5	-	6	ns
Clock High to Output Low-Z	t_{LZC}	6	-	6	-	6	-	6	-	ns
Output Hold from Clock High	t_{OH}	3	-	3	-	3	-	3	-	ns
Output Enable Low to Output Low-Z	t_{LZOE}	0	-	0	-	0	-	0	-	ns
Output Enable High to Output High-Z	t_{HZOE}	2	5	2	5	2	5	2	5	ns
Clock High to Output High-Z	t_{HZC}	-	6	-	6	-	6	-	6	ns
Clock High Pulse Width	t_{CH}	5	-	5	-	5	-	6	-	ns
Clock Low Pulse Width	t_{CL}	5	-	5	-	5	-	6	-	ns
Address Setup to Clock High	t_{AS}	2.5	-	2.5	-	2.5	-	2.5	-	ns
Address Status Setup to Clock High	t_{SS}	2.5	-	2.5	-	2.5	-	2.5	-	ns
Data Setup to Clock High	t_{DS}	2.5	-	2.5	-	2.5	-	2.5	-	ns
Write Setup to Clock High	t_{WS}	2.5	-	2.5	-	2.5	-	2.5	-	ns
Address/Advance Setup to Clock	t_{ADVS}	2.5	-	2.5	-	2.5	-	2.5	-	ns
Chip Select Setup to Clock High	t_{CSS}	2.5	-	2.5	-	2.5	-	2.5	-	ns
Address Hold from Clock High	t_{AH}	0.5	-	0.5	-	0.5	-	0.5	-	ns
Address Status Hold from Clock High	t_{SH}	0.5	-	0.5	-	0.5	-	0.5	-	ns
Data Hold from Clock High	t_{DH}	0.5	-	0.5	-	0.5	-	0.5	-	ns
Write Hold from Clock High	t_{WH}	0.5	-	0.5	-	0.5	-	0.5	-	ns
Address Advance Hold from Clock	t_{ADVH}	0.5	-	0.5	-	0.5	-	0.5	-	ns
Chip Select Hold from Clock High	t_{CSH}	0.5	-	0.5	-	0.5	-	0.5	-	ns

NOTE : All address inputs must meet the specified setup and hold times for all rising clock edges whenever ADSC and/or ADSP is sampled low and CS is sampled low. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected. Both chip selects must be active whenever ADSC or ADSP is sampled low in order for this device to remain enabled.

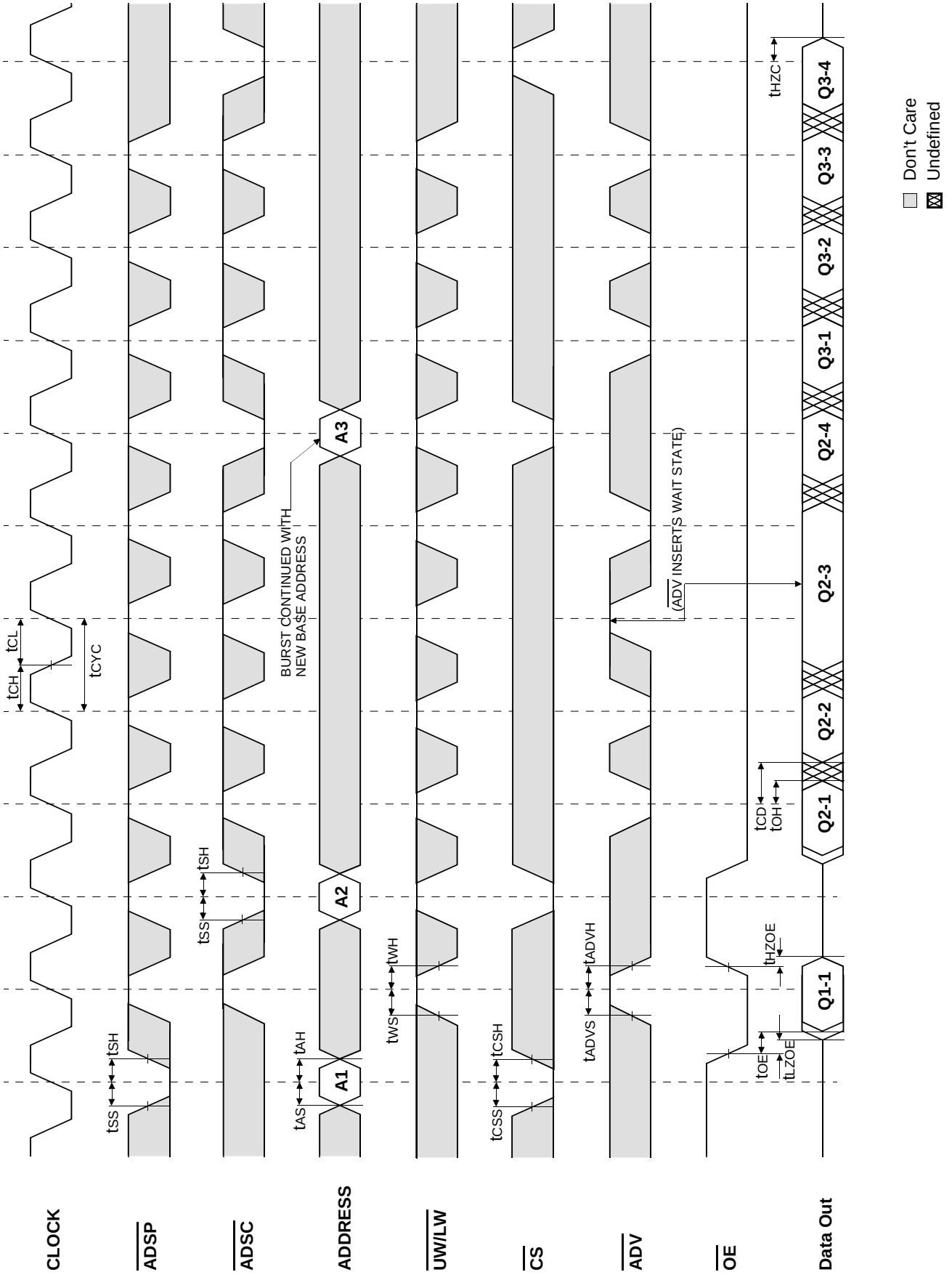




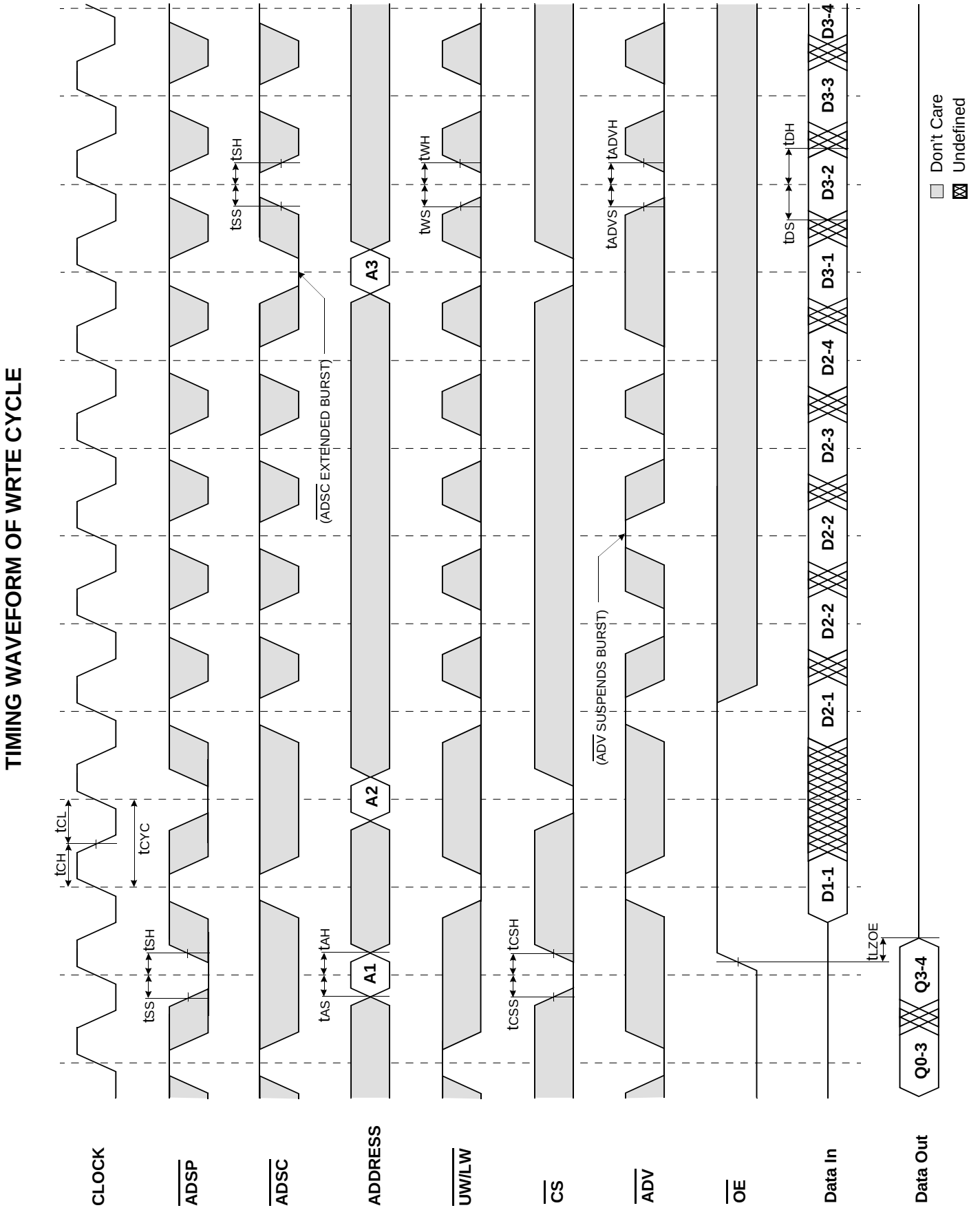
* Including Scope and Jig Capacitance

Fig. 1

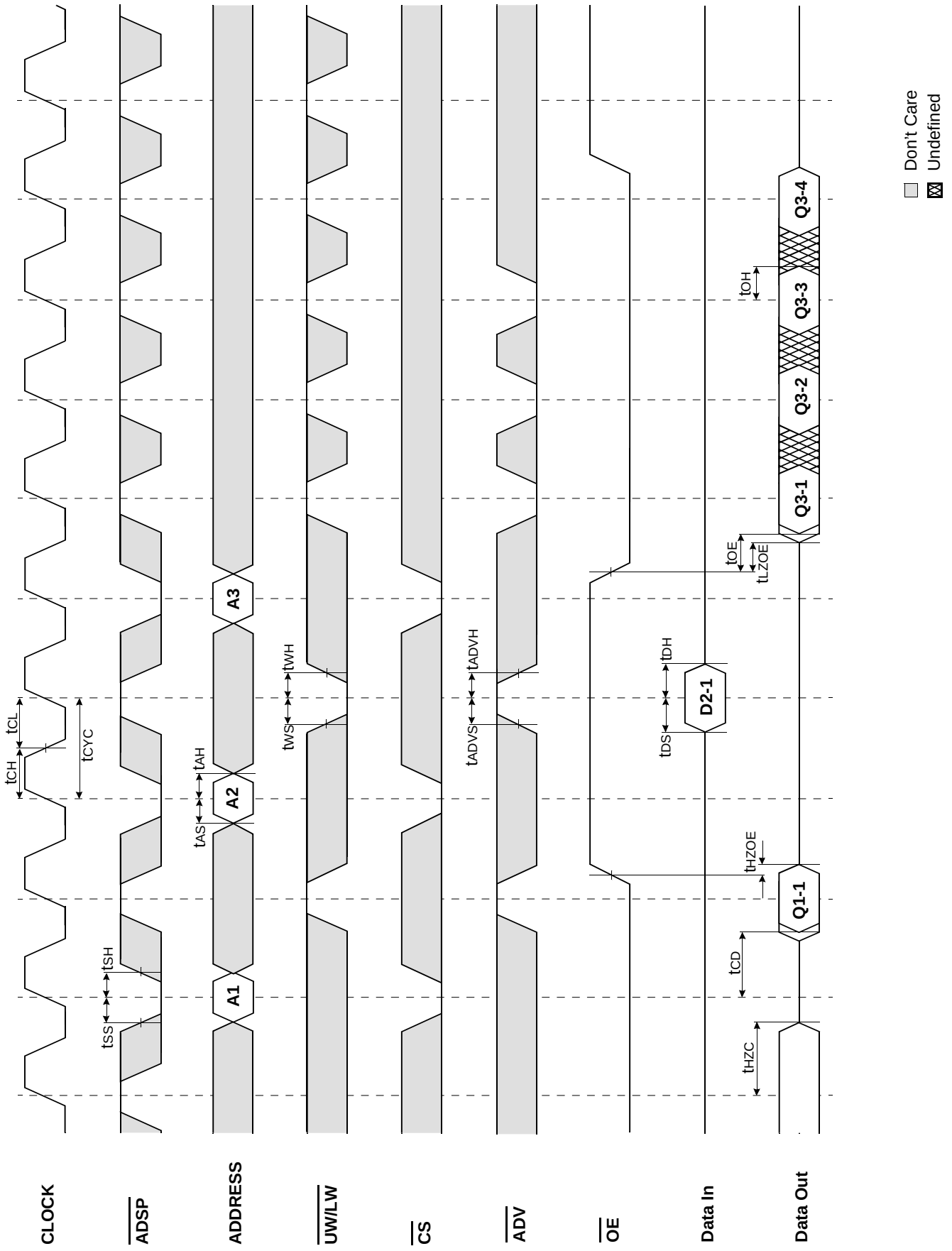
TIMING WAVEFORM OF READ CYCLE



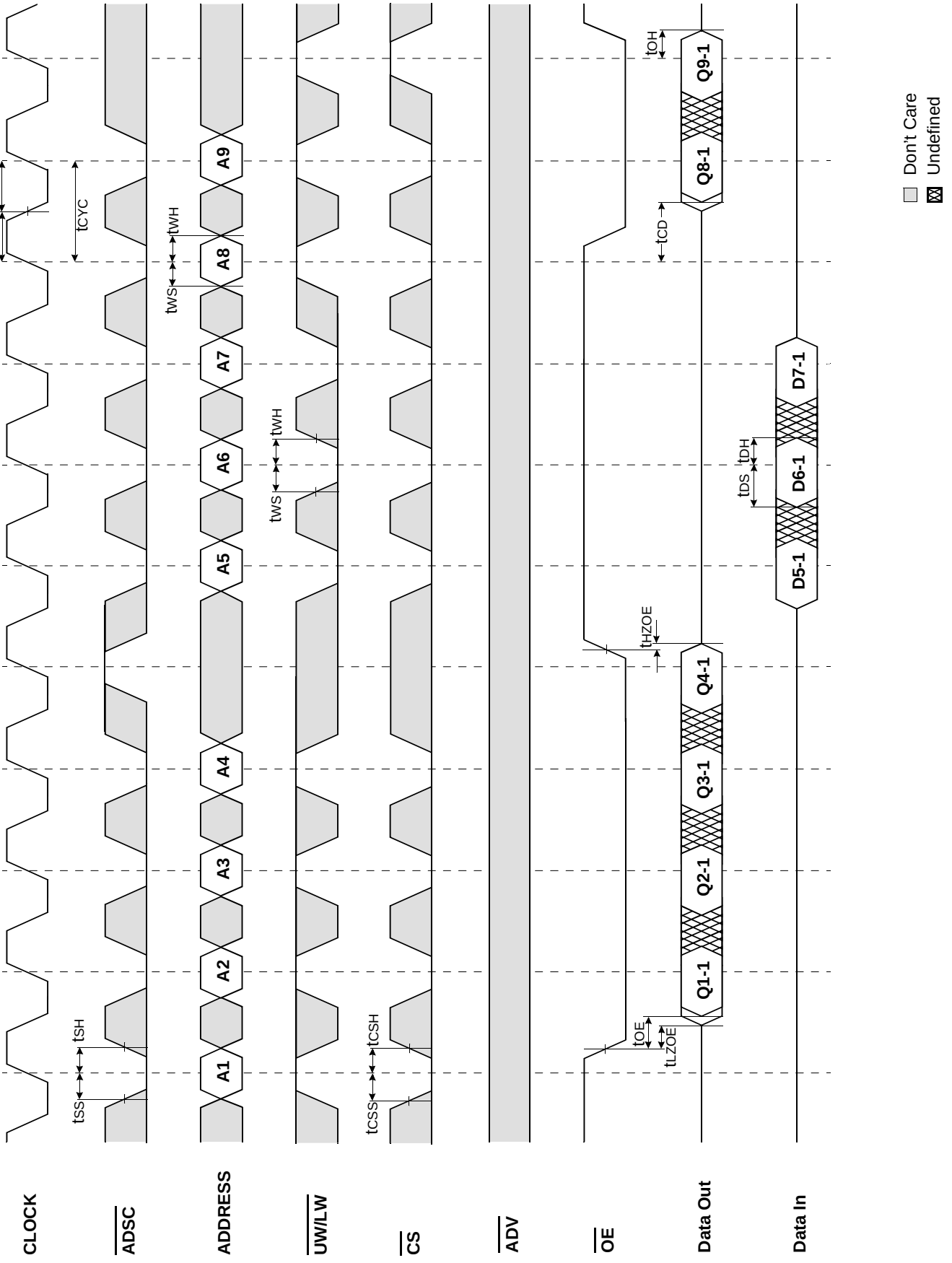
TIMING WAVEFORM OF WRTE CYCLE



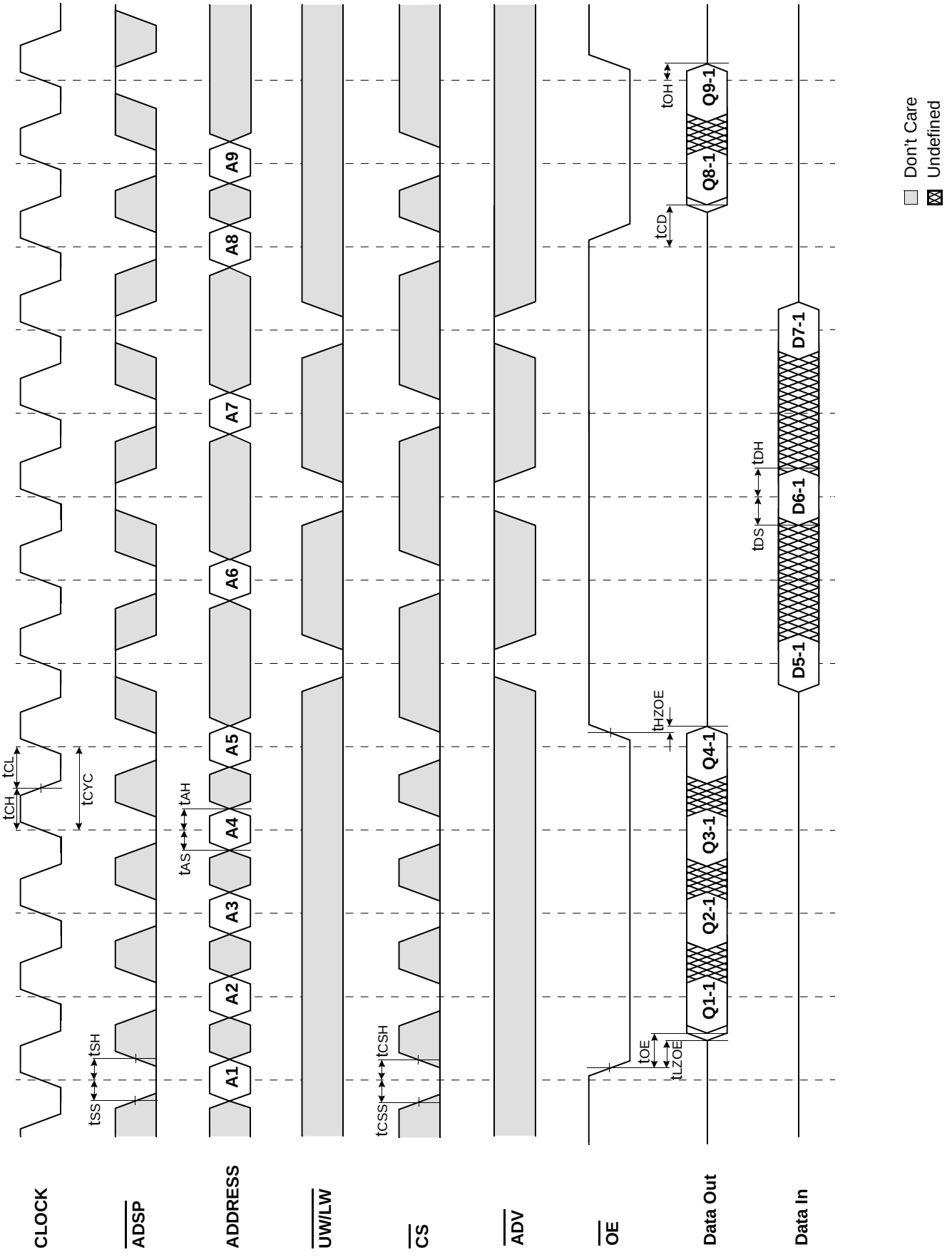
TIMING WAVEFORM OF COMBINATION READ/WRTE CYCLE(ADSP CONTROLLED, ADSC=HIGH)



TIMING WAVEFORM OF SINGLE READ/WRITE CYCLE($\overline{ADSC}$ CONTROLLED, $\overline{ADSP}$=HIGH)



TIMING WAVEFORM OF SINGLE READ/WRITE CYCLE($\overline{ADSP}$ CONTROLLED, $\overline{ADSC}$=HIGH)



TIMING WAVEFORM OF POWER DOWN CYCLE