

Document Title**512K x8 bit Super Low Power and Low Voltage Full CMOS Static RAM****Revision History**

<u>Revision No.</u>	<u>History</u>	<u>Draft Date</u>	<u>Remark</u>
0.0	Initial Draft	July 28, 1999	Preliminary
1.0	Finalize - Adopt new code. - Improve V_{IN} , V_{OUT} max. on 'ABSOLUTE MAXIMUM RATINGS' from 3.6V to $V_{CC}+0.3V$.	March 22, 2000	Final
2.0	Change for AC parameter - Change for tWHZ: 25 to 20ns for 70ns product - Change for tDW: 25 to 30ns for 70ns product	April 24, 2000	Final

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512K x 8 bit Super Low Power and Low Voltage Full CMOS Static RAM

FEATURES

- Process Technology: Full CMOS
- Organization: 512K x8 bit
- Power Supply Voltage: 2.3~2.7V
- Low Data Retention Voltage: 1.5V(Min)
- Three state output status and TTL Compatible
- Package Type: 48-FBGA-6.50x8.50

GENERAL DESCRIPTION

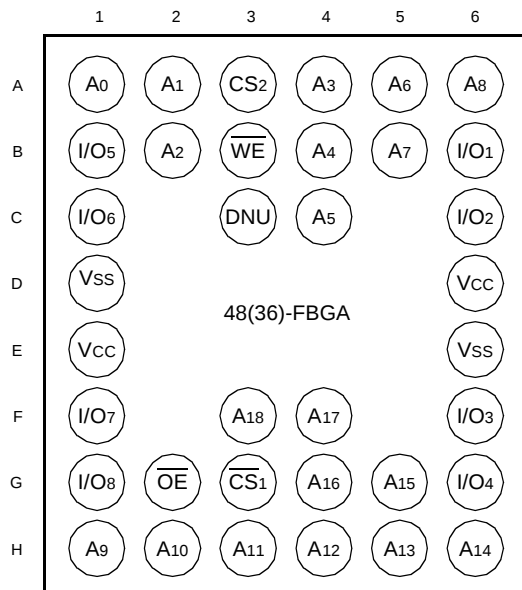
The K6F4008S2C families are fabricated by SAMSUNG's advanced full CMOS process technology. The families support industrial temperature range and Chip Scale Package for user flexibility of system design. The families also supports low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation		PKG Type
				Standby (Isb1, Typ.)	Operating (Icc1, Max)	
K6F4008S2C-F	Industrial(-40~85°C)	2.3~2.7V	70 ¹⁾ /85ns	0.5μA	2mA	48-FBGA-6.50x8.50

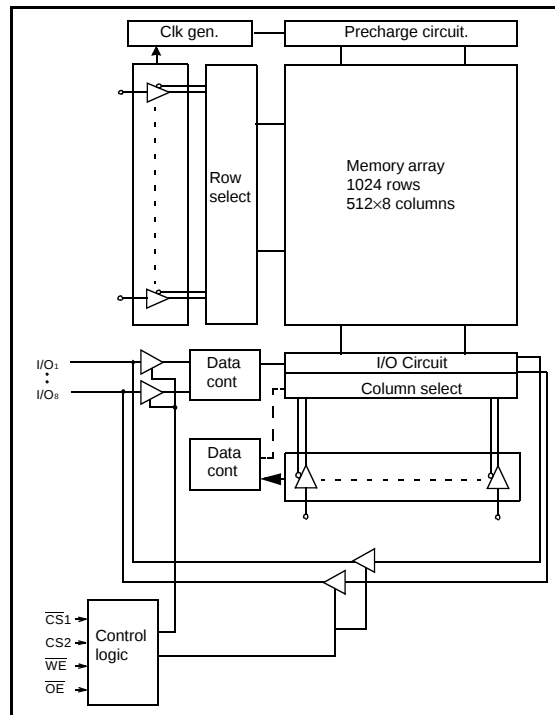
1. The parameter is measured with 30pF test load.

PIN DESCRIPTION



Name	Function	Name	Function
CS1, CS2	Chip Select Inputs	I/O1~I/O8	Data Inputs/Outputs
OE	Output Enable Input	Vcc	Power
WE	Write Enable Input	Vss	Ground
A0~A18	Address Inputs	DNU	Do Not Use

FUNCTIONAL BLOCK DIAGRAM



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PRODUCT LIST

Industrial Temperature Products(-40~85°C)	
Part Name	Function
K6F4008S2C-FF70	48-FBGA, 70ns, 2.5V
K6F4008S2C-FF85	48-FBGA, 85ns, 2.5V

FUNCTIONAL DESCRIPTION

CS ₁	CS ₂	OE	WE	I/O	Mode	Power
H	X ¹⁾	X ¹⁾	X ¹⁾	High-Z	Deselected	Standby
X ¹⁾	L	X ¹⁾	X ¹⁾	High-Z	Deselected	Standby
L	H	H	H	High-Z	Output Disabled	Active
L	H	L	H	Dout	Read	Active
L	H	X ¹⁾	L	Din	Write	Active

1. X means don't care (Must be in low or high state)

ABSOLUTE MAXIMUM RATINGS¹⁾

Item	Symbol	Ratings	Unit
Voltage on any pin relative to V _{ss}	V _{IN} , V _{OUT}	-0.2 to V _{CC} +0.3V	V
Voltage on V _{CC} supply relative to V _{ss}	V _{CC}	-0.2 to 3.6V	V
Power Dissipation	P _D	1.0	W
Storage temperature	T _{STG}	-65 to 150	°C
Operating Temperature	T _A	-40 to 85	°C

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS¹⁾

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V _{CC}	2.3	2.5	2.7	V
Ground	V _{SS}	0	0	0	V
Input high voltage	V _{IH}	2.0	-	V _{CC} +0.2 ²⁾	V
Input low voltage	V _{IL}	-0.2 ³⁾	-	0.6	V

Note:

1. T_A=-40 to 85°C, otherwise specified.
2. Overshoot: V_{CC}+1.0V in case of pulse width ≤20ns.
3. Undershoot: -1.0V in case of pulse width ≤20ns.
4. Overshoot and undershoot are sampled, not 100% tested.

CAPACITANCE¹⁾ (f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C _{IN}	V _{IN} =0V	-	8	pF
Input/Output capacitance	C _{IO}	V _{IO} =0V	-	10	pF

1. Capacitance is sampled, not 100% tested

DC AND OPERATING CHARACTERISTICS

Item	Symbol	Test Conditions	Min	Typ	Max	Unit
Input leakage current	I _{LI}	V _{IN} =V _{SS} to V _{CC}	-1	-	1	μA
Output leakage current	I _{LO}	$\overline{CS}_1=V_{IH}$, CS ₂ =V _{IL} or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$, V _{IO} =V _{SS} to V _{CC}	-1	-	1	μA
Operating power supply	I _{CC}	I _{IO} =0mA, $\overline{CS}_1=V_{IL}$, CS ₂ =V _{IH} , $\overline{WE}=V_{IH}$, V _{IN} =V _{IH} or V _{IL}	-	-	2	mA
Average operating current	I _{CC1}	Cycle time=1μs, 100%duty, I _{IO} =0mA, $\overline{CS}_1 \leq 0.2V$, CS ₂ ≥V _{CC} -0.2V, V _{IN} ≤0.2V or V _{IN} ≥V _{CC} -0.2V	-	-	2	mA
	I _{CC2}	Cycle time=Min, I _{IO} =0mA, 100% duty, $\overline{CS}_1=V_{IL}$, CS ₂ =V _{IH} , V _{IN} =V _{IL} or V _{IH}	-	-	20	mA
Output low voltage	V _{OL}	I _{OL} = 0.5mA	-	-	0.4	V
Output high voltage	V _{OH}	I _{OH} = -0.5mA	2.0	-	-	V
Standby Current(TTL)	I _{SB}	$\overline{CS}_1=V_{IH}$, CS ₂ =V _{IL} , Other inputs=V _{IH} or V _{IL}	-	-	0.3	mA
Standby Current (CMOS)	I _{SB1}	$\overline{CS}_1 \geq V_{CC}-0.2V$, CS ₂ ≥V _{CC} -0.2V($\overline{CS}_1$ controlled) or CS ₂ ≤0.2V(CS ₂ controlled), Other inputs=0-V _{CC}	-	0.5	10 ¹⁾	μA

1. Super low power product=5μA with special handling.

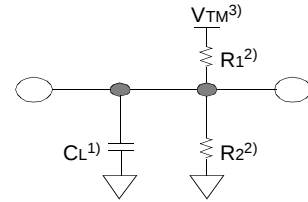
AC OPERATING CONDITIONS

TEST CONDITIONS (Test Load and Test Input/Output Reference)

Input pulse level: 0.4 to 2.2V

Input rising and falling time: 5ns

Input and output reference voltage: 1.1V

Output load (See right): $C_L = 100\text{pF} + 1\text{TTL}$ $C_L = 30\text{pF} + 1\text{TTL}$ 

1. Including scope and jig capacitance

2. $R_1 = 3070\Omega$, $R_2 = 3150\Omega$ 3. $V_{TM} = 2.3\text{V}$ AC CHARACTERISTICS ($V_{CC} = 2.3 \sim 2.7\text{V}$, Industrial product: $T_A = -40$ to 85°C)

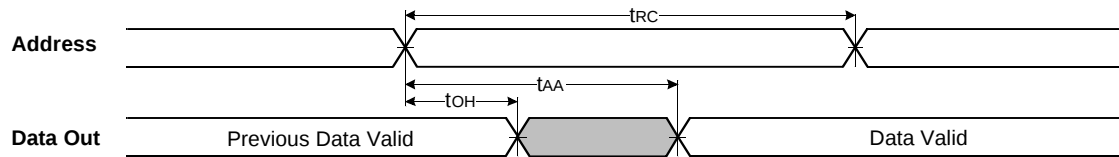
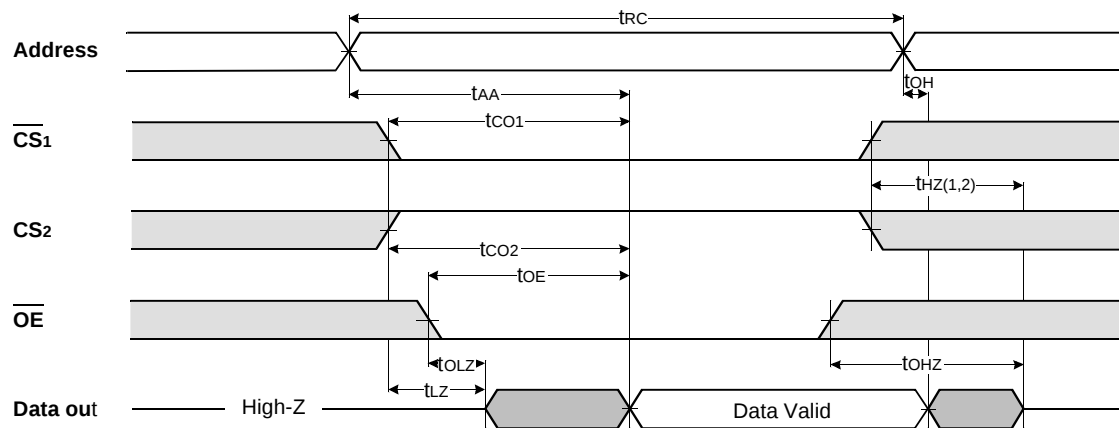
Parameter List		Symbol	Speed Bins				Units
			70ns		85ns		
			Min	Max	Min	Max	
Read	Read Cycle Time	t _{RC}	70	-	85	-	ns
	Address Access Time	t _{AA}	-	70	-	85	ns
	Chip Select to Output	t _{CO}	-	70	-	85	ns
	Output Enable to Valid Output	t _{OE}	-	35	-	40	ns
	Chip Select to Low-Z Output	t _{LZ}	10	-	10	-	ns
	Output Enable to Low-Z Output	t _{OLZ}	5	-	5	-	ns
	Chip Disable to High-Z Output	t _{HZ}	0	25	0	25	ns
	Output Disable to High-Z Output	t _{OHZ}	0	25	0	25	ns
	Output Hold from Address Change	t _{OH}	10	-	10	-	ns
Write	Write Cycle Time	t _{WC}	70	-	85	-	ns
	Chip Select to End of Write	t _{CW}	60	-	70	-	ns
	Address Set-up Time	t _{AS}	0	-	0	-	ns
	Address Valid to End of Write	t _{AW}	60	-	70	-	ns
	Write Pulse Width	t _{WP}	50	-	60	-	ns
	Write Recovery Time	t _{WR}	0	-	0	-	ns
	Write to Output High-Z	t _{WHZ}	0	20	0	25	ns
	Data to Write Time Overlap	t _{DW}	30	-	35	-	ns
	Data Hold from Write Time	t _{DH}	0	-	0	-	ns
	End Write to Output Low-Z	t _{OW}	5	-	5	-	ns

DATA RETENTION CHARACTERISTICS

Item	Symbol	Test Condition	Min	Typ	Max	Unit
V_{CC} for data retention	VDR	$\overline{CS}_1 \geq V_{CC} - 0.2\text{V}^{(1)}$	1.5	-	2.7	V
Data retention current	IDR	$V_{CC} = 1.5\text{V}$, $\overline{CS}_1 \geq V_{CC} - 0.2\text{V}^{(1)}$	-	0.5	3 ⁽²⁾	μA
Data retention set-up time	t _{SDR}	See data retention waveform	0	-	-	ns
Recovery time	t _{RDR}		t _{RC}	-	-	

1. $\overline{CS}_1 \geq V_{CC} - 0.2\text{V}$, $\overline{CS}_2 \geq V_{CC} - 0.2\text{V}$ ($\overline{CS}_1$ controlled) or $\overline{CS}_2 \leq 0.2\text{V}$ ($\overline{CS}_2$ controlled).2. Super low power product = $2\mu\text{A}$ with special handling.

TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{CS_1}=\overline{OE}=V_{IL}$, $CS_2=\overline{WE}=V_{IH}$)TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}=V_{IH}$)

NOTES (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, $t_{HZ}(\text{Max.})$ is less than $t_{LZ}(\text{Min.})$ both for a given device and from device to device interconnection.

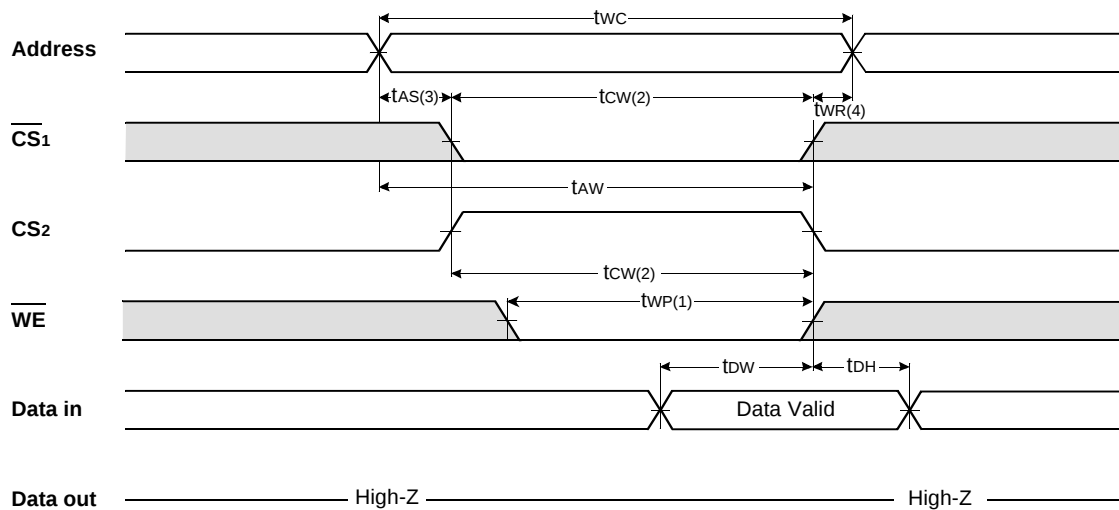
The diagram illustrates the timing relationships for a memory access operation. The signals and their timing parameters are as follows:

- Address:** The address bus signal. The total access time is t_{WC} (Write Cycle time).
- CS₁:** The first chip select signal. It is active for $t_{CW(2)}$ (Write Cycle time for CS₁) and has a setup time $t_{WR(4)}$ before the write data is valid.
- CS₂:** The second chip select signal. It is active for t_{AW} (Access time for CS₂) and has a setup time $t_{CW(2)}$ before the write data is valid.
- WE:** The write enable signal. It is active for $t_{WP(1)}$ (Write Pulse width for WE) and has a setup time $t_{AS(3)}$ before the write data is valid.
- Data in:** The data bus signal for writing. It is valid for t_{DW} (Data Valid time for Data in) and has a hold time t_{DH} after the write operation.
- Data out:** The data bus signal for reading. It is undefined during the write operation and becomes valid after the write operation, with a setup time t_{WHZ} (Write Hold time for Data out) before the next read operation.

The diagram illustrates the timing relationships for a memory access operation. The signals shown are Address, CS1, CS2, WE, Data in, and Data out. The timing parameters are defined as follows:

- tWC**: Address to Data Valid delay.
- tAS(3)**: CS1 setup time before Address Valid.
- tCW(2)**: CS1 hold time after Address Valid.
- tWR(4)**: CS1 setup time before Data Valid.
- tAW**: Address Valid to Data Valid delay.
- tWP(1)**: WE setup time before Data Valid.
- tDW**: Data Valid to Data Invalid delay.
- tDH**: Data Invalid to Data Valid delay.

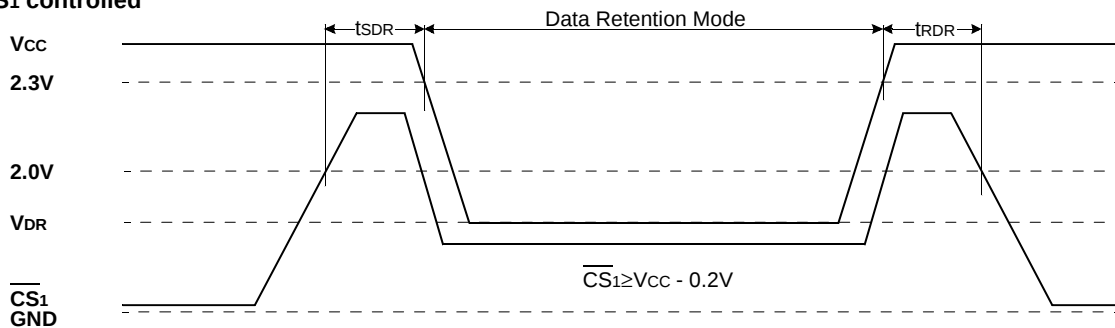
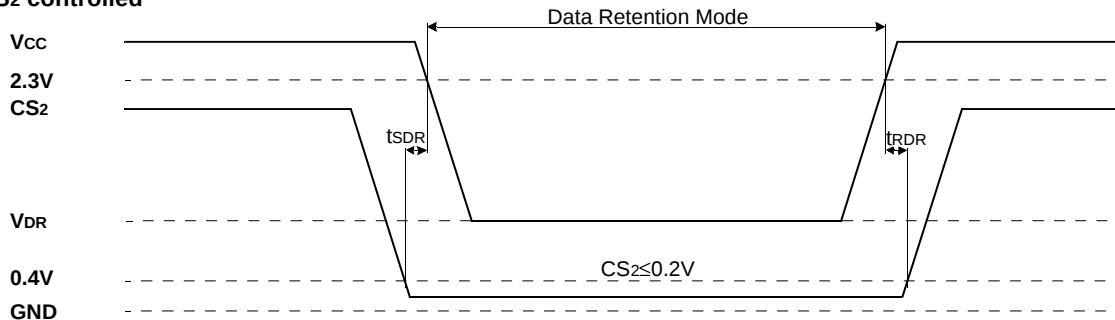
The Data in signal is shown as a pulse labeled "Data Valid". The Data out signal is shown as a pulse labeled "High-Z".

TIMING WAVEFORM OF WRITE CYCLE(3) (CS₂ Controlled)

NOTES (WRITE CYCLE)

1. A write occurs during the overlap of a low $\overline{CS_1}$, a high CS_2 and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS_1}$ goes low, CS_2 going high and $\overline{WE}$ going low: A write end at the earliest transition among CS_1 going high, CS_2 going low and $\overline{WE}$ going high, t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the CS_1 going low or CS_2 going high to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR1} applied in case a write ends as $\overline{CS_1}$ or $\overline{WE}$ going high t_{WR2} applied in case a write ends as CS_2 going to low.

DATA RETENTION WAVE FORM

 $\overline{CS_1}$ controlledCS₂ controlled

PACKAGE DIMENSIONS

Units: millimeters

48 BALL FINE PITCH BGA(0.75mm ball pitch)

