

Document Title**256Kx8 bit Super Low Power and Low Voltage Full CMOS Static RAM****Revision History**

<u>Revision No.</u>	<u>History</u>	<u>Draft Date</u>	<u>Remark</u>
0.0	Initial draft	October 2, 1996	Advance
0.1	Revise - Remove sTSP1 from product - Rename high power product to low power. ISB1=10.0mA(Max) - Add super low power version with special handling ISB1=1.0mA(Max) - Remove 70ns and add 85ns part on KM68FS2000 Family	December 1, 1996	Preliminary
1.0	Finalize	April 11, 1997	Final
2.0	Revise - Change datasheet format - Remove reverse type package from product - Remove reserved speed bin(100ns)	March 5, 1998	Final

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256Kx8 bit Super Low Power and Low Voltage Full CMOS Static RAM

FEATURES

- Process Technology : Full CMOS
- Organization : 256Kx8
- Power Supply Voltage
 - KM68FV2000 Family : 3.0 ~ 3.6V
 - KM68FS2000 Family : 2.3 ~ 3.3V
 - KM68FR2000 Family : 1.8 ~ 2.7V
- Low Data Retention Voltage : 1.5V(Min)
- Three state output and TTL Compatible
- Package Type : 32-TSOP1-0820F

GENERAL DESCRIPTION

The KM68FV2000, KM68FS2000 and KM68FR2000 families are fabricated by SAMSUNG's advanced Full CMOS process technology. The families support various operating temperature ranges and have various package types for user flexibility of system design. The families also supports low data retention voltage for battery back-up operation with low data retention current.

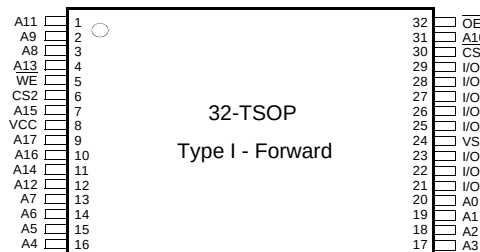
PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed(ns)	Power Dissipation		PKG Type
				Standby (Isb1, Max)	Operating (Icc2, Max)	
KM68FV2000	Commercial(0~70°C)	3.0~3.6V	70 ¹⁾ /85@Vcc=3.3±0.3V	10mA ²⁾	60mA	32-TSOP1-F
KM68FS2000		2.3~3.3V	85@Vcc=3.0±0.3V 120 ¹⁾ /150@Vcc=2.5±0.2V		55mA 30mA	
KM68FR2000		1.8~2.7V	300 ¹⁾ @Vcc=2.0±0.2V		15mA	
KM68FV2000I	Industrial(-40~85°C)	3.0~3.6V	70 ¹⁾ /85@Vcc=3.3±0.3V		60mA	
KM68FS2000I		2.3~3.3V	85@Vcc=3.0±0.3V 120 ¹⁾ /150@Vcc=2.5±0.2V		55mA 30mA	
KM68FR2000I		1.8~2.7V	300 ¹⁾ @Vcc=2.0±0.2V		15mA	

1. The parameter is measured with 30pF test load.

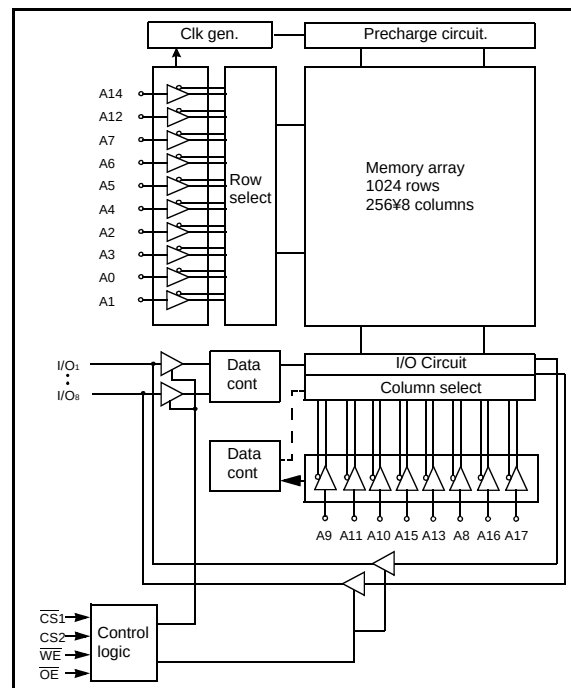
2. 2mA for super low power version with special handling.

PIN DESCRIPTION



Name	Function	Name	Function
CS1, CS2	Chip Select Input	I/O1~I/O8	Data Inputs/Outputs
OE	Output Enable	Vcc	Power
WE	Write Enable Input	Vss	Ground
A0~A17	Address Inputs	N.C.	No Connection

FUNCTIONAL BLOCK DIAGRAM



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PRODUCT LIST

Commercial Temperature Products(0~70°C)		Industrial Temperature Products(-40~85°C)	
Part Name	Function	Part Name	Function
KM68FV2000T-7 KM68FV2000T-8	32-TSOP F, 70ns, 3.3V, LL 32-TSOP F, 85ns, 3.3V, LL	KM68FV2000TI-7 KM68FV2000TI-8	32-TSOP F, 70ns, 3.3V, LL 32-TSOP F, 85ns, 3.3V, LL
KM68FS2000T-12 KM68FS2000T-15	32-TSOP F, 120/85ns, 2.5/3.0V, LL 32-TSOP F, 150/85ns, 2.5/3.0V, LL	KM68FS2000TI-12 KM68FS2000TI-15	32-TSOP F, 120/85ns, 2.5/3.0V, LL 32-TSOP F, 150/85ns, 2.5/3.0V, LL
KM68FR2000T-30	32-TSOP F, 300ns, 2.0/2.5V, LL	KM68FR2000TI-30	32-TSOP F, 300ns, 2.0/2.5V, LL

FUNCTIONAL DESCRIPTION

CS ₁	CS ₂	OE	WE	I/O	Mode	Power
H	X ¹⁾	X ¹⁾	X ¹⁾	High-Z	Deselected	Standby
X ¹⁾	L	X ¹⁾	X ¹⁾	High-Z	Deselected	Standby
L	H	H	H	High-Z	Output Disable	Active
L	H	L	H	Dout	Read	Active
L	H	X ¹⁾	L	Din	Write	Active

1. X means don't care (Must be high or low states)

ABSOLUTE MAXIMUM RATINGS¹⁾

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to V _{SS}	V _{IN} , V _{OUT}	-0.2 to 3.6V ²⁾	V	-
Voltage on V _{CC} supply relative to V _{SS}	V _{CC}	-0.2 to 4.0V ³⁾	V	-
Power Dissipation	P _D	1.0	W	-
Storage temperature	T _{STG}	-55 to 150	°C	-
Operating Temperature	T _A	0 to 70	°C	KM68FV2000, KM68FS2000, KM68FR2000
		-40 to 85	°C	KM68FV2000I, KM68FS2000I, KM68FR2000I
Soldering temperature and time	T _{SOLDER}	260°C, 5sec (Lead Only)	-	-

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2. V_{IN}/V_{OUT}= -0.2 to 3.9V for KM68FV2000 Family.

3. Maximum V_{CC}= -0.2 to 4.6V for KM68FV2000 Family.

RECOMMENDED DC OPERATING CONDITIONS¹⁾

Item	Symbol	Product	Min	Typ ²⁾	Max	Unit
Supply voltage	V _{CC}	KM68FV2000 Family KM68FS2000 Family KM68FR2000 Family	3.0 2.3 1.8	3.3 2.5/3.0 2.0/2.5	3.6 3.3 2.7	V
Ground	V _{SS}	All Family	0	0	0	V
Input high voltage	V _{IH}	KM68FV2000 Family	V _{CC} =3.3±0.3V	2.2	V _{CC} +0.2 ²⁾	V
		KM68FS2000 Family	V _{CC} =3.0±0.3V	2.2		
			V _{CC} =2.5±0.2V	2.0		
		KM68FR2000 Family	V _{CC} =2.5±0.2V	2.0		
			V _{CC} =2.0±0.2V	1.6		
Input low voltage	V _{IL}	All Family	-0.2 ³⁾	-	0.4	V

Note

1. Commercial Product : T_A=0 to 70°C, unless otherwise specifiedIndustrial Product : T_A=-40 to 85°C, unless otherwise specified2. Overshoot : V_{CC} + 1.0V in case of pulse width ≤ 20ns

3. Undershoot : -1.0V in case of pulse width ≤ 20ns

4. Overshoot and undershoot are sampled, not 100% tested.

CAPACITANCE¹⁾ (f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C _{IN}	V _{IN} =0V	-	8	pF
Input/Output capacitance	C _{IO}	V _{IO} =0V	-	10	pF

1. Capacitance is sampled, not 100% tested

DC AND OPERATING CHARACTERISTICS

Item	Symbol	Test Conditions	Min	Typ	Max	Unit
Input leakage current	I _{LI}	V _{IN} =V _{SS} to V _{CC}	-1	-	1	mA
Output leakage current	I _{LO}	$\overline{CS}_1$ =V _{IH} or CS ₂ =V _{IL} or $\overline{OE}$ =V _{IH} or $\overline{WE}$ =V _{IL} , V _{IO} =V _{SS} to V _{CC}	-1	-	1	mA
Operating power supply current	I _{CC}	I _{IO} =0mA, $\overline{CS}_1$ =V _{IL} , CS ₂ =V _{IH} , V _{IN} =V _{IL} or V _{IH} , Read	-	-	10	mA
Average operating current	I _{CC1}	Cycle time=1μs, 100% duty, I _{IO} =0mA, $\overline{CS}_1$ ≤0.2V, CS ₂ ≥V _{CC} -0.2V, V _{IN} ≤0.2V or V _{IN} ≥V _{CC} -0.2V	Read	-	-	10
			Write	-	-	15
	I _{CC2}	Cycle time=Min, 100% duty, I _{IO} =0mA, $\overline{CS}_1$ =V _{IL} , CS ₂ =V _{IH} , V _{IN} =V _{IL} or V _{IH}	V _{CC} =3.3V@70ns	-	-	55 ¹⁾
			V _{CC} =2.7V@120ns	-	-	30
			V _{CC} =2.2V@300ns	-	-	15
Output low voltage	V _{OL}	I _{OL}	2.1mA at V _{CC} =3.0/3.3V	-	-	0.4
			0.5mA at V _{CC} =2.5V	-	-	0.4
			0.33mA at V _{CC} =2.0V	-	-	0.4
Output high voltage	V _{OH}	I _{OH}	-1.0mA at V _{CC} =3.0/3.3V	2.4	-	-
			-0.5mA at V _{CC} =2.5V	2.0	-	-
			-0.44mA at V _{CC} =2.0V	1.6	-	-
Standby Current(TTL)	I _{SB}	$\overline{CS}_1$ =V _{IH} or CS ₂ =V _{IL} , Other inputs=V _{IL} or V _{IH}	-	-	0.3	mA
Standby Current(CMOS)	I _{SB1}	$\overline{CS}_1$ ≥V _{CC} -0.2V, CS ₂ ≥V _{CC} -0.2V or CS ₂ ≤0.2V, Other inputs=0-V _{CC}	-	-	10 ²⁾	mA

1. The value is measured at V_{CC}=3.0±0.3V- I_{CC2}=60mA with 70ns at V_{CC}=3.3±0.3V, but this value is not 100% tested but obtained statistically.

2. Super low power product = 2mA with special handling.

AC OPERATING CONDITIONS

TEST CONDITIONS (Test Load and Test Input/Output Reference)

Input pulse level : 0.4 to 2.2V for Vcc=3.3V, 3.0V, 2.5V

0.4 to 1.8V for Vcc=2.0V

Input rising and falling time : 5ns

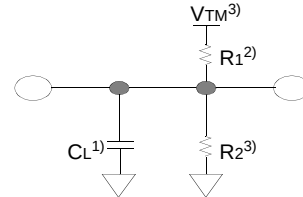
Input and output reference voltage : 1.5V for Vcc=3.3V, 3.0V

1.1V for Vcc=2.5V

0.9V for Vcc=2.0V

Output load (See right) : CL=100pF+1TTL

CL=30pF+1TTL



1. Including scope and jig capacitance

2. R1=3070W, R2=3150W

3. VTM=2.8V for Vcc=3.0/3.3V

=2.3V for Vcc=2.5V

=1.8V for Vcc=2.0V

AC CHARACTERISTICS (Commercial product : TA=0 to 70°C, Industrial product : TA=-40 to 85°C KM68FV2000 Family : Vcc=3.0~3.6V, KM68FS2000 Family : Vcc=2.3~3.3V, KM68FR2000 Family : Vcc=1.8~2.7V)

Parameter List		Symbol	Speed Bins										Units
			70ns		85ns		120ns		150ns		300ns		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Read	Read cycle time	trc	70	-	85	-	120	-	150	-	300	-	ns
	Address access time	tAA	-	70	-	85	-	120	-	150	-	300	ns
	Chip select to output	tCO1, tCO2	-	70	-	85	-	120	-	150	-	300	ns
	Output enable to valid output	tOE	-	35	-	45	-	60	-	75	-	150	ns
	Chip select to low-Z output	tLZ1, tLZ2	10	-	10	-	10	-	20	-	50	-	ns
	Output enable to low-Z output	tOLZ	5	-	5	-	5	-	10	-	30	-	ns
	Chip disable to high-Z output	tHZ1, tHZ2	0	25	0	25	0	35	0	40	0	60	ns
	Output disable to high-Z output	tOHZ	0	25	0	25	0	35	0	40	0	60	ns
	Output hold from address change	tOH	10	-	15	-	15	-	15	-	30	-	ns
Write	Write cycle time	tWC	70	-	85	-	120	-	150	-	300	-	ns
	Chip select to end of write	tCW	65	-	70	-	100	-	120	-	300	-	ns
	Address set-up time	tAS	0	-	0	-	0	-	0	-	0	-	ns
	Address valid to end of write	tAW	65	-	70	-	100	-	120	-	300	-	ns
	Write pulse width	tWP	55	-	60	-	80	-	100	-	200	-	ns
	Write recovery time	tWR	0	-	0	-	0	-	0	-	0	-	ns
	Write to output high-Z	tWHZ	0	25	0	25	0	35	0	40	0	60	ns
	Data to write time overlap	tdW	30	-	35	-	50	-	60	-	120	-	ns
	Data hold from write time	tdH	0	-	0	-	0	-	0	-	0	-	ns
	End write to output low-Z	tOW	5	-	5	-	5	-	5	-	20	-	ns

DATA RETENTION CHARACTERISTICS

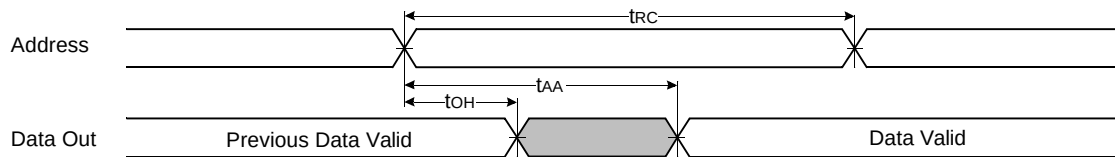
Item	Symbol	Test Condition	Min	Typ	Max	Unit
Vcc for data retention	VDR	$\overline{CS}_1 \geq V_{cc} - 0.2V^{(1)}$	1.5	-	3.6	V
Data retention current	IDR	$V_{cc} = 3.0V, \overline{CS}_1 \geq V_{cc} - 0.2V^{(1)}$	-	-	10 ⁽²⁾	mA
Data retention set-up time	tSDR	See data retention waveform	0	-	-	ns
Recovery time	trDR		trc	-	-	

1. $\overline{CS}_1 \geq V_{cc} - 0.2V$, $\overline{CS}_2 \geq V_{cc} - 0.2V$ ($\overline{CS}_1$ controlled) or $\overline{CS}_2 \leq 0.2V$ ($\overline{CS}_2$ controlled)

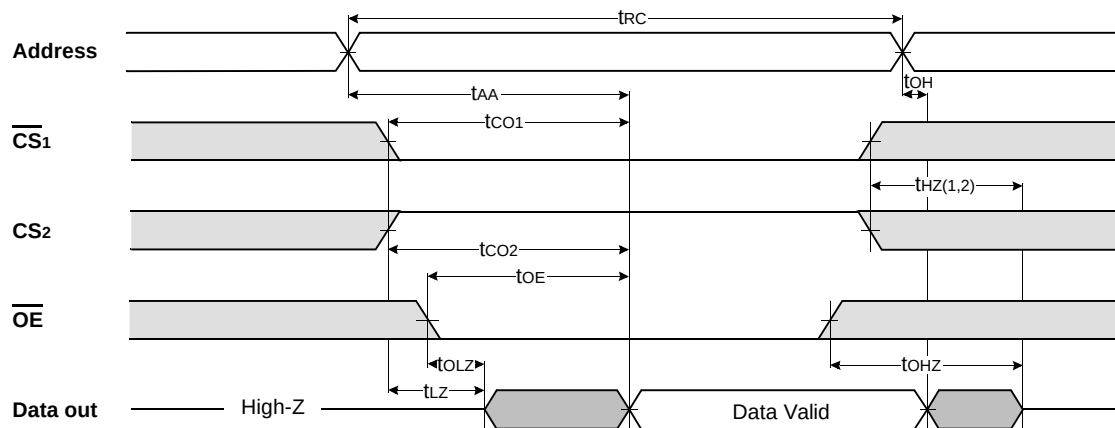
2. Super low power product = 2mA with special handling.

TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{CS1}=\overline{OE}=V_{IL}$, $\overline{WE}=V_{IH}$)



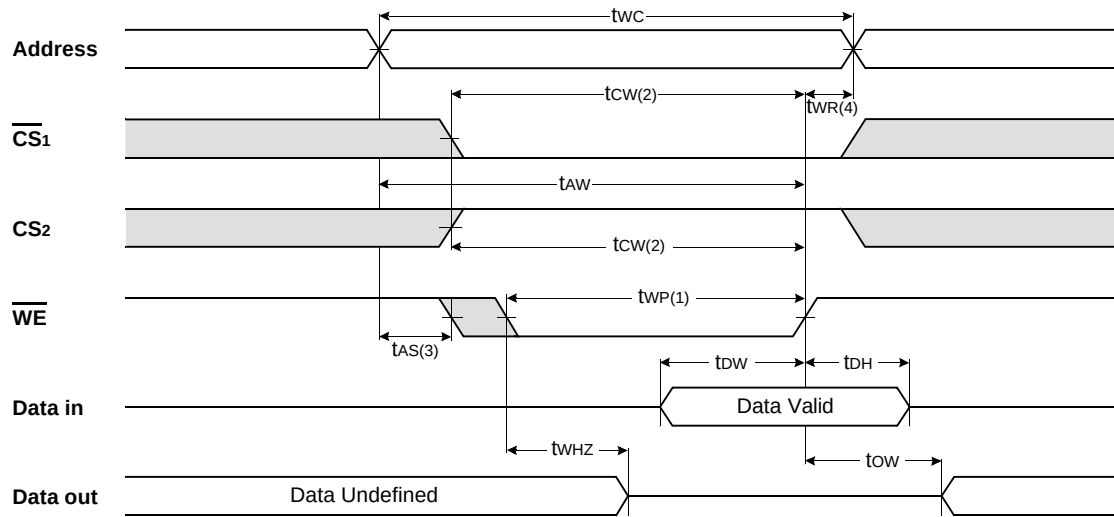
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}=V_{IH}$)



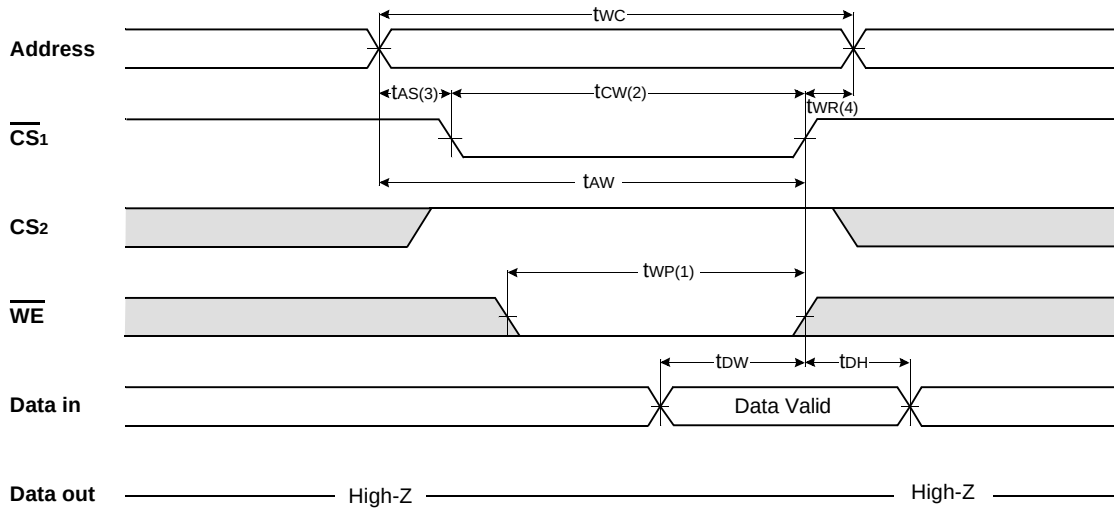
NOTES (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, $t_{HZ}(\text{Max.})$ is less than $t_{LZ}(\text{Min.})$ both for a given device and from device to device interconnection.

TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{CS1}$ Controlled)



The diagram illustrates the timing relationships for the 28C02 EPROM. The signals shown are Address, CS1 (active low), CS2, WE (active low), Data in, and Data out. The timing parameters are defined as follows:

- tWC**: Write Cycle time, from the start of the first address strobe to the start of the last address strobe.
- tAS(3)**: Address Strobe time, from the start of the address strobe to the start of the data valid period.
- tCW(2)**: Chip Write time, from the start of the first address strobe to the start of the data valid period.
- tWR(4)**: Word Strobe time, from the start of the word strobe to the start of the data valid period.
- tAW**: Address Valid time, from the start of the first address strobe to the start of the data valid period.
- tWP(2)**: Word Pulse time, from the start of the word pulse to the start of the data valid period.
- tWP(1)**: Word Pulse time, from the start of the word pulse to the start of the data valid period.
- tdw**: Data Valid time, from the start of the data valid period to the start of the data valid period.
- tdH**: Data Hold time, from the start of the data valid period to the start of the data valid period.

1. A write occurs during the overlap of a low $\overline{CS_1}$, a high CS_2 and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS_1}$ goes low, CS_2 going high and $\overline{WE}$ going low : A write end at the earliest transition among CS_1 going high, CS_2 going low and $\overline{WE}$ going high, t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the CS_1 going low or CS_2 going high to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. $t_{WR(1)}$ applied in case a write ends as $\overline{CS_1}$ or $\overline{WE}$ going high $t_{WR(2)}$ applied in case a write ends as CS_2 going to low.

The diagram illustrates the timing for Data Retention Mode. It shows three signals: VCC, CS1, and VDR. VCC transitions between 3.0V, 2.7V, 2.3V, and 1.8V. CS1 is active-low, transitioning from high to low and back to high. VDR is a square wave that transitions between VCC and a lower level. The time interval tSDR is marked between the first VCC transition and the first CS1 transition. The time interval tRDR is marked between the last CS1 transition and the last VCC transition. The condition $\overline{CS1} \geq V_{CC} - 0.2V$ is indicated during the Data Retention Mode period.

The diagram illustrates the Data Retention Mode timing. It shows three signals: VCC, CS2, and VDR. VCC transitions from 3.0V/2.7V/2.3V/1.8V to 0.4V and back. CS2 transitions from high to low and back. VDR is shown at 0.4V during the retention period. Key timing parameters are tSDR (Setup time before VCC drops) and tRDR (Hold time after VCC rises). The retention voltage is specified as CS2 ≤ 0.2V.

Units : millimeter(inch)

Technical drawing of a rectangular component, likely a PCB or a similar electronic component, showing dimensions and tolerances.

Top View Dimensions:

- Overall width: 20.00 ± 0.20 (mm), 0.787 ± 0.008 (inches)
- Overall height: 8.40 ± 0.331 (mm), 0.331 (inches)
- Pin #1 to Pin #16 distance: 0.20 ± 0.10 (mm), 0.008 ± 0.004 (inches)
- Pin #16 to Pin #17 distance: 0.50 ± 0.0197 (mm)
- Pin #17 to Pin #32 distance: 0.05 ± 0.002 (mm), 0.002 (inches)
- Pin #32 to Pin #1 distance: 0.25 ± 0.010 (mm)

Side View Dimensions:

- Overall thickness: 0.25 ± 0.010 (mm), 0.010 (inches)
- Pin #1 to Pin #16 distance: $0.45 \sim 0.75$ (mm), $0.018 \sim 0.030$ (inches)
- Pin #16 to Pin #17 distance: 0.15 ± 0.10 (mm), 0.006 ± 0.004 (inches)
- Pin #17 to Pin #32 distance: 0.004 ± 0.004 (mm), 0.004 (inches)
- Pin #32 to Pin #1 distance: 0.004 ± 0.004 (mm), 0.004 (inches)

Other Dimensions:

- Pin #1 to Pin #16 distance: 0.50 ± 0.0197 (mm)
- Pin #17 to Pin #32 distance: 0.05 ± 0.002 (mm), 0.002 (inches)
- Pin #32 to Pin #1 distance: 0.25 ± 0.010 (mm)