

Document Title

256Kx 4 High Speed Static RAM(5V Operating), Evolutionary Pin Out.
Operated at Commercial Temperature Range.

Revision History

<u>Rev. No.</u>	<u>History</u>	<u>Draft Data</u>	<u>Remark</u>															
Rev. 0.0	Initial release with Design Target.	Jan. 18th, 1995	Design Target															
Rev. 1.0	Release to Preliminary Data Sheet. 1.1. Replace Design Target to Preliminary	Apr. 22th, 1995	Preliminary															
Rev. 2.0	Release to final Data Sheet. 2.1. Delete Preliminary	Feb. 29th, 1996	Final															
Rev. 3.0	Update D.C and A.C parameters. 3.1. Update D.C parameters	Jul. 16th, 1996	Final															
	<table><tr><td>Items</td><td>Previous spec. (15/17/20ns part)</td><td>Updated spec. (15/17/20ns part)</td></tr><tr><td>Icc</td><td>190/180/170mA</td><td>145/145/140mA</td></tr><tr><td>I_{sb}</td><td>30mA</td><td>25mA</td></tr><tr><td>I_{sb1}</td><td>10mA</td><td>8mA</td></tr></table>	Items	Previous spec. (15/17/20ns part)	Updated spec. (15/17/20ns part)	Icc	190/180/170mA	145/145/140mA	I _{sb}	30mA	25mA	I _{sb1}	10mA	8mA					
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	3.2. Update A.C parameters																	
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Rev. 4.0	Update D.C and A.C parameters 4.1. Update D.C and A.C parameters.	Jun. 2nd, 1997	Final															
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	4.2. Add the test condition for V _{OH1} with V _{CC} =5V±5% at 25°C																	
	4.3. Add timing diagram to define t _{WP} as "(Timing Wave Form of Write Cycle(CS=Controlled))"																	
Rev. 5.0	5.1. Delete 17ns Part	Feb. 25th, 1998	Final															

The attached data sheets are prepared and approved by SAMSUNG Electronics. SAMSUNG Electronics CO., LTD. reserve the right to change the specifications. SAMSUNG Electronics will evaluate and reply to your requests and questions on the parameters of this device. If you have any questions, please contact the SAMSUNG branch office near your office, call or contact Headquarters.

256K x 4 Bit (with OE) High-Speed CMOS Static RAM

FEATURES

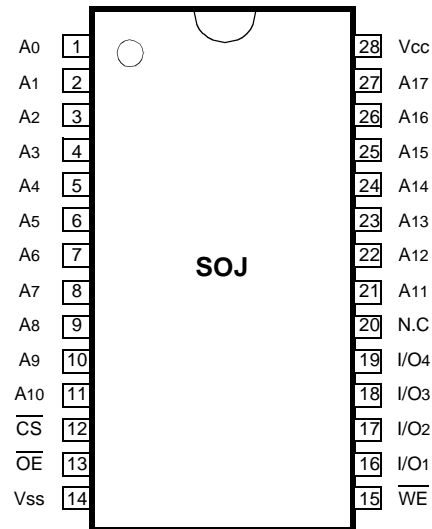
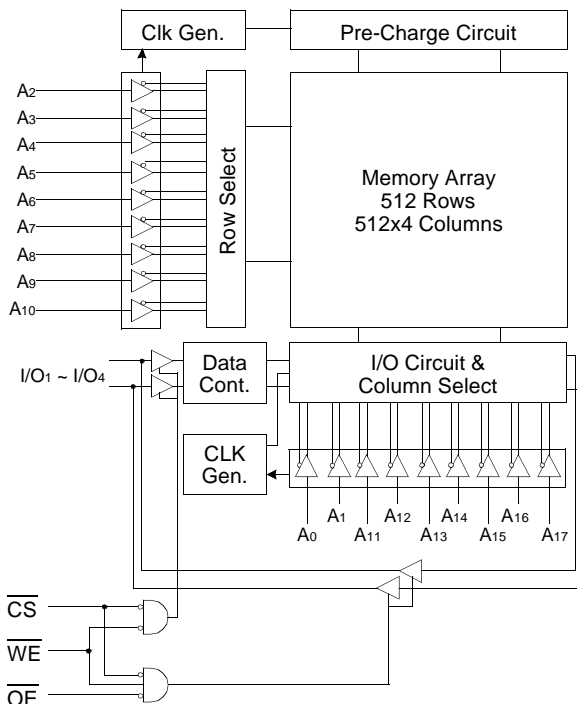
- Fast Access Time 15, 20ns(Max.)
- Low Power Dissipation
 - Standby (TTL) : 25mA(Max.)
 - (CMOS) : 8mA(Max.)
- Operating KM641001A - 15 : 125mA(Max.)
- KM641001A - 20 : 120mA(Max.)
- Single 5.0V±10% Power Supply
- TTL Compatible Inputs and Outputs
- I/O Compatible with 3.3V Device
- Fully Static Operation
 - No Clock or Refresh required
- Three State Outputs
- Standard Pin Configuration
 - KM641001AJ : 28-SOJ-400A

GENERAL DESCRIPTION

The KM641001A is a 1,048,576-bit high-speed Static Random Access Memory organized as 262,144 words by 4 bits. The KM641001A uses 4 common input and output lines and has an output enable pin which operates faster than address access time at read cycle. The device is fabricated using SAMSUNG's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM641001A is packaged in a 400 mil 28-pin plastic SOJ.

PIN CONFIGURATION (Top View)

FUNCTIONAL BLOCK DIAGRAM



PIN FUNCTION

Pin Name	Pin Function
A0 - A17	Address Inputs
WE	Write Enable
CS	Chip Select
OE	Output Enable
I/O1 ~ I/O4	Data Inputs/Outputs
Vcc	Power(+5.0V)
Vss	Ground
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	V _{IN} , V _{OUT}	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss	V _{CC}	-0.5 to 7.0	V
Power Dissipation	P _D	1.0	W
Storage Temperature	T _{STG}	-65 to 150	°C
Operating Temperature	T _A	0 to 70	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS(T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{CC}	4.5	5.0	5.5	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.2	-	V _{CC} + 0.5**	V
Input Low Voltage	V _{IL}	-0.5*	-	0.8	V

* V_{IL}(Min)=-2.0V a.c(Pulse Width ≤ 10ns) for I ≤ 20mA

** V_{IH}(Max)=V_{CC} + 2.0V a.c (Pulse Width ≤ 10ns) for I ≤ 20mA

DC AND OPERATING CHARACTERISTICS(T_A=0 to 70°C, V_{CC}=5.0V±10%, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	I _{LI}	V _{IN} = V _{SS} to V _{CC}		-2	2	μA
Output Leakage Current	I _{LO}	$\overline{CS}=V_{IH}$ or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$ V _{OUT} =V _{SS} to V _{CC}		-2	2	μA
Operating Current	I _{CC}	Min. Cycle, 100% Duty CS=V _{IL} , V _{IN} = V _{IH} or V _{IL} , I _{OUT} =0mA	15ns	-	125	mA
			20ns	-	120	
Standby Current	I _{SB}	Min. Cycle, $\overline{CS}=V_{IH}$		-	25	mA
	I _{SB1}	f=0MHz, $\overline{CS} \geq V_{CC}-0.2V$, V _{IN} ≥V _{CC} -0.2V or V _{IN} ≤ 0.2V		-	8	mA
Output Low Voltage Level	V _{OL}	I _{OL} =8mA		-	0.4	V
Output High Voltage Level	V _{OH}	I _{OH} =-4mA		2.4	-	V
	V _{OH1} *	I _{OH1} =-0.1mA		-	3.95	V

* V_{CC}=5.0V, Temp =25°C

CAPACITANCE*(T_A=25°C, f=1.0MHz)

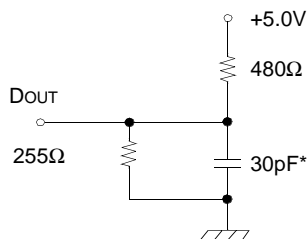
Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	C _{I/O}	V _{I/O} =0V	-	8	pF
Input Capacitance	C _{IN}	V _{IN} =0V	-	6	pF

* NOTE : Capacitance is sampled and not 100% tested.

AC CHARACTERISTICS($T_A=0$ to 70°C , $V_{CC}=5.0\text{V}\pm 10\%$, unless otherwise noted.)**TEST CONDITIONS**

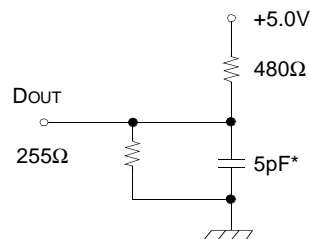
Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

Output Loads(A)



Output Loads(B)

for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ



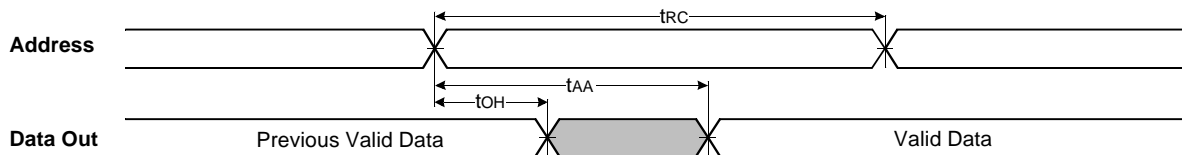
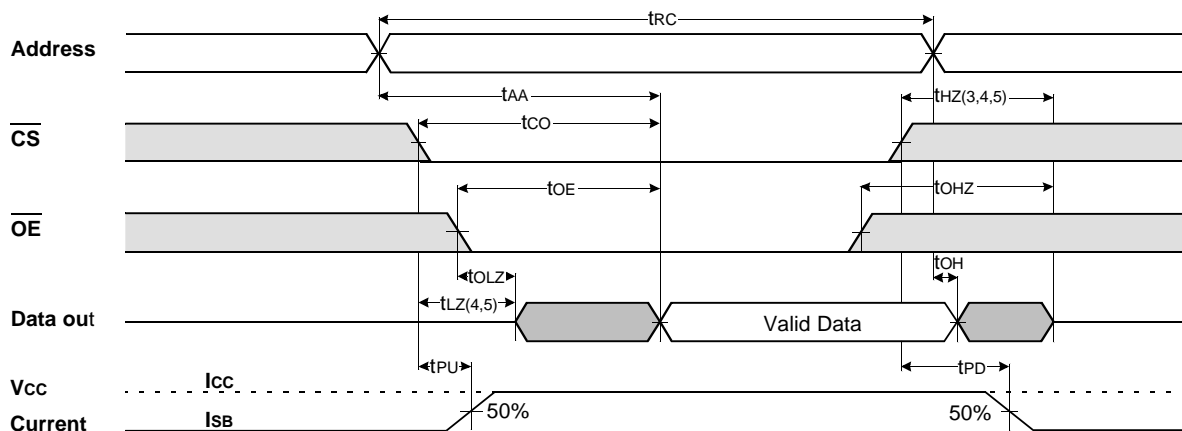
* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM641001A-15		KM641001A-20		Unit
		Min	Max	Min	Max	
Read Cycle Time	tRC	15	-	20	-	ns
Address Access Time	tAA	-	15	-	20	ns
Chip Select to Output	tCO	-	15	-	20	ns
Output Enable to Valid Output	tOE	-	8	-	10	ns
Chip Enable to Low-Z Output	tLZ	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	6	0	8	ns
Output Disable to High-Z Output	tOHZ	0	6	0	8	ns
Output Hold from Address Change	tOH	3	-	3	-	ns
Chip Selection to Power Up Time	tPU	0	-	0	-	ns
Chip Selection to Power Down Time	tPD	-	15	-	20	ns

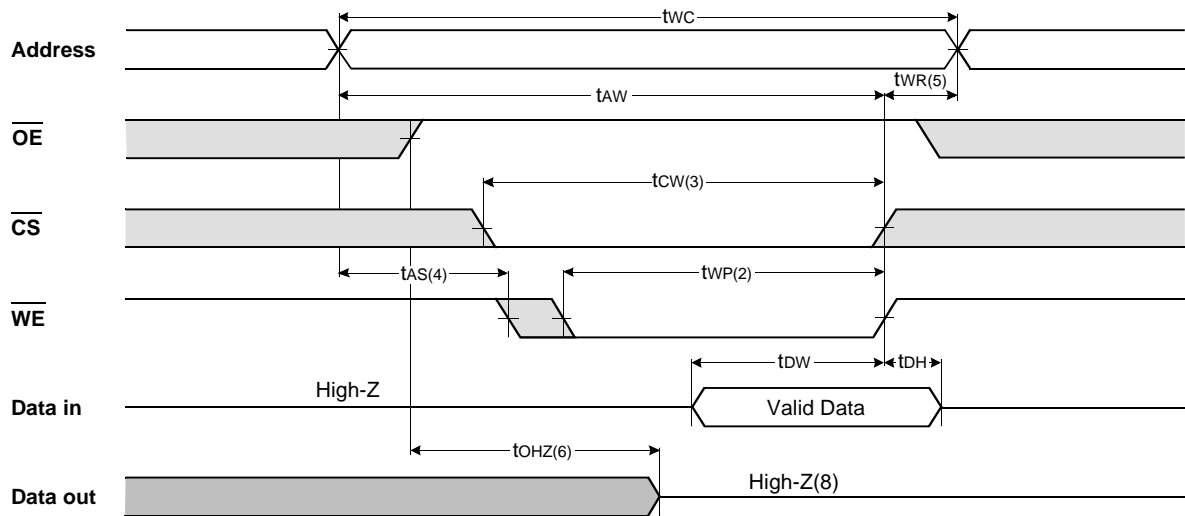
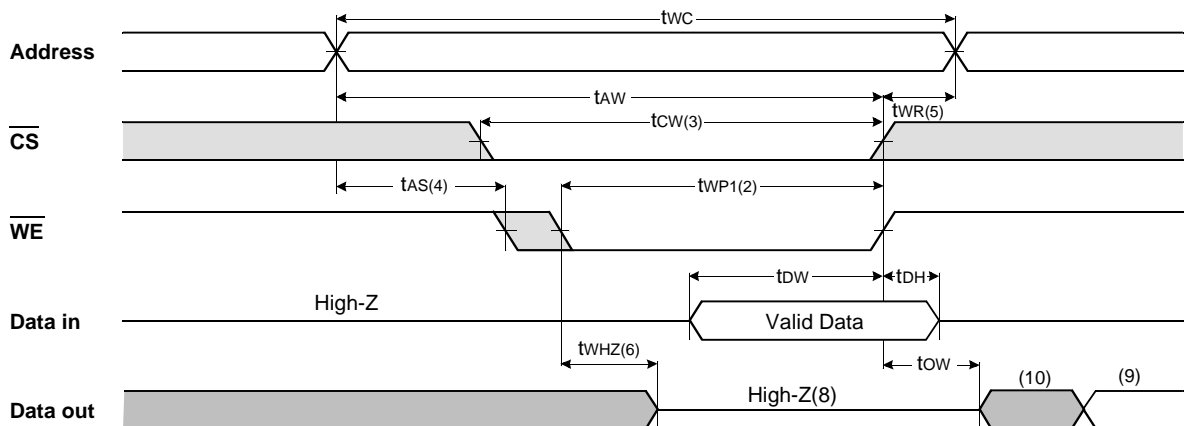
WRITE CYCLE

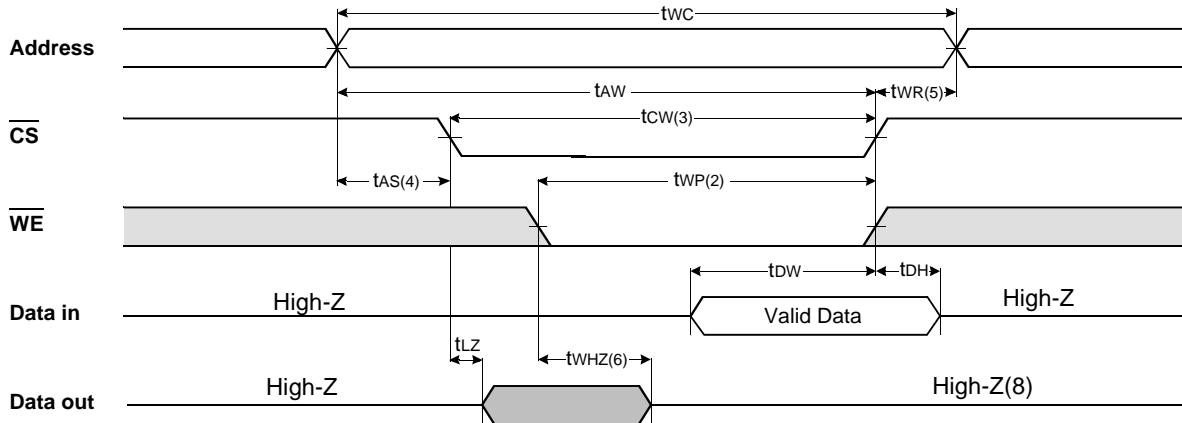
Parameter	Symbol	KM641001A-15		KM641001A-20		Unit
		Min	Max	Min	Max	
Write Cycle Time	tWC	15	-	20	-	ns
Chip Select to End of Write	tCW	10	-	12	-	ns
Address Set-up Time	tAS	0	-	0	-	ns
Address Valid to End of Write	tAW	10	-	12	-	ns
Write Pulse Width($\overline{\text{OE}}$ High)	tWP	10	-	12	-	ns
Write Pulse Width($\overline{\text{OE}}$ Low)	tWP1	15	-	20	-	ns
Write Recovery Time	tWR	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	8	0	10	ns
Data to Write Time Overlap	tDW	7	-	9	-	ns
Data Hold from Write Time	tDH	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	3	-	ns

TIMING DIAGRAMS
TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{\text{CS}}=\overline{\text{OE}}=V_{\text{IL}}$, $\overline{\text{WE}}=V_{\text{IH}}$)

TIMING WAVEFORM OF READ CYCLE(2) ($\overline{\text{WE}}=V_{\text{IH}}$)


NOTES(READ CYCLE)

1. \overline{WE} is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referenced to V_{OH} or V_{OL} levels.
4. At any given temperature and voltage condition, $t_{HZ}(\text{Max.})$ is less than $t_{LZ}(\text{Min.})$ both for a given device and from device to device.
5. Transition is measured $\pm 200\text{mV}$ from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}=V_{IL}$.
7. Address valid prior to coincident with \overline{CS} transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{OE}=\text{Clock}$)**TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{OE}=\text{Low Fixed}$)**

TIMING WAVEFORM OF WRITE CYCLE(3) ($\overline{\text{CS}}$ =Controlled)

NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{\text{CS}}$ and $\overline{\text{WE}}$. A write begins at the latest transition $\overline{\text{CS}}$ going low and $\overline{\text{WE}}$ going low ; A write ends at the earliest transition $\overline{\text{CS}}$ going high or $\overline{\text{WE}}$ going high. t_{WP} is measured from the beginning of write to the end of write.
3. t_{CW} is measured from the later of $\overline{\text{CS}}$ going low to end of write.
4. t_{AS} is measured from the address valid to the beginning of write.
5. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{\text{CS}}$ or $\overline{\text{WE}}$ going high.
6. If $\overline{\text{OE}}$, $\overline{\text{CS}}$ and $\overline{\text{WE}}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{\text{CS}}$ goes low simultaneously with $\overline{\text{WE}}$ going or after $\overline{\text{WE}}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{\text{CS}}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

$\overline{\text{CS}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	Mode	I/O Pin	Supply Current
H	X	X*	Not Select	High-Z	I_{SB} , I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	DOUT	I_{CC}
L	L	X	Write	DIN	I_{CC}

* NOTE : X means Don't Care.

PACKAGE DIMENSIONS

28-SOJ-400A

Units: millimeters/inches

