

## 64M-Bit (8Mx8 /4Mx16) CMOS MASK ROM

## FEATURES

- Switchable organization  
8,388,608 x 8(byte mode)  
4,194,304 x 16(word mode)
- Fast access time :  
100ns(Max.) :  $C_L=50pF$   
120ns(Max.) :  $C_L=100pF$
- Supply voltage : single +5V
- Current consumption  
Operating : 70mA(Max.)  
Standby : 50 $\mu$ A(Max.)
- Fully static operation
- All inputs and outputs TTL compatible
- Three state outputs
- Package  
-. K3N7C1000C-GC : 44-SOP-600

## GENERAL DESCRIPTION

The K3N7C1000C-GC is a fully static mask programmable ROM fabricated using silicon gate CMOS process technology, and is organized either as 8,388,608 x 8 bit(byte mode) or as 4,194,304 x 16 bit(word mode) depending on BHE voltage level.(See mode selection table)

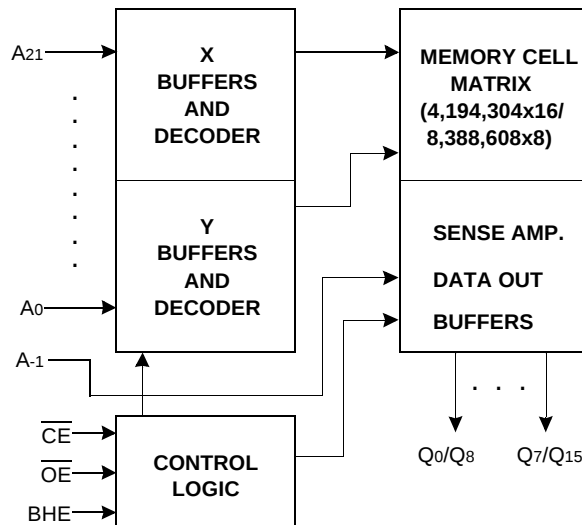
This device operates with a 5V single power supply, and all inputs and outputs are TTL compatible.

Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

It is suitable for use in program memory of microprocessor, and data memory, character generator.

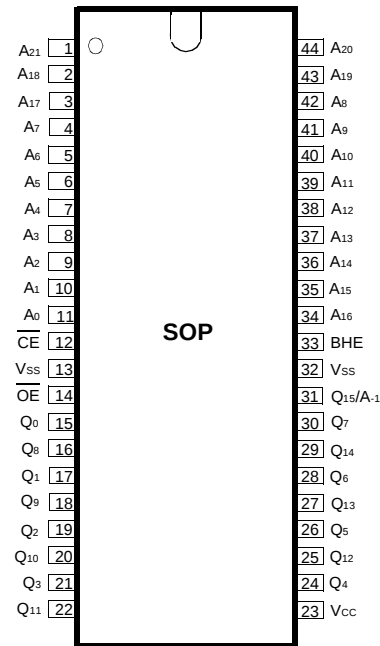
The K3N7C1000C-GC is packaged in a 44-SOP.

## FUNCTIONAL BLOCK DIAGRAM



| Pin Name        | Pin Function                                    |
|-----------------|-------------------------------------------------|
| A0 - A21        | Address Inputs                                  |
| Q0 - Q14        | Data Outputs                                    |
| Q15 /A-1        | Output 15(Word mode)/<br>LSB Address(Byte mode) |
| BHE             | Word/Byte selection                             |
| $\overline{CE}$ | Chip Enable                                     |
| $\overline{OE}$ | Output Enable                                   |
| Vcc             | Power ( +5V)                                    |
| Vss             | Ground                                          |

## PIN CONFIGURATION



K3N7C1000C-GC

## ABSOLUTE MAXIMUM RATINGS

| Item                               | Symbol            | Rating       | Unit |
|------------------------------------|-------------------|--------------|------|
| Voltage on Any Pin Relative to Vss | V <sub>IN</sub>   | -0.3 to +7.0 | V    |
| Temperature Under Bias             | T <sub>BIAS</sub> | -10 to +85   | °C   |
| Storage Temperature                | T <sub>Stg</sub>  | -55 to +150  | °C   |

**NOTE :** Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS(Voltage reference to Vss, TA=0 to 70°C)

| Item           | Symbol          | Min | Typ | Max | Unit |
|----------------|-----------------|-----|-----|-----|------|
| Supply Voltage | V <sub>CC</sub> | 4.5 | 5.0 | 5.5 | V    |
| Supply Voltage | V <sub>SS</sub> | 0   | 0   | 0   | V    |

## DC CHARACTERISTICS

| Parameter                      | Symbol           | Test Conditions                                                                                           | Min  | Max                  | Unit |
|--------------------------------|------------------|-----------------------------------------------------------------------------------------------------------|------|----------------------|------|
| Operating Current              | I <sub>CC</sub>  | Cycle=5MHz, all outputs open<br>CE=OE=V <sub>IL</sub> , V <sub>IN</sub> =0.6V to 2.4V (AC Test Condition) | -    | 70                   | mA   |
| Standby Current(TTL)           | I <sub>SB1</sub> | CE=V <sub>IH</sub> , all outputs open                                                                     | -    | 1                    | mA   |
| Standby Current(CMOS)          | I <sub>SB2</sub> | CE=V <sub>CC</sub> , all outputs open                                                                     | -    | 50                   | μA   |
| Input Leakage Current          | I <sub>LI</sub>  | V <sub>IN</sub> =0 to V <sub>CC</sub>                                                                     | -    | 10                   | μA   |
| Output Leakage Current         | I <sub>LO</sub>  | V <sub>OUT</sub> =0 to V <sub>CC</sub>                                                                    | -    | 10                   | μA   |
| Input High Voltage, All Inputs | V <sub>IH</sub>  |                                                                                                           | 2.2  | V <sub>CC</sub> +0.3 | V    |
| Input Low Voltage, All Inputs  | V <sub>IL</sub>  |                                                                                                           | -0.3 | 0.8                  | V    |
| Output High Voltage Level      | V <sub>OH</sub>  | I <sub>OH</sub> =-400μA                                                                                   | 2.4  | -                    | V    |
| Output Low Voltage Level       | V <sub>OL</sub>  | I <sub>OL</sub> =2.1mA                                                                                    | -    | 0.4                  | V    |

**NOTE :** Minimum DC Voltage(V<sub>IL</sub>) is -0.3V an input pins. During transitions, this level may undershoot to -2.0V for periods <20ns.  
Maximum DC voltage on input pins(V<sub>IH</sub>) is V<sub>CC</sub>+0.3V which, during transitions, may overshoot to V<sub>CC</sub>+2.0V for periods <20ns.

## MODE SELECTION

| CE | OE | BHE | Q15/A-1 | Mode      | Data                                                                            | Power   |
|----|----|-----|---------|-----------|---------------------------------------------------------------------------------|---------|
| H  | X  | X   | X       | Standby   | High-Z                                                                          | Standby |
| L  | H  | X   | X       | Operating | High-Z                                                                          | Active  |
| L  | L  | H   | Output  | Operating | Q <sub>0</sub> ~Q <sub>15</sub> : Dout                                          | Active  |
|    |    | L   | Input   | Operating | Q <sub>0</sub> ~Q <sub>7</sub> : Dout<br>Q <sub>8</sub> ~Q <sub>14</sub> : Hi-Z | Active  |

## CAPACITANCE(TA=25°C, f=1.0MHz)

| Item               | Symbol           | Test Conditions      | Min | Max | Unit |
|--------------------|------------------|----------------------|-----|-----|------|
| Output Capacitance | C <sub>OUT</sub> | V <sub>OUT</sub> =0V | -   | 12  | pF   |
| Input Capacitance  | C <sub>IN</sub>  | V <sub>IN</sub> =0V  | -   | 12  | pF   |

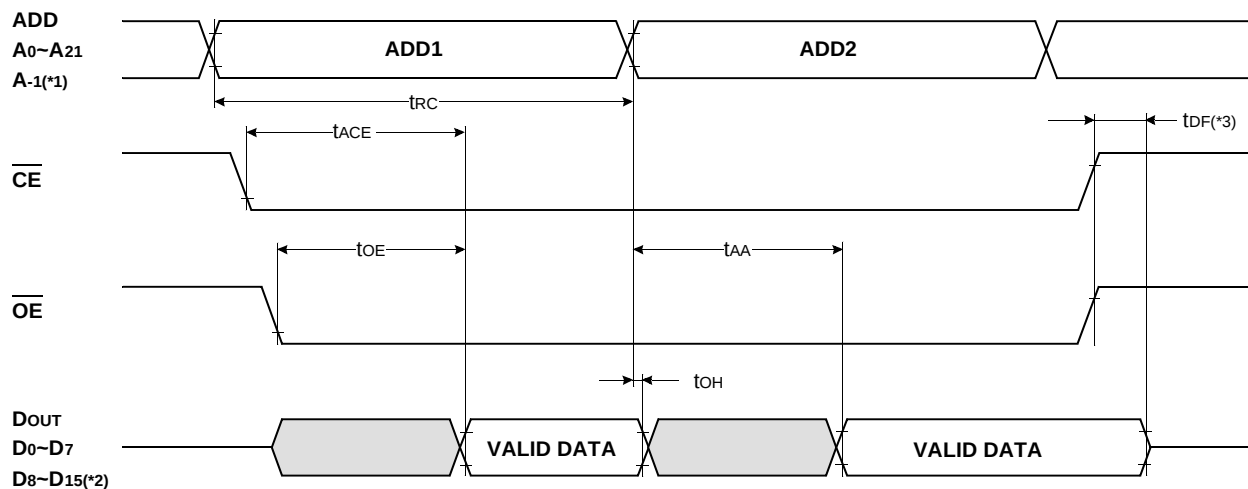
**NOTE :** Capacitance is periodically sampled and not 100% tested.

**AC CHARACTERISTICS**( $T_A=0^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$ ,  $V_{CC}=5\text{V}\pm 10\%$ , unless otherwise noted.)**TEST CONDITIONS**

| Item                           | Value                                              |
|--------------------------------|----------------------------------------------------|
| Input Pulse Levels             | 0.6V to 2.4V                                       |
| Input Rise and Fall Times      | 10ns                                               |
| Input and Output timing Levels | 0.8V and 2.0V                                      |
| Output Loads                   | 1 TTL Gate and $C_L=50\text{pF}$ or $100\text{pF}$ |

**READ CYCLE**

| Item                                    | Symbol    | K3N7C1000C-GC10<br>( $C_L=50\text{pF}$ ) |     | K3N7C1000C-GC12<br>( $C_L=100\text{pF}$ ) |     | K3N7C1000C-GC15<br>( $C_L=100\text{pF}$ ) |     | Unit |
|-----------------------------------------|-----------|------------------------------------------|-----|-------------------------------------------|-----|-------------------------------------------|-----|------|
|                                         |           | Min                                      | Max | Min                                       | Max | Min                                       | Max |      |
| Read Cycle Time                         | $t_{RC}$  | 100                                      |     | 120                                       |     | 150                                       |     | ns   |
| Chip Enable Access Time                 | $t_{ACE}$ |                                          | 100 |                                           | 120 |                                           | 150 | ns   |
| Address Access Time                     | $t_{AA}$  |                                          | 100 |                                           | 120 |                                           | 150 | ns   |
| Output Enable Access Time               | $t_{OE}$  |                                          | 50  |                                           | 60  |                                           | 70  | ns   |
| Output or Chip Disable to Output High-Z | $t_{DF}$  |                                          | 20  |                                           | 20  |                                           | 30  | ns   |
| Output Hold from Address Change         | $t_{OH}$  | 0                                        |     | 0                                         |     | 0                                         |     | ns   |

**TIMING DIAGRAM****READ****NOTES :**\*1. Byte Mode only. A-1 is Least Significant Bit Address. ( $BHE = V_{IL}$ )\*2. Word Mode only. ( $BHE = V_{IH}$ )\*3.  $t_{DF}$  is defined as the time at which the outputs achieve the open circuit condition and is not referenced to  $V_{OH}$  or  $V_{OL}$  level.