

2Mx64 SODIMM

(2MX8 Base)

Revision 2.0

November 1997

DRAM MODULE

Revision History

Version 2.0 (November 1997)

- Changed module PCB from 6-Layer to 4-Layer.

DRAM MODULE

KMM466F203CS2-L & KMM466F213CS2-L EDO Mode

2M x 64 DRAM SODIMM using 2MX8, 2K & 4K Refresh, 3.3V, Low power/Self-Refresh

GENERAL DESCRIPTION

The Samsung KMM466F20(1)3CS2-L is a 2Mx64bits Dynamic RAM high density memory module. The Samsung KMM466F20(1)3CS2-L consists of eight CMOS 2Mx8bits DRAMs in TSOP 400mil packages and a 1K or 2K EEPROM in 8-pin TSSOP package mounted on a 144-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM466F20(1)3CS2-L is a Small Out-line Dual in-line Memory Module and is intended for mounting into 144 pin edge connector sockets.

PERFORMANCE RANGE

Speed	t _{TRAC}	t _{CAC}	t _{RC}	t _{HPC}
-L5	50ns	13ns	90ns	25ns
-L6	60ns	15ns	110ns	30ns

FEATURES

- Part Identification
 - KMM466F203CS2-L(4096 cycles/128ms, TSOP, L-ver)
 - KMM466F213CS2-L(2048 cycles/128ms, TSOP, L-ver)
- Extended Data Out Mode Operation
- New JEDEC standard proposal with EEPROM
- Serial Presense Detect with EEPROM
- $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh capability
- Self -refresh capability
- $\overline{\text{RAS}}$ -only and Hidden refresh capability
- LVTTTL compatible inputs and outputs
- Single +3.3V±0.3V power supply
- PCB : Height(1000mil), Double sided component

PIN CONFIGURATIONS

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	Vss	2	Vss	49	DQ13	50	DQ45	97	DQ22	98	DQ54
3	DQ0	4	DQ32	51	DQ14	52	DQ46	99	DQ23	100	DQ55
5	DQ1	6	DQ33	53	DQ15	54	DQ47	101	Vcc	102	Vcc
7	DQ2	8	DQ34	55	Vss	56	Vss	103	A6	104	A7
9	DQ3	10	DQ35	57	RSVD	58	RSVD	105	A8	106	N.C
11	Vcc	12	Vcc	59	RSVD	60	RSVD	107	Vss	108	Vss
13	DQ4	14	DQ36	61	RFU	62	RFU	109	A9	110	NC
15	DQ5	16	DQ37	63	Vcc	64	Vcc	111	A10	112	A11
17	DQ6	18	DQ38	65	RFU	66	RFU	113	Vcc	114	Vcc
19	DQ7	20	DQ39	67	$\overline{\text{W}}$	68	RFU	115	$\overline{\text{CAS2}}$	116	$\overline{\text{CAS6}}$
21	Vss	22	Vss	69	$\overline{\text{RAS0}}$	70	RFU	117	$\overline{\text{CAS3}}$	118	$\overline{\text{CAS7}}$
23	$\overline{\text{CAS0}}$	24	$\overline{\text{CAS4}}$	71	NC	72	RFU	119	Vss	120	Vss
25	$\overline{\text{CAS1}}$	26	$\overline{\text{CAS5}}$	73	$\overline{\text{OE}}$	74	RFU	121	DQ24	122	DQ56
27	Vcc	28	Vcc	75	Vss	76	Vss	123	DQ25	124	DQ57
29	A0	30	A3	77	RSVD	78	RSVD	125	DQ26	126	DQ58
31	A1	32	A4	79	RSVD	80	RSVD	127	DQ27	128	DQ59
33	A2	34	A5	81	Vcc	82	Vcc	129	Vcc	130	Vcc
35	Vss	36	Vss	83	DQ16	84	DQ48	131	DQ28	132	DQ60
37	DQ8	38	DQ40	85	DQ17	86	DQ49	133	DQ29	134	DQ61
39	DQ9	40	DQ41	87	DQ18	88	DQ50	135	DQ30	136	DQ62
41	DQ10	42	DQ42	89	DQ19	90	DQ51	137	DQ31	138	DQ63
43	DQ11	44	DQ43	91	Vss	92	Vss	139	Vss	140	Vss
45	Vcc	46	Vcc	93	DQ20	94	DQ52	141	**SDA	142	**SCL
47	DQ12	48	DQ44	95	DQ21	96	DQ53	143	Vcc	144	Vcc

PIN NAMES

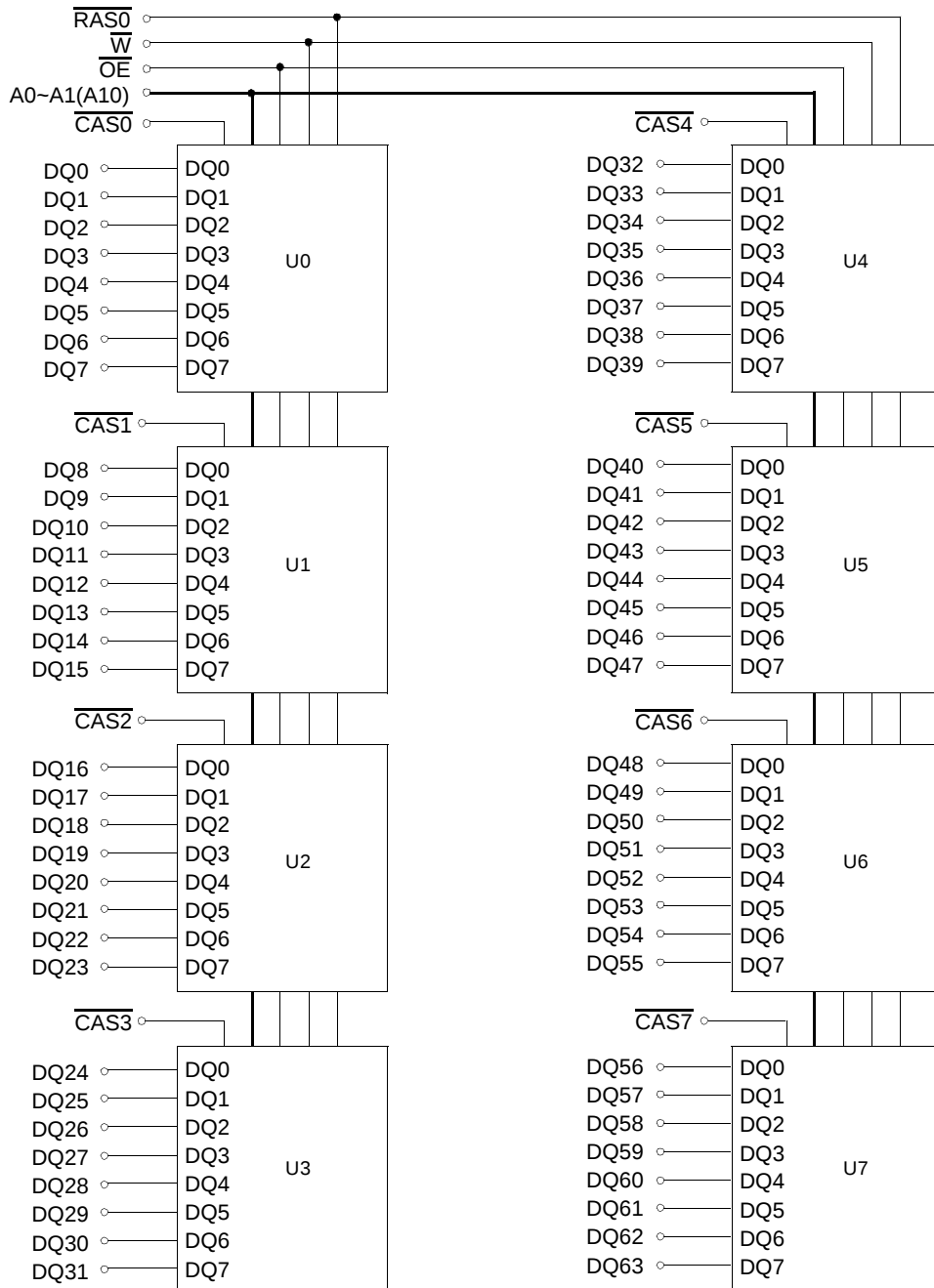
Pin Name	Function
A0 to 11	Address Inputs (4K ref.)
A0 to 10	Address Inputs (2K ref.)
DQ0 - DQ63	Data In/Out
$\overline{\text{W}}$	Read/Write Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{RAS0}}$	Row Address Strobe
$\overline{\text{CAS0}}$ - $\overline{\text{CAS7}}$	Column Address Strobe
Vcc	Power(+3.3V)
Vss	Ground
NC	No Connection
**SDA	Serial Address / Data I/O
**SCL	Serial Clock
RSVD	Reserved Use
RFU	Reserved for Future Use

- * These pins are not used in this module.
 ** These pins should be NC in the system which does not support SPD.

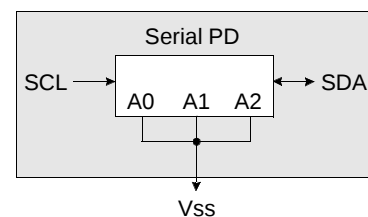
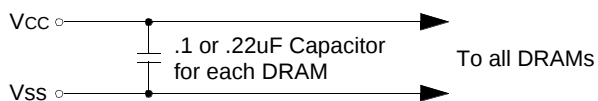
Note : A11 is used for only KMM466F203CS2-L (4K ref.)

DRAM MODULE

FUNCTIONAL BLOCK DIAGRAM



*A11 is used for only KMM466F203CS2-L (4K ref.)



DRAM MODULE

ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative V _{ss}	V _{IN} , V _{OUT}	-0.5 to +4.6	V
Voltage on V _{cc} supply relative to V _{ss}	V _{CC}	-0.5 to +4.6	V
Storage Temperature	T _{stg}	-55 to +125	°C
Power Dissipation	P _D	8	W
Short Circuit Output Current	I _{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{CC}	3.0	3.3	3.6	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.0	-	V _{CC} +0.3 ^{*1}	V
Input Low Voltage	V _{IL}	-0.3 ^{*2}	-	0.8	V

*1 : V_{CC}+1.3V at pulse width ≤15ns, which is measured at V_{CC}.

*2 : -1.3V at pulse width ≤15ns, which is measured at V_{SS}.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM466F203CS2-L		KMM466F213CS2-L		Unit
		Min	Max	Min	Max	
I _{CC1}	-L5	-	720	-	880	mA
	-L6	-	640	-	800	
I _{CC2}	Don't care	-	8	-	8	mA
I _{CC3}	-L5	-	720	-	880	mA
	-L6	-	640	-	800	
I _{CC4}	-L5	-	640	-	720	mA
	-L6	-	560	-	640	
I _{CC5}	Don't care	-	1.6	-	1.6	mA
I _{CC6}	-L5	-	720	-	880	mA
	-L6	-	640	-	800	
I _{CC7}	-	-	2.0	-	2.0	mA
I _{CCS}	-	-	1.6	-	1.6	mA
I _{I(L)} I _{O(L)}	Don't care	-40	40	-40	40	uA
		-5	5	-5	5	
V _{OH} V _{OL}	Don't care	2.4	-	2.4	-	V
		-	0.4	-	0.4	

I_{CC1} : Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC}=min)

I_{CC2} : Standby Current ($\overline{RAS}=\overline{CAS}=\overline{W}=V_{IH}$)

I_{CC3} : $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}=V_{IH}$, $\overline{RAS}$ cycling @t_{RC}=min)

I_{CC4} : Extended Data Out Mode Current * ($\overline{RAS}=V_{IL}$, $\overline{CAS}$ cycling : t_{HPC}=min)

I_{CC5} : Standby Current ($\overline{RAS}=\overline{CAS}=\overline{W}=V_{CC}-0.2V$)

I_{CC6} : $\overline{CAS}$ -Before- $\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min)

I_{CC7} : Battery back-up current. Average power supply, Battery back-up mode.

Input high voltage(V_{IH})=V_{CC}-0.2V, Input low voltage(V_{IL})=0.2V, $\overline{UCAS}$, $\overline{LCAS}$ =0.2V,

Din=Don't care, t_{RC}=31.25us(4K/L-ver), 62.5us(2K/L-ver), t_{RAS}=t_{RASmin}~300ns)

I_{CCS} : Self Refresh Current ($\overline{RAS}=\overline{UCAS}=\overline{LCAS}=V_{IL}$, $\overline{W}=\overline{OE}=A0-A1=V_{CC}-0.2V$ or 0.2V, DQ~DQ63=V_{CC}-0.2V or Open)

I_{I(L)} : Input Leakage Current (Any input 0 ≤ V_{IN} ≤ V_{CC}+0.3V, all other pins not under test=0 V)

I_{O(L)} : Output Leakage Current(Data Out is disabled, 0V ≤ V_{OUT} ≤ V_{CC})

V_{OH} : Output High Voltage Level (I_{OH} = -2mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 2mA)

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}=V_{IL}$. In I_{CC4}, address can be changed maximum once within one page mode cycle, t_{HPC}.

DRAM MODULE

CAPACITANCE (TA = 25°C, VCC=3.3V, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0-A10]	CIN1	-	50	pF
Input capacitance[W, OE]	CIN2	-	66	pF
Input capacitance[RAS0]	CIN3	-	66	pF
Input capacitance[CAS0 - CAS7]	CIN4	-	17	pF
Input/Output capacitance[DQ0 - 63]	CDQ	-	17	pF

AC CHARACTERISTICS (0°C≤TA≤70°C, See notes 1,2.)

Test condition : VCC=3.3V±0.3V, VIH/UIL=2.0/0.8V, VOH/VOL=2.0/0.8V, Output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	tRC	90		110		ns	
Read-modify-write cycle time	tRWC	131		155		ns	
Access time from $\overline{\text{RAS}}$	tRAC		50		60	ns	
Access time from $\overline{\text{CAS}}$	tCAC		13		15	ns	3,4,5
Access time from column address	tAA		25		30	ns	3,9
$\overline{\text{CAS}}$ to output in Low-Z	tCLZ	3		3		ns	3
$\overline{\text{OE}}$ to output in Low-Z	tOLZ	3		3		ns	3
Output buffer turn-off delay from $\overline{\text{CAS}}$	tCEZ	3	13	3	15	ns	3,12
Transition time(rise and fall)	tT	2	50	2	50	ns	2
$\overline{\text{RAS}}$ precharge time	tRP	30		40		ns	
$\overline{\text{RAS}}$ pulse width	tRAS	50	10K	60	10K	ns	
$\overline{\text{RAS}}$ hold time	tRSH	13		15		ns	
$\overline{\text{CAS}}$ hold time	tCSH	38		45		ns	
$\overline{\text{CAS}}$ pulse width	tCAS	8	10K	10	10K	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	tRCD	20	37	20	45	ns	4
$\overline{\text{RAS}}$ to column address delay time	tRAD	15	25	15	30	ns	9
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	tCRP	5		5		ns	
Row address set-up time	tASR	0		0		ns	
Row address hold time	tRAH	10		10		ns	
Column address set-up time	tASC	0		0		ns	13
Column address hold time	tCAH	8		10		ns	13
Column address to $\overline{\text{RAS}}$ lead time	tRAL	25		30		ns	
Read command set-up time	tRCS	0		0		ns	
Read command hold referenced to $\overline{\text{CAS}}$	tRCH	0		0		ns	7
Read command hold referenced to $\overline{\text{RAS}}$	tRRH	0		0		ns	7
Write command set-up time	tWCS	0		0		ns	6
Write command hold time	tWCH	10		10		ns	6
Write command pulse width	tWP	10		10		ns	
Write command to $\overline{\text{RAS}}$ lead time	tRWL	13		15		ns	
Write command to $\overline{\text{CAS}}$ lead time	tCWL	8		10		ns	16
Data set-up time	tDS	0		0		ns	8
Data hold time	tDH	8		10		ns	8
Refresh period	tREF		128		128	ms	
$\overline{\text{CAS}}$ to $\overline{\text{W}}$ dealy time	tCWD	36		40		ns	6,15
$\overline{\text{RAS}}$ to $\overline{\text{W}}$ dealy time	tRWD	73		85		ns	6

DRAM MODULE

AC CHARACTERISTICS (Continued)

Test condition : $V_{CC}=3.3V\pm0.3V$, $V_{IH}/V_{IL}=2.0/0.8V$, $V_{OH}/V_{OL}=2.0/0.8V$, output loading $C_L=100pF$

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Column address to $\overline{W}$ delay time	t_{AWD}	48		55		ns	6
$\overline{CAS}$ precharge to $\overline{W}$ delay time	t_{CPWD}	53		60		ns	6
$\overline{CAS}$ setup time ($\overline{CAS}$ -before- $\overline{RAS}$ refresh)	t_{CSR}	5		5		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$ -before- $\overline{RAS}$ refresh)	t_{CHR}	10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		5		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		28		35	ns	3
Hyper page mode cycle time	t_{HPC}	25		30		ns	10
Hyper page mode read-modify write cycle time	t_{HPRWC}	68		77		ns	10
$\overline{CAS}$ precharge time (Hyper page cycle)	t_{CP}	8		10		ns	14
$\overline{RAS}$ pulse width (Hyper page cycle)	t_{RASP}	50	200K	60	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	30		35		ns	
$\overline{OE}$ access time	t_{OEA}		13		15	ns	3
$\overline{OE}$ to data delay	t_{OED}	13		15		ns	
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	3	13	3	15	ns	
$\overline{OE}$ command hold time	t_{OEH}	13		15		ns	
Output data hold time	t_{DOH}	5		5		ns	
Output buffer turn off delay from $\overline{RAS}$	t_{REZ}	3	13	3	15	ns	12
Output buffer turn off delay from $\overline{W}$	t_{WEZ}	3	13	3	15	ns	
$\overline{W}$ to data delay	t_{WED}	15		15		ns	
$\overline{OE}$ to $\overline{CAS}$ hold time	t_{OCH}	5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	t_{CHO}	5		5		ns	
$\overline{OE}$ precharge time	t_{OEP}	5		5		ns	
$\overline{W}$ pulse width	t_{WPE}	5		5		ns	
$\overline{RAS}$ pulse width (C-B-R self refresh)	t_{RASS}	100		100		ns	11
$\overline{RAS}$ precharge time (C-B-R self refresh)	t_{RPS}	90		110		ns	11
$\overline{CAS}$ hold time (C-B-R self refresh)	t_{CHS}	-50		-50		ns	11

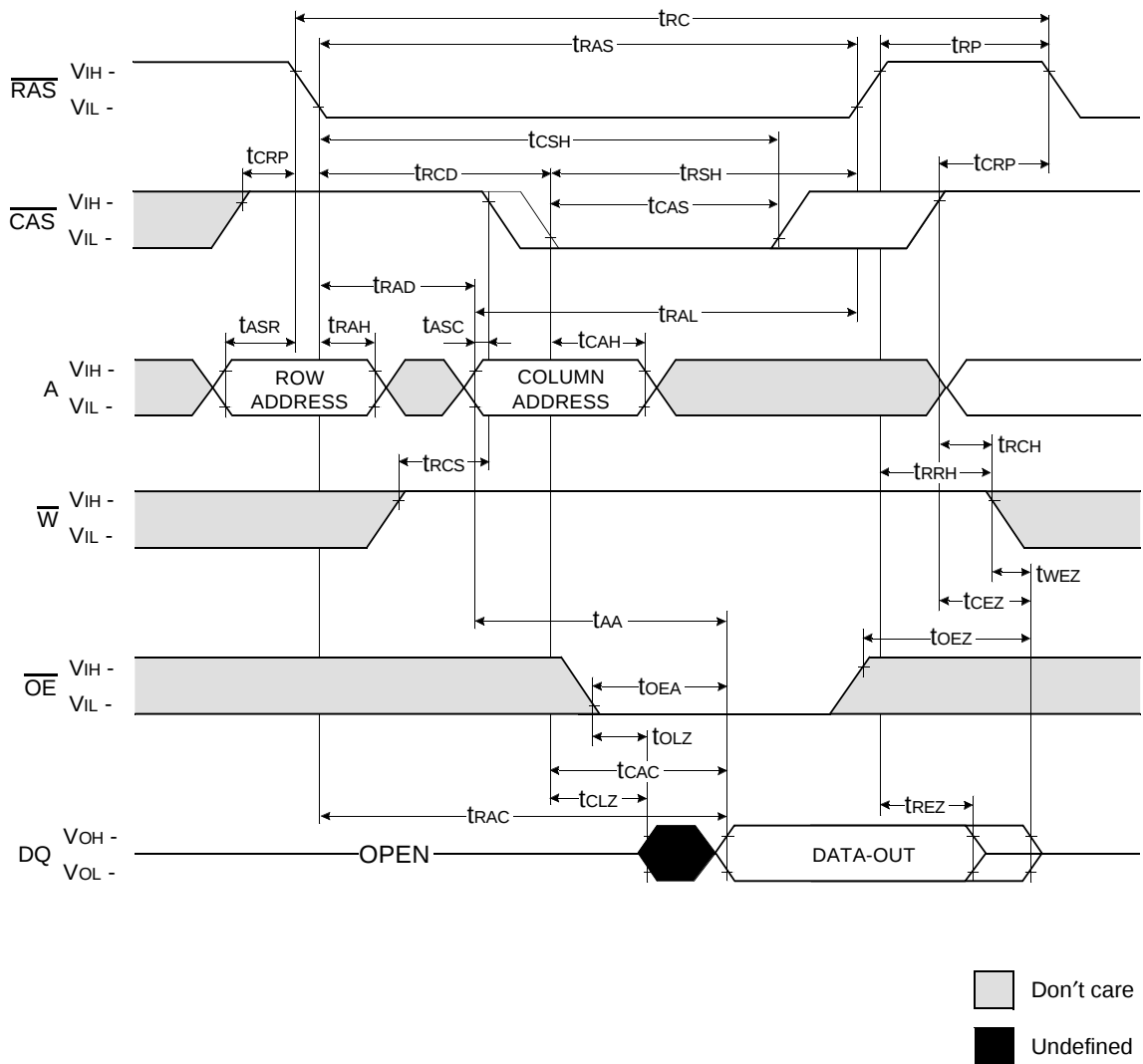
DRAM MODULE

NOTES

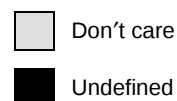
1. An initial pause of 200 μ s is required after power-up followed by any 8 $\overline{\text{RAS}}$ -only or $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycles before proper device operation is achieved.
2. Input voltage levels are V_{IH}/V_{IL} . $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 1 TTL loads and 100pF.
4. Operation within the $t_{RCD}(\text{max})$ limit insures that $t_{RAC}(\text{max})$ can be met. $t_{RCD}(\text{max})$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD}(\text{max})$ limit, then access time is controlled exclusively by t_{CAC} .
5. Assumes that $t_{RCD} \geq t_{RCD}(\text{max})$.
6. t_{WCS} , t_{RWD} , t_{CWD} , t_{AWD} and t_{CPWD} are not-restrictive operating parameter. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}(\text{min})$, the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{RWD} \geq t_{RWD}(\text{min})$, $t_{CWD} \geq t_{CWD}(\text{min})$, $t_{AWD} \geq t_{AWD}(\text{min})$ and $t_{CPWD} \geq t_{CPWD}(\text{min})$. The cycle is a read-modify-write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of data out(at access time) is indeterminated.
7. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
8. These parameters are referenced to the $\overline{\text{CAS}}$ leading edge in early write cycles.
9. Operation within the $t_{RAD}(\text{max})$ limit insures that $t_{RAC}(\text{max})$ can be met. $t_{RAD}(\text{max})$ is specified as reference point only. If t_{RAD} is greater than the specified $t_{RAD}(\text{max})$ limit access time is controlled by t_{AA} .
10. $t_{ASC} \geq 6\text{ns}$, Assume $t_T = 2.0\text{ns}$
11. For all of the refresh mode except distributed $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh, 4096 cycles of burst refresh must be executed within 16ms before and after self-refresh in order to meet refresh specification.
12. If $\overline{\text{RAS}}$ goes high before $\overline{\text{CAS}}$ high going, the open circuit condition of the output is achieved by $\overline{\text{CAS}}$ high going. If $\overline{\text{CAS}}$ goes high before $\overline{\text{RAS}}$ high going, the open circuit condition of the output is achieved by $\overline{\text{RAS}}$ going.
13. t_{ASC} , t_{CAH} are referenced to the earlier $\overline{\text{CAS}}$ falling edge.
14. t_{CP} is specified from the last $\overline{\text{CAS}}$ rising edge in the previous cycle to the first $\overline{\text{CAS}}$ falling edge in the next cycle.
15. t_{CWD} is referenced to the later $\overline{\text{CAS}}$ falling edge at word read-modify-write cycle.
16. t_{CWL} is specified from $\overline{\text{W}}$ falling edge to the earlier $\overline{\text{CAS}}$ rising edge.
17. t_{CSR} is referenced to earlier $\overline{\text{CAS}}$ falling edge to the $\overline{\text{RAS}}$ falling edge.

DRAM MODULE

READ CYCLE



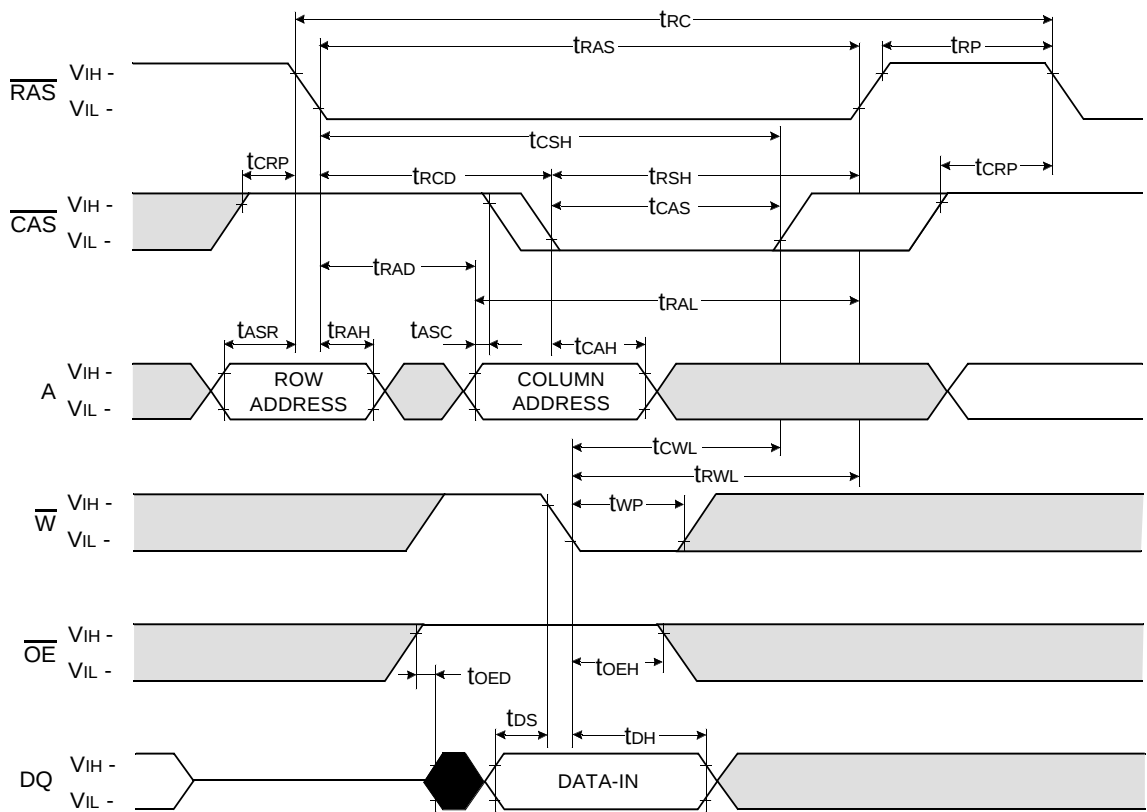
NOTE : DOUT = OPEN



DRAM MODULE

WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

NOTE : Dout = OPEN



Don't care
Undefined

The diagram illustrates the timing relationships for a memory device. The signals shown are:

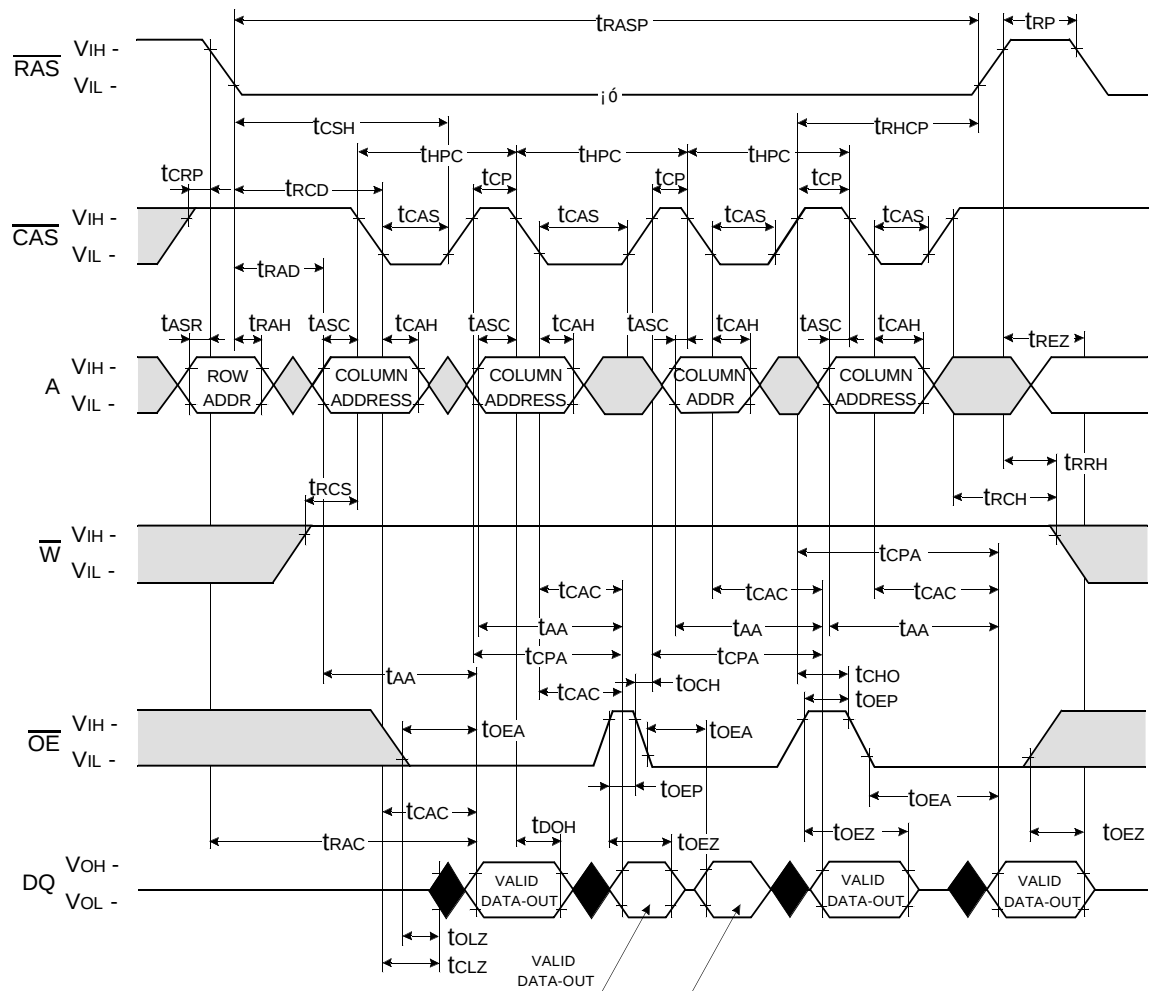
- RAS**: Row Address Strobe, with parameters t_{RAS} , t_{RWC} , and t_{RP} .
- CAS**: Column Address Strobe, with parameters t_{CRP} , t_{RCD} , t_{RSH} , t_{CAS} , t_{RAD} , t_{ASR} , t_{RAH} , t_{ASC} , t_{CAH} , and t_{CSH} .
- A**: Address bus, showing ROW ADDR and COLUMN ADDRESS phases.
- W**: Write Enable, with parameters t_{AWD} , t_{CWD} , t_{RWL} , t_{CWL} , and t_{WP} .
- OE**: Output Enable, with parameters t_{RWD} , t_{OEA} , t_{OLZ} , t_{CLZ} , t_{CAC} , t_{AA} , t_{RAC} , t_{OED} , t_{OEZ} , t_{DS} , and t_{DH} .
- DQ**: Data bus, showing VALID DATA-OUT and VALID DATA-IN phases.

The diagram uses standard timing notation with horizontal arrows indicating time intervals and vertical lines indicating signal transitions. Shaded areas represent signal levels during specific operations.

Undefined

DRAM MODULE

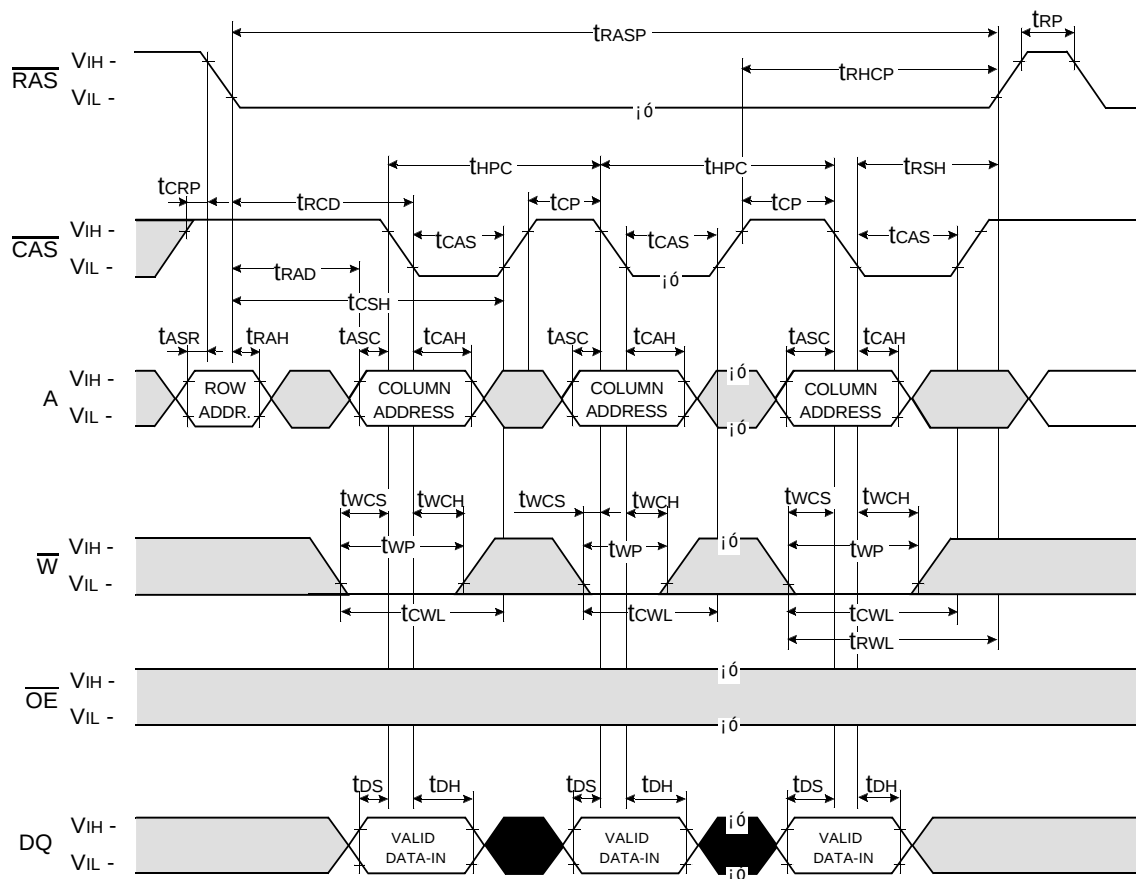
HYPER PAGE READ CYCLE



DRAM MODULE

HYPER PAGE WRITE CYCLE (EARLY WRITE)

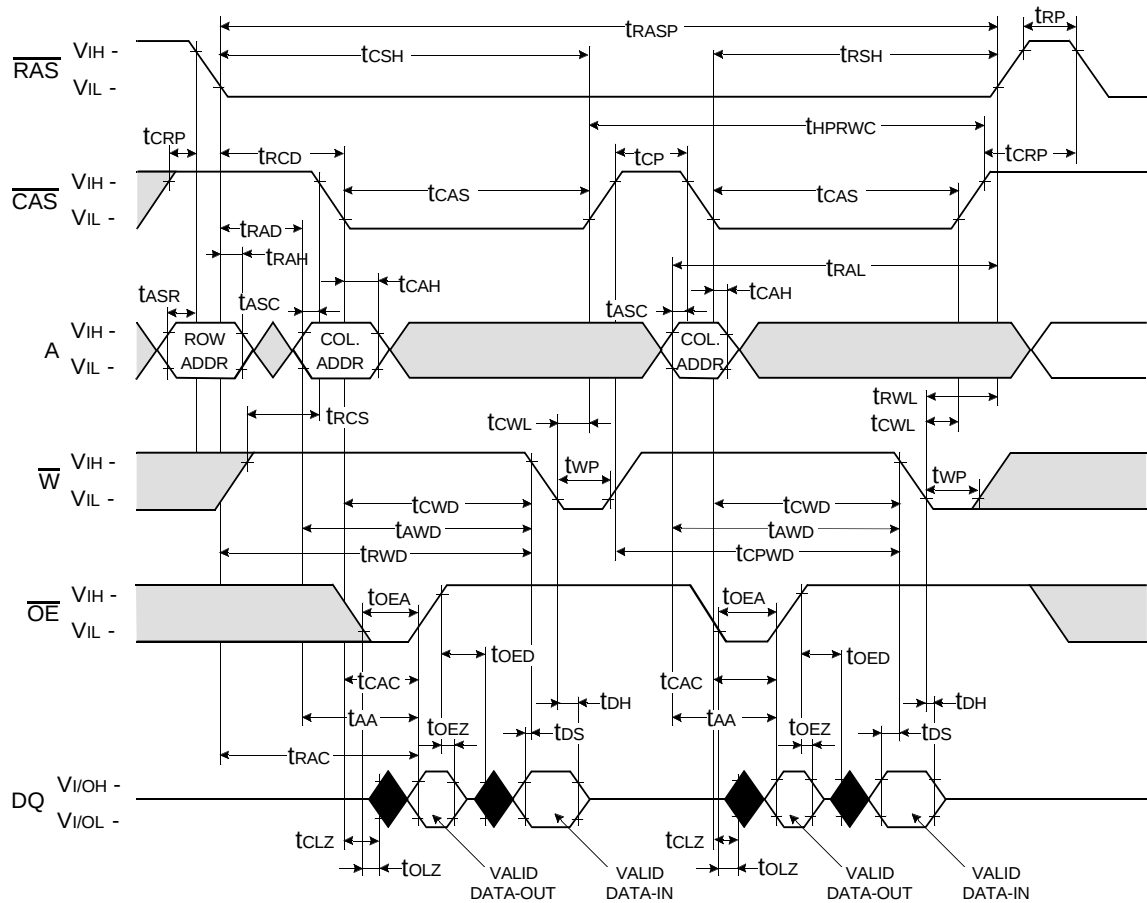
NOTE : DOUT = OPEN



Don't care
Undefined

DRAM MODULE

HYPER PAGE READ-MODIFY-WRITE CYCLE



Don't care
Undefined

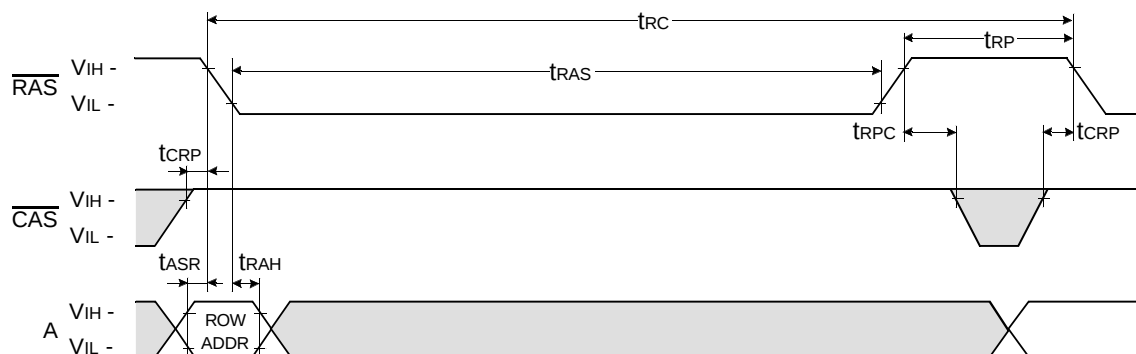
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DRAM MODULE

$\overline{\text{RAS}}$ - ONLY REFRESH CYCLE*

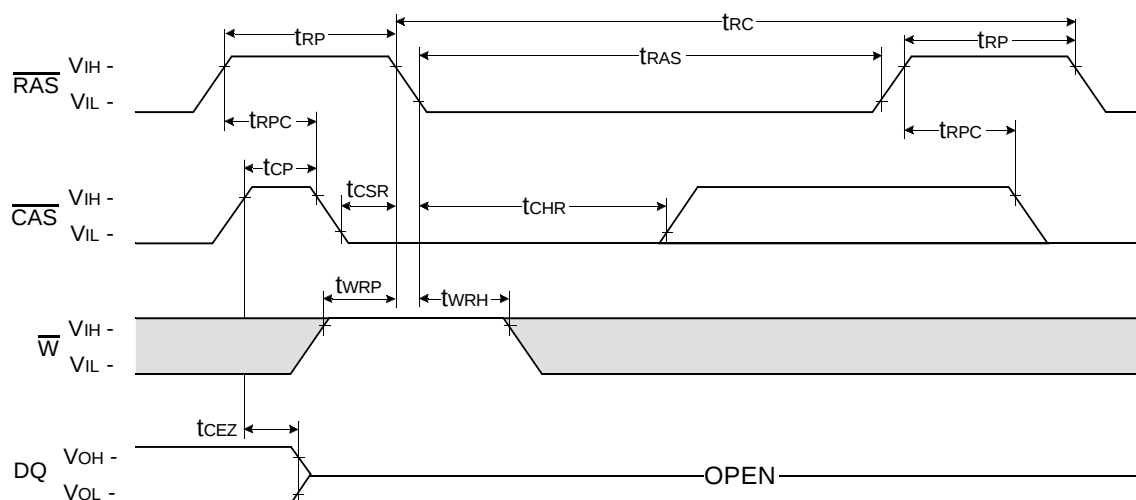
NOTE : $\overline{\text{W}}$, $\overline{\text{OE}}$, DIN = Don't care

DOUT = OPEN



$\overline{\text{CAS}}$ - BEFORE - $\overline{\text{RAS}}$ REFRESH CYCLE

NOTE : $\overline{\text{OE}}$, A = Don't care

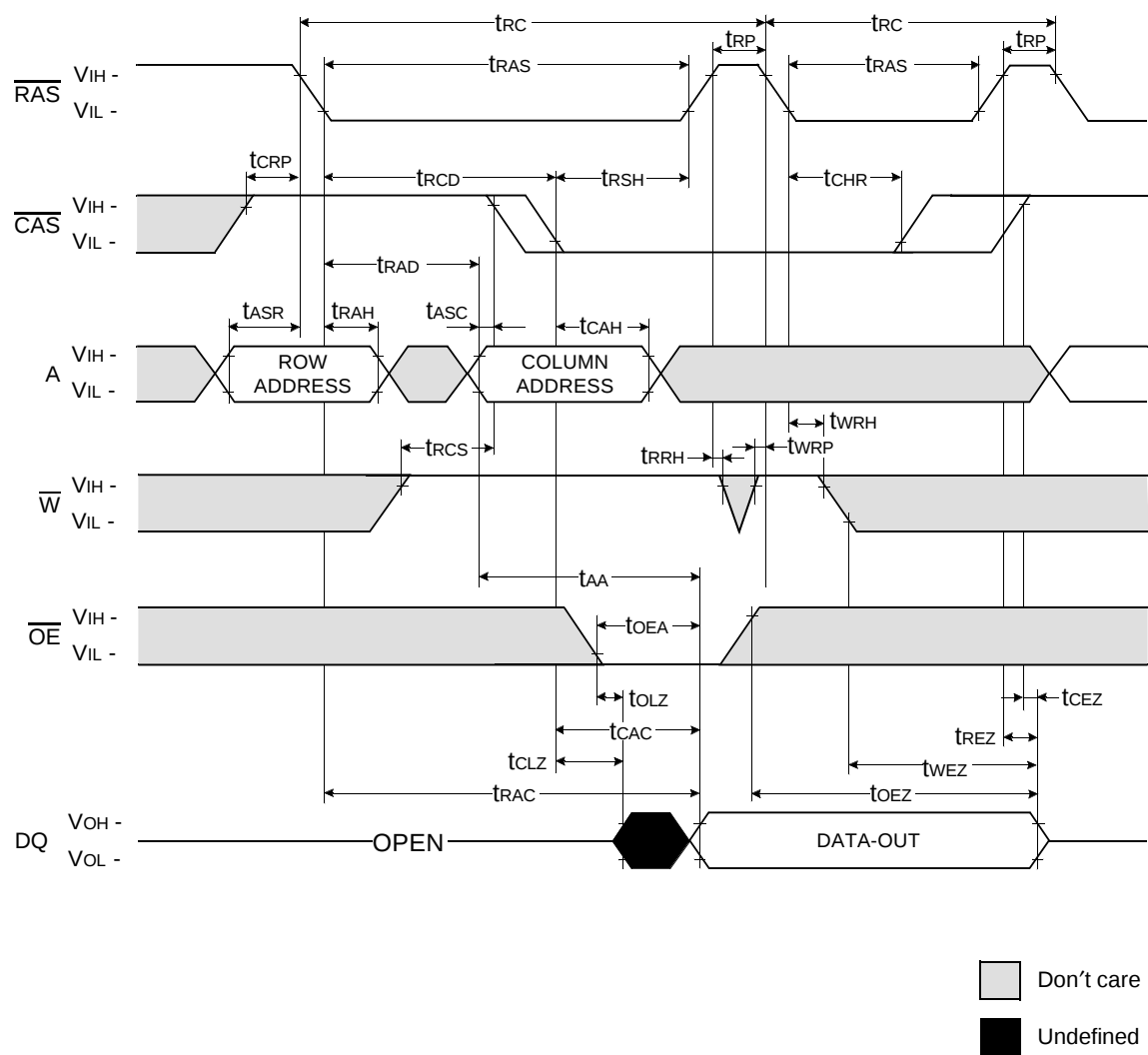


Don't care
Undefined

* In $\overline{\text{RAS}}$ -only refresh cycle of 64Mb A-die & B-die, when $\overline{\text{CAS}}$ signal transits from Low to High, the valid data may be cut off.

DRAM MODULE

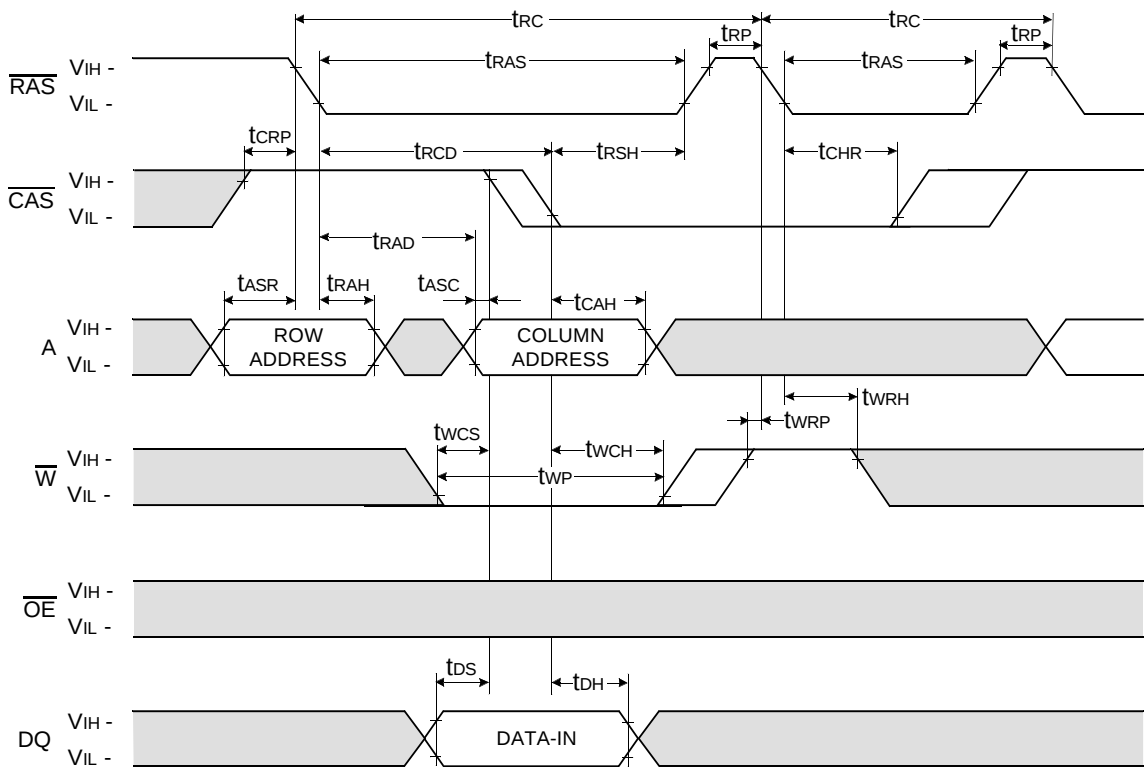
HIDDEN REFRESH CYCLE (READ)



DRAM MODULE

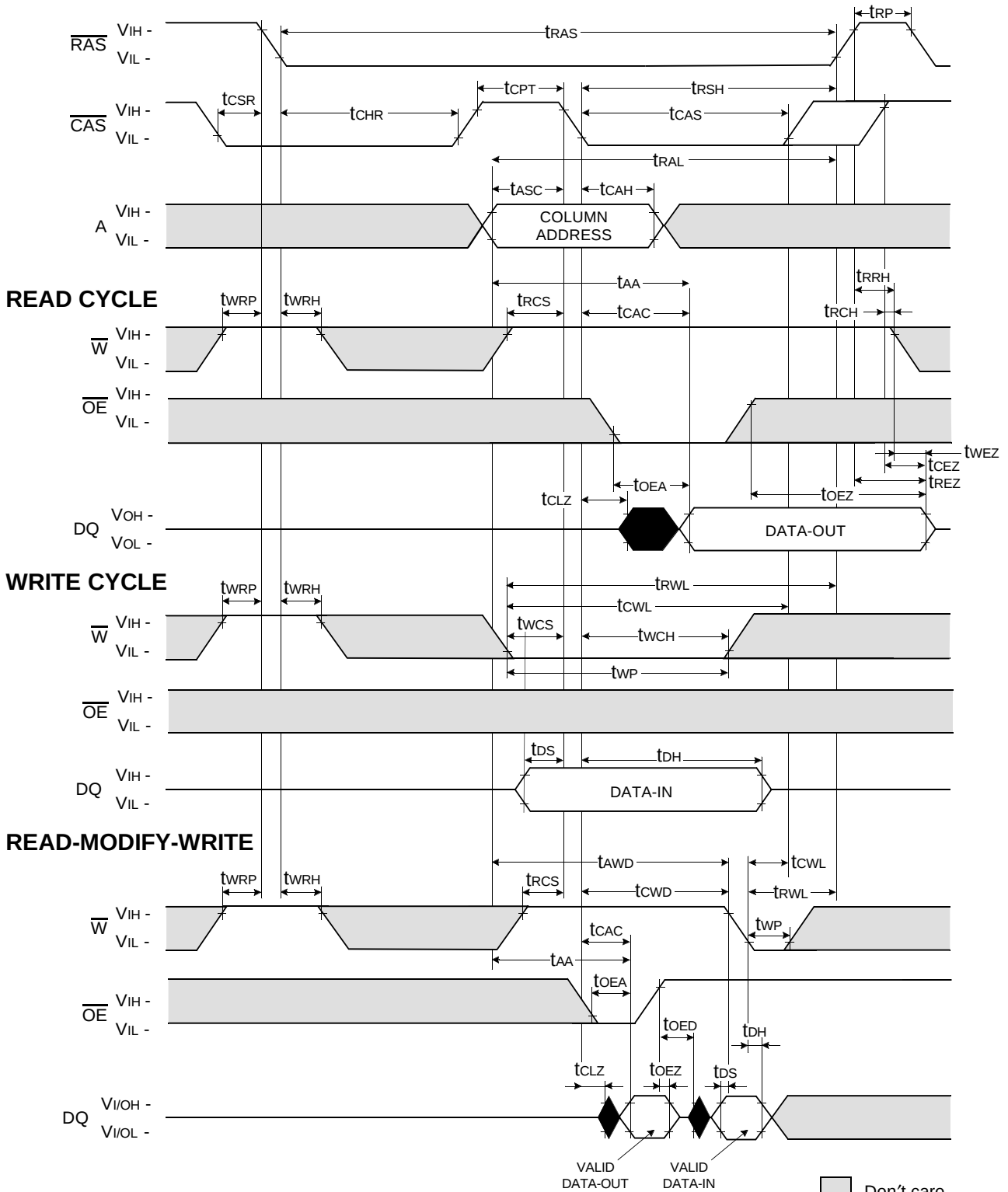
HIDDEN REFRESH CYCLE (WRITE)

NOTE : DOUT = OPEN



DRAM MODULE

CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE

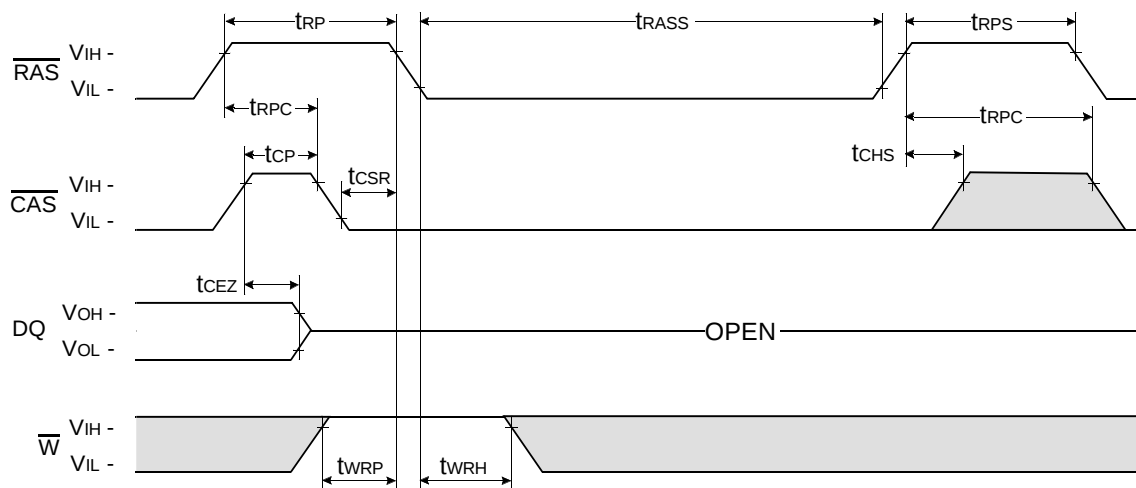


NOTE : This timing diagram is applied to all devices besides 64M DRAM based modules.

DRAM MODULE

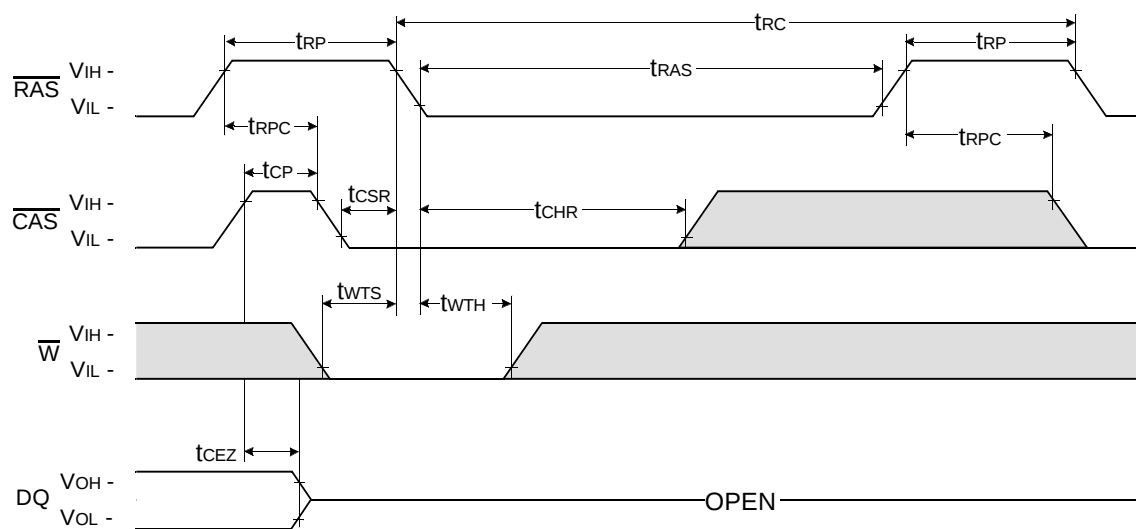
$\overline{\text{CAS}}$ - BEFORE - $\overline{\text{RAS}}$ SELF REFRESH CYCLE

NOTE : $\overline{\text{OE}}$, A = Don't care



TEST MODE IN CYCLE

NOTE : $\overline{\text{OE}}$, A = Don't care

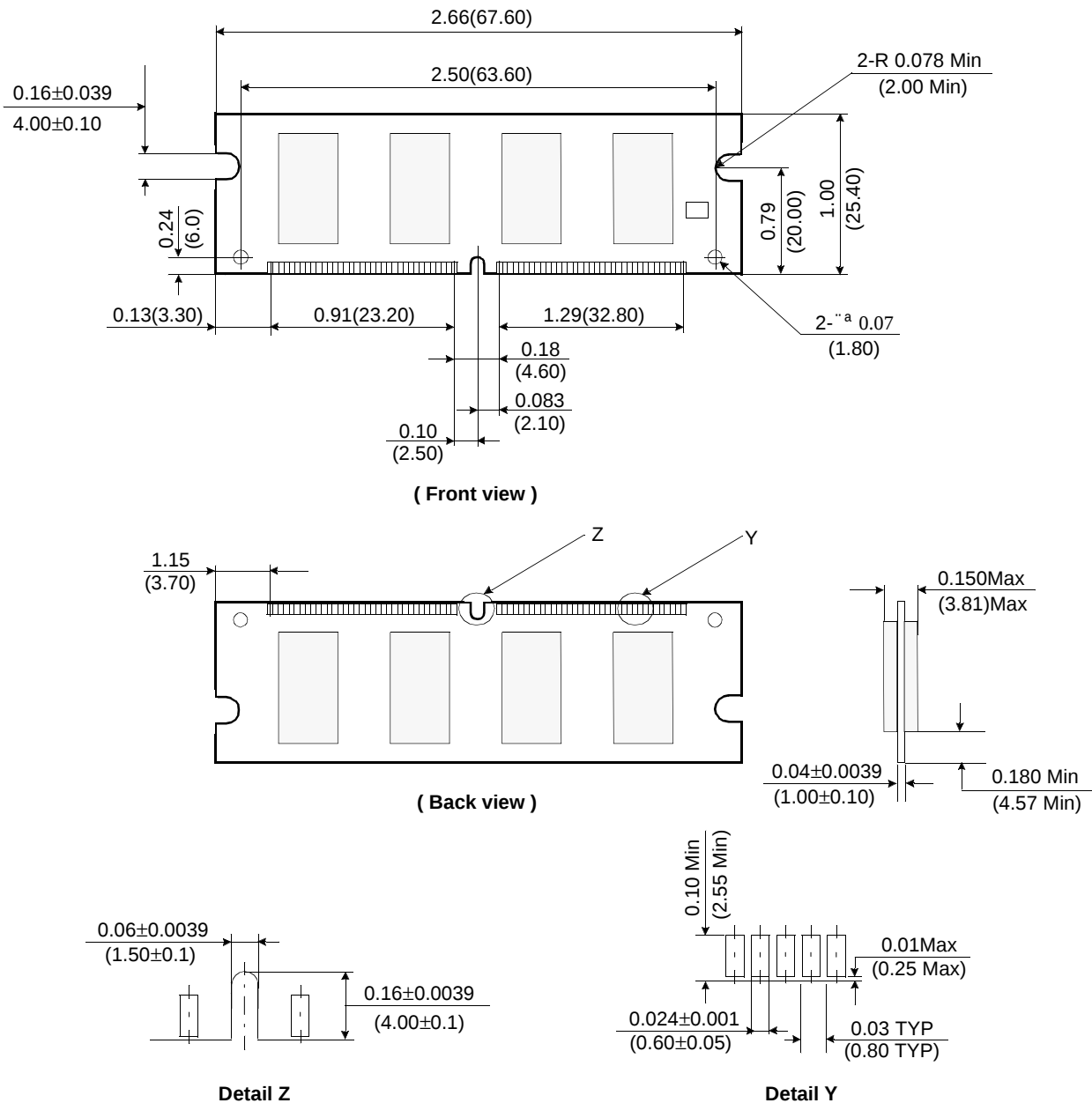


□ Don't care
■ Undefined

DRAM MODULE

PACKAGE DIMENSIONS

Units : Inches (millimeters)



Tolerances : ±.005(.13) unless otherwise specified

The used device is 2MX8 DRAM with EDO mode, TSOP
DRAM Part No. : KMM466F203CS2-L -- KM48V2004CS-L
KMM466F213CS2-L -- KM48V2104CS-L

Revision History
Rev 2.0 : November 1997