

## 8M x 8bit CMOS Dynamic RAM with Fast Page Mode

### DESCRIPTION

This is a family of 8,388,608 x 8 bit Fast Page Mode CMOS DRAMs. Fast Page Mode offers high speed random access of memory cells within the same row. Refresh cycle(4K Ref. or 8K Ref.), access time (-45, -5 or -6), power consumption(Normal or Low power) are optional features of this family. All of this family have  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh,  $\overline{\text{RAS}}$ -only refresh and Hidden refresh capabilities. Furthermore, Self-refresh operation is available in L-version. This 8Mx8 Fast Page Mode DRAM family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability.

### FEATURES

#### • Part Identification

- KM48V8000C/C-L(3.3V, 8K Ref.)
- KM48V8100C/C-L(3.3V, 4K Ref.)

#### • Active Power Dissipation

Unit : mW

| Speed | 8K  | 4K  |
|-------|-----|-----|
| -45   | 324 | 432 |
| -5    | 288 | 396 |
| -6    | 252 | 360 |

#### • Refresh Cycles

| Part NO.    | Refresh cycle | Refresh time |       |
|-------------|---------------|--------------|-------|
|             |               | Normal       | L-ver |
| KM48V8000C* | 8K            | 64ms         | 128ms |
| KM48V8100C  | 4K            |              |       |

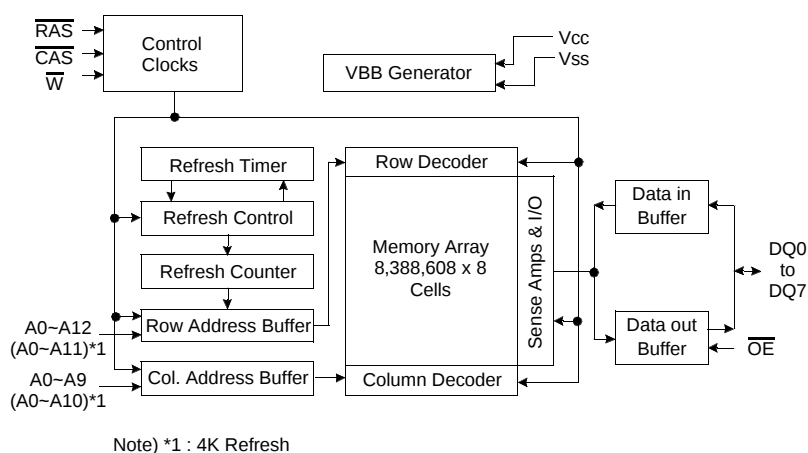
- \* Access mode &  $\overline{\text{RAS}}$  only refresh mode  
: 8K cycle/64ms(Normal), 8K cycle/128ms(L-ver.)  
 $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  & Hidden refresh mode  
: 4K cycle/64ms(Normal), 4K cycle/128ms(L-ver.)

#### • Performance Range

| Speed | t <sub>RAC</sub> | t <sub>CAC</sub> | t <sub>RC</sub> | t <sub>PC</sub> |
|-------|------------------|------------------|-----------------|-----------------|
| -45   | 45ns             | 12ns             | 80ns            | 31ns            |
| -5    | 50ns             | 13ns             | 90ns            | 35ns            |
| -6    | 60ns             | 15ns             | 110ns           | 40ns            |

- Fast Page Mode operation
- $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh capability
- $\overline{\text{RAS}}$ -only and Hidden refresh capability
- Self-refresh capability (L-ver only)
- Fast parallel test mode capability
- LVTTTL(3.3V) compatible inputs and outputs
- Early Write or output enable controlled write
- JEDEC Standard pinout
- Available in Plastic SOJ and TSOP(II) packages
- +3.3V±0.3V power supply

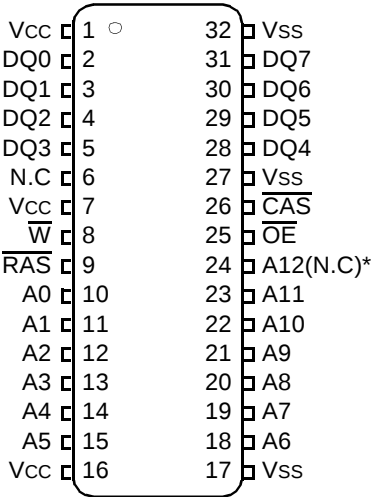
### FUNCTIONAL BLOCK DIAGRAM



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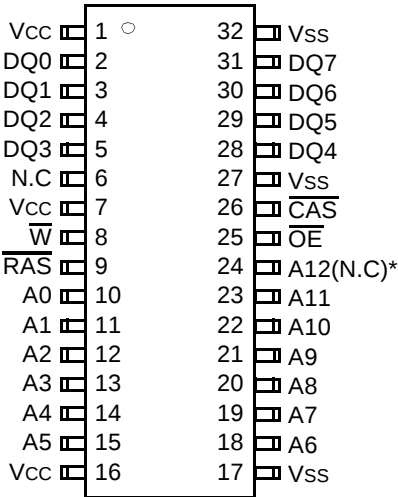
PIN CONFIGURATION (Top Views)

•KM48V80(1)00CK



(K : 400mil SOJ)

•KM48V80(1)00CS



(S : 400mil TSOP(II))

\* (N.C) : N.C for 4K Refresh product

| Pin Name | Pin Function               |
|----------|----------------------------|
| A0 - A12 | Address Inputs(8K Product) |
| A0 - A11 | Address Inputs(4K Product) |
| DQ0 - 7  | Data In/Out                |
| Vss      | Ground                     |
| RAS      | Row Address Strobe         |
| CAS      | Column Address Strobe      |
| W        | Read/Write Input           |
| OE       | Data Output Enable         |
| Vcc      | Power(+3.3V)               |
| N.C      | No Connection              |

**ABSOLUTE MAXIMUM RATINGS**

| Parameter                             | Symbol                            | Rating       | Units |
|---------------------------------------|-----------------------------------|--------------|-------|
| Voltage on any pin relative to Vss    | V <sub>IN</sub> ,V <sub>OUT</sub> | -0.5 to +4.6 | V     |
| Voltage on Vcc supply relative to Vss | V <sub>CC</sub>                   | -0.5 to +4.6 | V     |
| Storage Temperature                   | T <sub>stg</sub>                  | -55 to +150  | °C    |
| Power Dissipation                     | P <sub>D</sub>                    | 1            | W     |
| Short Circuit Output Current          | I <sub>OS</sub>                   | 50           | mA    |

\* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**RECOMMENDED OPERATING CONDITIONS** (Voltage referenced to Vss, T<sub>A</sub>= 0 to 70°C)

| Parameter          | Symbol          | Min                | Typ | Max                                | Units |
|--------------------|-----------------|--------------------|-----|------------------------------------|-------|
| Supply Voltage     | V <sub>CC</sub> | 3.0                | 3.3 | 3.6                                | V     |
| Ground             | V <sub>SS</sub> | 0                  | 0   | 0                                  | V     |
| Input High Voltage | V <sub>IH</sub> | 2.0                | -   | V <sub>CC</sub> +0.3* <sup>1</sup> | V     |
| Input Low Voltage  | V <sub>IL</sub> | -0.3* <sup>2</sup> | -   | 0.8                                | V     |

\*1 :V<sub>CC</sub>+1.3V at pulse width≤15ns which is measured at V<sub>CC</sub>

\*2 : -1.3 at pulse width≤15ns which is measured at V<sub>SS</sub>

**DC AND OPERATING CHARACTERISTICS** (Recommended operating conditions unless otherwise noted.)

| Parameter                                                                                                        | Symbol            | Min | Max | Units |
|------------------------------------------------------------------------------------------------------------------|-------------------|-----|-----|-------|
| Input Leakage Current (Any input 0≤V <sub>IN</sub> ≤V <sub>CC</sub> +0.3V, all other pins not under test=0 Volt) | I <sub>I(L)</sub> | -5  | 5   | uA    |
| Output Leakage Current (Data out is disabled, 0V≤V <sub>OUT</sub> ≤V <sub>CC</sub> )                             | I <sub>O(L)</sub> | -5  | 5   | uA    |
| Output High Voltage Level(I <sub>OH</sub> =-2mA)                                                                 | V <sub>OH</sub>   | 2.4 | -   | V     |
| Output Low Voltage Level(I <sub>OL</sub> =2mA)                                                                   | V <sub>OL</sub>   | -   | 0.4 | V     |

## DC AND OPERATING CHARACTERISTICS (Continued)

| Symbol           | Power       | Speed      | Max        |            | Units |
|------------------|-------------|------------|------------|------------|-------|
|                  |             |            | KM48V8000C | KM48V8100C |       |
| I <sub>CC1</sub> | Don't care  | -45        | 90         | 120        | mA    |
|                  |             | -5         | 80         | 110        | mA    |
|                  |             | -6         | 70         | 100        | mA    |
| I <sub>CC2</sub> | Normal<br>L | Don't care | 1          | 1          | mA    |
|                  |             |            | 1          | 1          | mA    |
| I <sub>CC3</sub> | Don't care  | -45        | 90         | 120        | mA    |
|                  |             | -5         | 80         | 110        | mA    |
|                  |             | -6         | 70         | 100        | mA    |
| I <sub>CC4</sub> | Don't care  | -45        | 70         | 70         | mA    |
|                  |             | -5         | 60         | 60         | mA    |
|                  |             | -6         | 50         | 50         | mA    |
| I <sub>CC5</sub> | Normal<br>L | Don't care | 500        | 500        | μA    |
|                  |             |            | 200        | 200        | μA    |
| I <sub>CC6</sub> | Don't care  | -45        | 120        | 120        | mA    |
|                  |             | -5         | 110        | 110        | mA    |
|                  |             | -6         | 100        | 100        | mA    |
| I <sub>CC7</sub> | L           | Don't care | 350        | 350        | μA    |
| I <sub>CCS</sub> | L           | Don't care | 350        | 350        | μA    |

I<sub>CC1</sub>\* : Operating Current ( $\overline{RAS}$  and  $\overline{CAS}$ , Address cycling @ $t_{RC}=\min$ .)

I<sub>CC2</sub> : Standby Current ( $\overline{RAS}=\overline{CAS}=\overline{W}=V_{IH}$ )

I<sub>CC3</sub>\* :  $\overline{RAS}$ -only Refresh Current ( $\overline{CAS}=V_{IH}$ ,  $\overline{RAS}$ , Address cycling @ $t_{RC}=\min$ .)

I<sub>CC4</sub>\* : Fast Page Mode Current ( $\overline{RAS}=V_{IL}$ ,  $\overline{CAS}$ , Address cycling @ $t_{PC}=\min$ .)

I<sub>CC5</sub> : Standby Current ( $\overline{RAS}=\overline{CAS}=\overline{W}=V_{CC}-0.2V$ )

I<sub>CC6</sub>\* :  $\overline{CAS}$ -Before- $\overline{RAS}$  Refresh Current ( $\overline{RAS}$  and  $\overline{CAS}$  cycling @ $t_{RC}=\min$ )

I<sub>CC7</sub> : Battery back-up current, Average power supply current, Battery back-up mode

Input high voltage( $V_{IH}$ )= $V_{CC}-0.2V$ , Input low voltage( $V_{IL}$ )= $0.2V$ ,  $\overline{CAS}=\overline{CAS}$ -before- $\overline{RAS}$  cycling or  $0.2V$ ,

$\overline{W}$ ,  $\overline{OE}=V_{IH}$ , Address=Don't care,  $DQ=Open$ ,  $TRC=31.25\mu s$

I<sub>CCS</sub> : Self Refresh Current

$\overline{RAS}=\overline{CAS}=0.2V$ ,  $\overline{W}=\overline{OE}=A0 \sim A12(A11)=V_{CC}-0.2V$  or  $0.2V$ ,  $DQ0 \sim DQ7=V_{CC}-0.2V$ ,  $0.2V$  or  $Open$

**\*Note :** I<sub>CC1</sub>, I<sub>CC3</sub>, I<sub>CC4</sub> and I<sub>CC6</sub> are dependent on output loading and cycle rates. Specified values are obtained with the output open. I<sub>CC</sub> is specified as an average current. In I<sub>CC1</sub>, I<sub>CC3</sub> and I<sub>CC6</sub>, address can be changed maximum once while  $\overline{RAS}=V_{IL}$ . In I<sub>CC4</sub>, address can be changed maximum once within one fast page mode cycle time,  $t_{PC}$ .

## CAPACITANCE (T<sub>A</sub>=25°C, V<sub>CC</sub>=3.3V, f=1MHz)

| Parameter                                                                                                                | Symbol           | Min | Max | Units |
|--------------------------------------------------------------------------------------------------------------------------|------------------|-----|-----|-------|
| Input capacitance [A0 ~ A12]                                                                                             | C <sub>IN1</sub> | -   | 5   | pF    |
| Input capacitance [ $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , $\overline{\text{W}}$ , $\overline{\text{OE}}$ ] | C <sub>IN2</sub> | -   | 7   | pF    |
| Output capacitance [DQ0 - DQ7]                                                                                           | C <sub>DQ</sub>  | -   | 7   | pF    |

## AC CHARACTERISTICS (0°C ≤ T<sub>A</sub> ≤ 70°C, See note 2)

Test condition : V<sub>CC</sub>=3.3V±0.3V, V<sub>IH</sub>/V<sub>IL</sub>=2.2/0.7V, V<sub>OH</sub>/V<sub>OL</sub>=2.0/0.8V

| Parameter                                                         | Symbol           | -45 |     | -5  |     | -6  |     | Units | Note   |
|-------------------------------------------------------------------|------------------|-----|-----|-----|-----|-----|-----|-------|--------|
|                                                                   |                  | Min | Max | Min | Max | Min | Max |       |        |
| Random read or write cycle time                                   | t <sub>RC</sub>  | 80  |     | 90  |     | 110 |     | ns    |        |
| Read-modify-write cycle time                                      | t <sub>RWC</sub> | 115 |     | 133 |     | 153 |     | ns    |        |
| Access time from $\overline{\text{RAS}}$                          | t <sub>RAC</sub> |     | 45  |     | 50  |     | 60  | ns    | 3,4,10 |
| Access time from $\overline{\text{CAS}}$                          | t <sub>CAC</sub> |     | 12  |     | 13  |     | 15  | ns    | 3,4,5  |
| Access time from column address                                   | t <sub>AA</sub>  |     | 23  |     | 25  |     | 30  | ns    | 3,10   |
| $\overline{\text{CAS}}$ to output in Low-Z                        | t <sub>CLZ</sub> | 0   |     | 0   |     | 0   |     | ns    | 3      |
| Output buffer turn-off delay                                      | t <sub>OFF</sub> | 0   | 13  | 0   | 13  | 0   | 13  | ns    | 6      |
| Transition time (rise and fall)                                   | t <sub>r</sub>   | 1   | 50  | 1   | 50  | 1   | 50  | ns    | 2      |
| $\overline{\text{RAS}}$ precharge time                            | t <sub>RP</sub>  | 25  |     | 30  |     | 40  |     | ns    |        |
| $\overline{\text{RAS}}$ pulse width                               | t <sub>RAS</sub> | 45  | 10K | 50  | 10K | 60  | 10K | ns    |        |
| $\overline{\text{RAS}}$ hold time                                 | t <sub>RSH</sub> | 12  |     | 13  |     | 15  |     | ns    |        |
| $\overline{\text{CAS}}$ hold time                                 | t <sub>CSH</sub> | 45  |     | 50  |     | 60  |     | ns    |        |
| $\overline{\text{CAS}}$ pulse width                               | t <sub>CAS</sub> | 12  | 10K | 13  | 10K | 15  | 10K | ns    |        |
| $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time     | t <sub>RCD</sub> | 18  | 33  | 20  | 37  | 20  | 45  | ns    | 4      |
| $\overline{\text{RAS}}$ to column address delay time              | t <sub>RAD</sub> | 13  | 22  | 15  | 25  | 15  | 30  | ns    | 10     |
| $\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time | t <sub>CRP</sub> | 5   |     | 5   |     | 5   |     | ns    |        |
| Row address set-up time                                           | t <sub>ASR</sub> | 0   |     | 0   |     | 0   |     | ns    |        |
| Row address hold time                                             | t <sub>RAH</sub> | 8   |     | 10  |     | 10  |     | ns    |        |
| Column address set-up time                                        | t <sub>ASC</sub> | 0   |     | 0   |     | 0   |     | ns    |        |
| Column address hold time                                          | t <sub>CAH</sub> | 8   |     | 10  |     | 10  |     | ns    |        |
| Column address to $\overline{\text{RAS}}$ lead time               | t <sub>RAL</sub> | 23  |     | 25  |     | 30  |     | ns    |        |
| Read command set-up time                                          | t <sub>RCS</sub> | 0   |     | 0   |     | 0   |     | ns    |        |
| Read command hold time referenced to $\overline{\text{CAS}}$      | t <sub>RCH</sub> | 0   |     | 0   |     | 0   |     | ns    | 8      |
| Read command hold time referenced to $\overline{\text{RAS}}$      | t <sub>RRH</sub> | 0   |     | 0   |     | 0   |     | ns    | 8      |
| Write command hold time                                           | t <sub>WCH</sub> | 8   |     | 10  |     | 10  |     | ns    |        |
| Write command pulse width                                         | t <sub>WP</sub>  | 8   |     | 10  |     | 10  |     | ns    |        |
| Write command to $\overline{\text{RAS}}$ lead time                | t <sub>RWL</sub> | 13  |     | 15  |     | 15  |     | ns    |        |
| Write command to $\overline{\text{CAS}}$ lead time                | t <sub>CWL</sub> | 12  |     | 13  |     | 15  |     | ns    |        |
| Data set-up time                                                  | t <sub>DS</sub>  | 0   |     | 0   |     | 0   |     | ns    | 9      |
| Data hold time                                                    | t <sub>DH</sub>  | 10  |     | 10  |     | 10  |     | ns    | 9      |

## AC CHARACTERISTICS (Continued)

| Parameter                                                                                               | Symbol | -45 |      | -5  |      | -6  |      | Units | Note     |
|---------------------------------------------------------------------------------------------------------|--------|-----|------|-----|------|-----|------|-------|----------|
|                                                                                                         |        | Min | Max  | Min | Max  | Min | Max  |       |          |
| Refresh period (Normal)                                                                                 | tREF   |     | 64   |     | 64   |     | 64   | ms    |          |
| Refresh period (L-ver)                                                                                  | tREF   |     | 128  |     | 128  |     | 128  | ms    |          |
| Write command set-up time                                                                               | twCS   | 0   |      | 0   |      | 0   |      | ns    | 7        |
| $\overline{\text{CAS}}$ to $\overline{\text{W}}$ delay time                                             | tcWD   | 32  |      | 36  |      | 38  |      | ns    | 7        |
| $\overline{\text{RAS}}$ to $\overline{\text{W}}$ delay time                                             | trWD   | 67  |      | 73  |      | 83  |      | ns    | 7        |
| Column address to $\overline{\text{W}}$ delay time                                                      | tAWD   | 43  |      | 48  |      | 53  |      | ns    | 7        |
| $\overline{\text{CAS}}$ precharge $\overline{\text{W}}$ delay time                                      | tcpWD  | 48  |      | 53  |      | 60  |      | ns    |          |
| $\overline{\text{CAS}}$ set-up time ( $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh) | tCSR   | 5   |      | 5   |      | 5   |      | ns    |          |
| $\overline{\text{CAS}}$ hold time ( $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)   | tCHR   | 10  |      | 10  |      | 10  |      | ns    |          |
| $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ precharge time                                       | trPC   | 5   |      | 5   |      | 5   |      | ns    |          |
| Access time from $\overline{\text{CAS}}$ precharge                                                      | tCPA   |     | 26   |     | 30   |     | 35   | ns    | 3        |
| Fast Page mode cycle time                                                                               | tPC    | 31  |      | 35  |      | 40  |      | ns    |          |
| Fast Page mode read-modify-write cycle time                                                             | tPRWC  | 70  |      | 76  |      | 85  |      | ns    |          |
| $\overline{\text{CAS}}$ precharge time (Fast page cycle)                                                | tCP    | 9   |      | 10  |      | 10  |      | ns    |          |
| $\overline{\text{RAS}}$ pulse width (Fast page cycle)                                                   | trASP  | 45  | 200K | 50  | 200K | 60  | 200K | ns    |          |
| $\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge                                | trHCP  | 28  |      | 30  |      | 35  |      | ns    |          |
| $\overline{\text{OE}}$ access time                                                                      | toEA   |     | 12   |     | 13   |     | 15   | ns    | 3        |
| $\overline{\text{OE}}$ to data delay                                                                    | toED   | 12  |      | 13  |      | 13  |      | ns    |          |
| Output buffer turn off delay time from $\overline{\text{OE}}$                                           | toEZ   | 0   | 13   | 0   | 13   | 0   | 13   | ns    | 6        |
| $\overline{\text{OE}}$ command hold time                                                                | toEH   | 12  |      | 13  |      | 15  |      | ns    |          |
| Write command set-up time (Test mode in)                                                                | twTS   | 10  |      | 10  |      | 10  |      | ns    | 11       |
| Write command hold time (Test mode in)                                                                  | twTH   | 15  |      | 15  |      | 15  |      | ns    | 11       |
| $\overline{\text{W}}$ to $\overline{\text{RAS}}$ precharge time (C-B-R refresh)                         | twRP   | 10  |      | 10  |      | 10  |      | ns    |          |
| $\overline{\text{W}}$ to $\overline{\text{RAS}}$ hold time (C-B-R refresh)                              | twRH   | 10  |      | 10  |      | 10  |      | ns    |          |
| $\overline{\text{RAS}}$ pulse width (C-B-R self refresh)                                                | trASS  | 100 |      | 100 |      | 100 |      | us    | 13,14,15 |
| $\overline{\text{RAS}}$ precharge time (C-B-R self refresh)                                             | trPS   | 80  |      | 90  |      | 110 |      | ns    | 13,14,15 |
| $\overline{\text{CAS}}$ hold time (C-B-R self refresh)                                                  | tCHS   | -50 |      | -50 |      | -50 |      | ns    | 13,14,15 |

## TEST MODE CYCLE

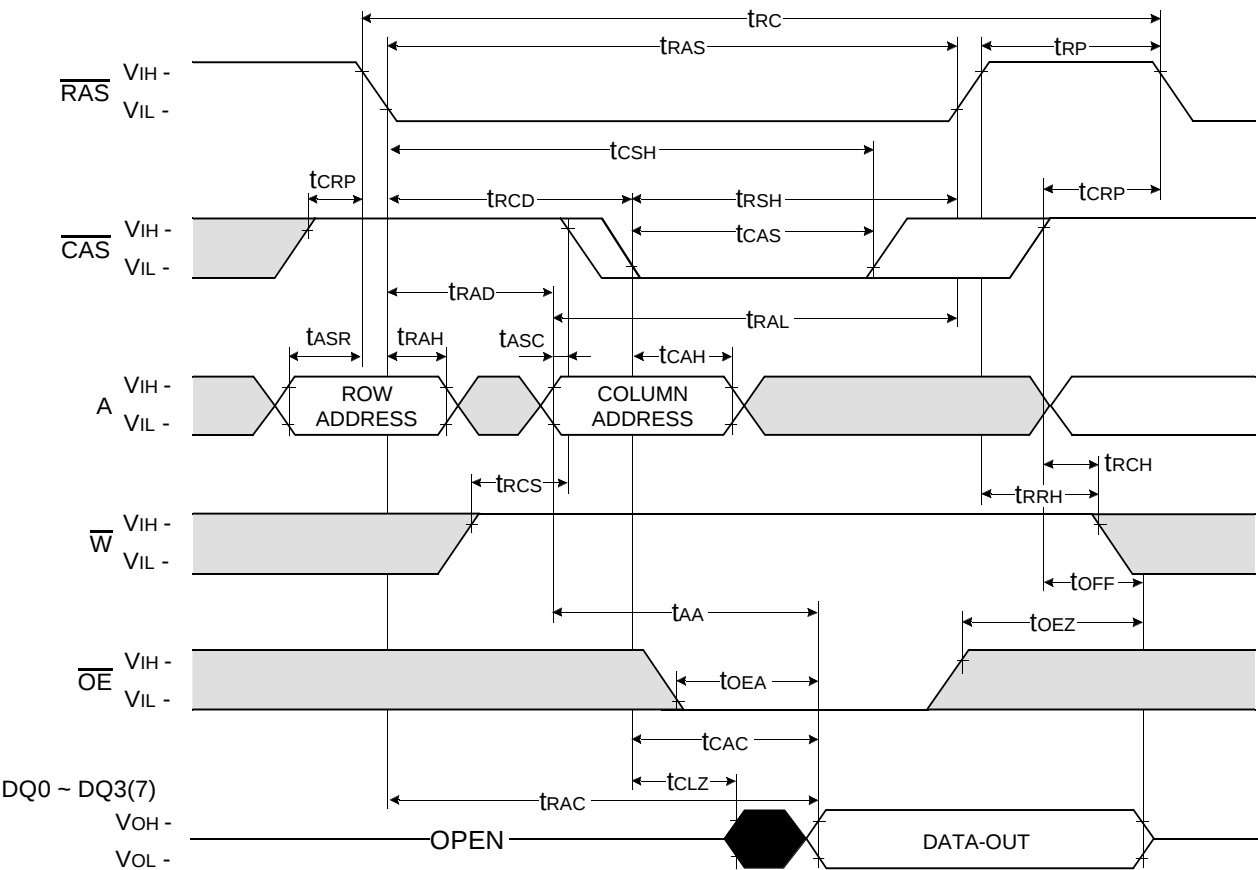
( Note 11 )

| Parameter                                                   | Symbol            | -45 |      | -5  |      | -6  |      | Units | Note      |
|-------------------------------------------------------------|-------------------|-----|------|-----|------|-----|------|-------|-----------|
|                                                             |                   | Min | Max  | Min | Max  | Min | Max  |       |           |
| Random read or write cycle time                             | t <sub>RC</sub>   | 85  |      | 95  |      | 115 |      | ns    |           |
| Read-modify-write cycle time                                | t <sub>RWC</sub>  | 120 |      | 138 |      | 160 |      | ns    |           |
| Access time from $\overline{\text{RAS}}$                    | t <sub>RAC</sub>  |     | 50   |     | 55   |     | 65   | ns    | 3,4,10,12 |
| Access time from $\overline{\text{CAS}}$                    | t <sub>CAC</sub>  |     | 17   |     | 18   |     | 20   | ns    | 3,4,5,12  |
| Access time from column address                             | t <sub>AA</sub>   |     | 28   |     | 30   |     | 35   | ns    | 3,10,12   |
| $\overline{\text{RAS}}$ pulse width                         | t <sub>RAS</sub>  | 50  | 10K  | 55  | 10K  | 65  | 10K  | ns    |           |
| $\overline{\text{CAS}}$ pulse width                         | t <sub>CAS</sub>  | 17  | 10K  | 18  | 10K  | 20  | 10K  | ns    |           |
| $\overline{\text{RAS}}$ hold time                           | t <sub>RS</sub>   | 17  |      | 18  |      | 20  |      | ns    |           |
| $\overline{\text{CAS}}$ hold time                           | t <sub>CS</sub>   | 50  |      | 55  |      | 65  |      | ns    |           |
| Column Address to $\overline{\text{RAS}}$ lead time         | t <sub>RAL</sub>  | 28  |      | 30  |      | 35  |      | ns    |           |
| $\overline{\text{CAS}}$ to $\overline{\text{W}}$ delay time | t <sub>CWD</sub>  | 37  |      | 41  |      | 43  |      | ns    | 7         |
| $\overline{\text{RAS}}$ to $\overline{\text{W}}$ delay time | t <sub>RWD</sub>  | 72  |      | 78  |      | 88  |      | ns    | 7         |
| Column Address to $\overline{\text{W}}$ delay time          | t <sub>AWD</sub>  | 48  |      | 53  |      | 58  |      | ns    | 7         |
| Fast Page mode cycle time                                   | t <sub>PC</sub>   | 36  |      | 40  |      | 45  |      | ns    |           |
| Fast Page mode read-modify-write cycle time                 | t <sub>PRWC</sub> | 75  |      | 81  |      | 90  |      | ns    |           |
| $\overline{\text{RAS}}$ pulse width (Fast page cycle)       | t <sub>RASP</sub> | 50  | 200K | 55  | 200K | 65  | 200K | ns    |           |
| Access time from $\overline{\text{CAS}}$ precharge          | t <sub>CPA</sub>  |     | 31   |     | 35   |     | 40   | ns    | 3         |
| $\overline{\text{OE}}$ access time                          | t <sub>OE</sub>   |     | 17   |     | 18   |     | 20   | ns    | 3         |
| $\overline{\text{OE}}$ to data delay                        | t <sub>OED</sub>  | 17  |      | 18  |      | 18  |      | ns    |           |
| $\overline{\text{OE}}$ command hold time                    | t <sub>OE</sub>   | 17  |      | 18  |      | 20  |      | ns    |           |

## NOTES

1. An initial pause of 200 $\mu$ s is required after power-up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2.  $V_{IH}(\min)$  and  $V_{IL}(\max)$  are reference levels for measuring timing of input signals. Transition times are measured between  $V_{IH}(\min)$  and  $V_{IL}(\max)$  and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 1 TTL load and 100pF.
4. Operation within the  $t_{RCD}(\max)$  limit insures that  $t_{RAC}(\max)$  can be met.  $t_{RCD}(\max)$  is specified as a reference point only. If  $t_{RCD}$  is greater than the specified  $t_{RCD}(\max)$  limit, then access time is controlled exclusively by  $t_{CAC}$ .
5. Assumes that  $t_{RCD} \geq t_{RCD}(\max)$ .
6.  $t_{OFF}(\min)$  and  $t_{OEZ}(\max)$  define the time at which the output achieves the open circuit condition and are not referenced  $V_{OH}$  or  $V_{OL}$ .
7.  $t_{WCS}$ ,  $t_{RWD}$ ,  $t_{CWD}$  and  $t_{AWD}$  are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If  $t_{WCS} \geq t_{WCS}(\min)$ , the cycles is an early write cycle and the data output will remain high impedance for the duration of the cycle. If  $t_{CWD} \geq t_{CWD}(\min)$ ,  $t_{RWD} \geq t_{RWD}(\min)$  and  $t_{AWD} \geq t_{AWD}(\min)$ , then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a read cycle.
9. This parameters are referenced to the  $\overline{CAS}$  falling edge in early write cycles and to the  $\overline{W}$  falling edge in read-modify-write cycles.
10. Operation within the  $t_{RAD}(\max)$  limit insures that  $t_{RAC}(\max)$  can be met.  $t_{RAD}(\max)$  is specified as a reference point only. If  $t_{RAD}$  is greater than the specified  $t_{RAD}(\max)$  limit, then access time is controlled by  $t_{AA}$ .
11. These specifications are applied in the test mode.
12. In test mode read cycle, the value of  $t_{RAC}$ ,  $t_{AA}$ ,  $t_{CAC}$  is delayed by 2ns to 5ns for the specified values. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
13. If  $t_{RASS} \geq 100\mu s$ , then  $\overline{RAS}$  precharge time must use  $t_{RPS}$  instead of  $t_{RP}$ .
14. For  $\overline{RAS}$ -only-Refresh and Burst  $\overline{CAS}$ -before- $\overline{RAS}$  refresh mode, 4096 cycles(4K/8K) of burst refresh must be executed within 64ms before and after self refresh, in order to meet refresh specification.
15. For distributed  $\overline{CAS}$ -before- $\overline{RAS}$  with 15.6 $\mu s$  interval, CBR refresh should be executed with in 15.6 $\mu s$  immediately before and after self refresh in order to meet refresh specification.

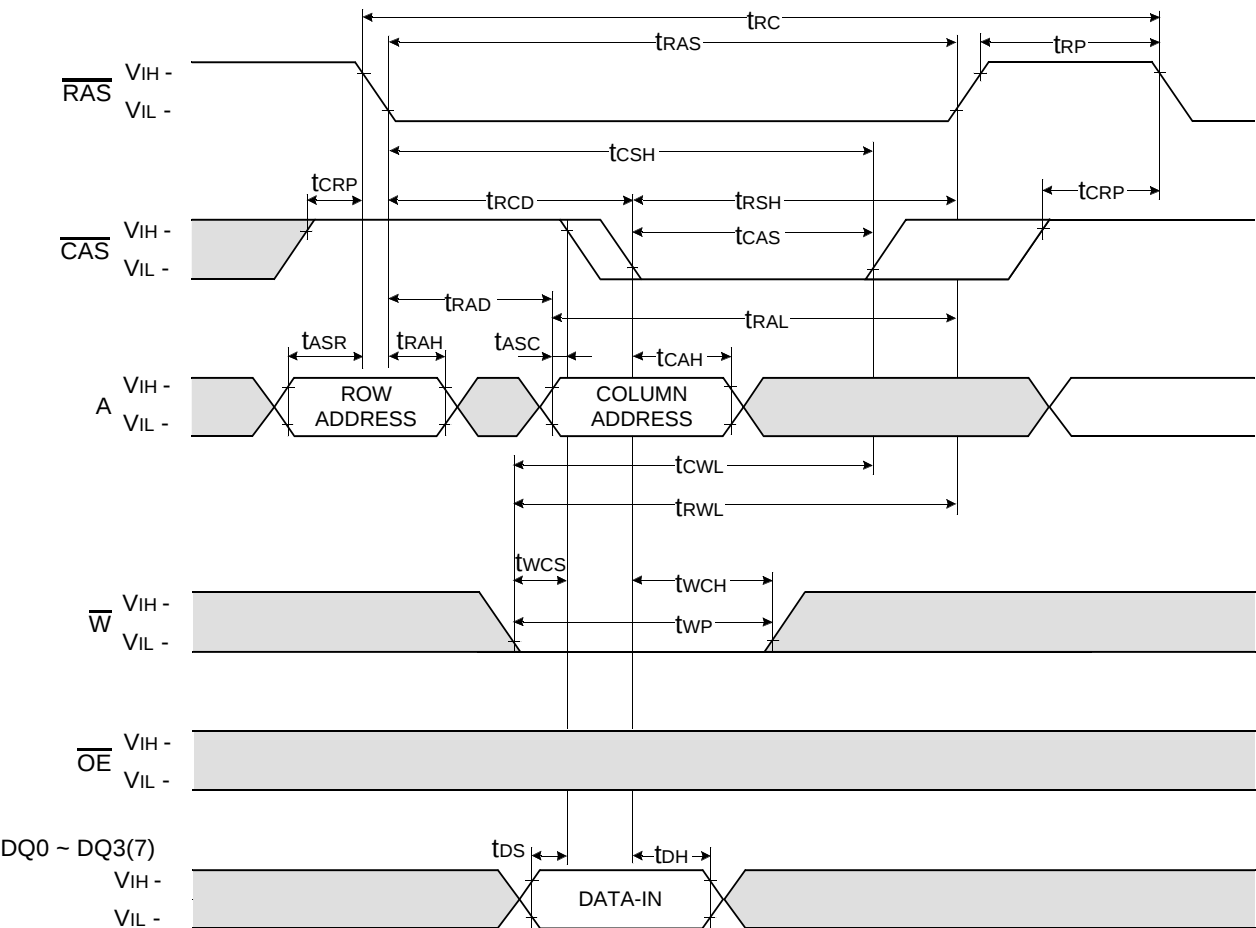
READ CYCLE



Don't care  
Undefined

WRITE CYCLE ( EARLY WRITE )

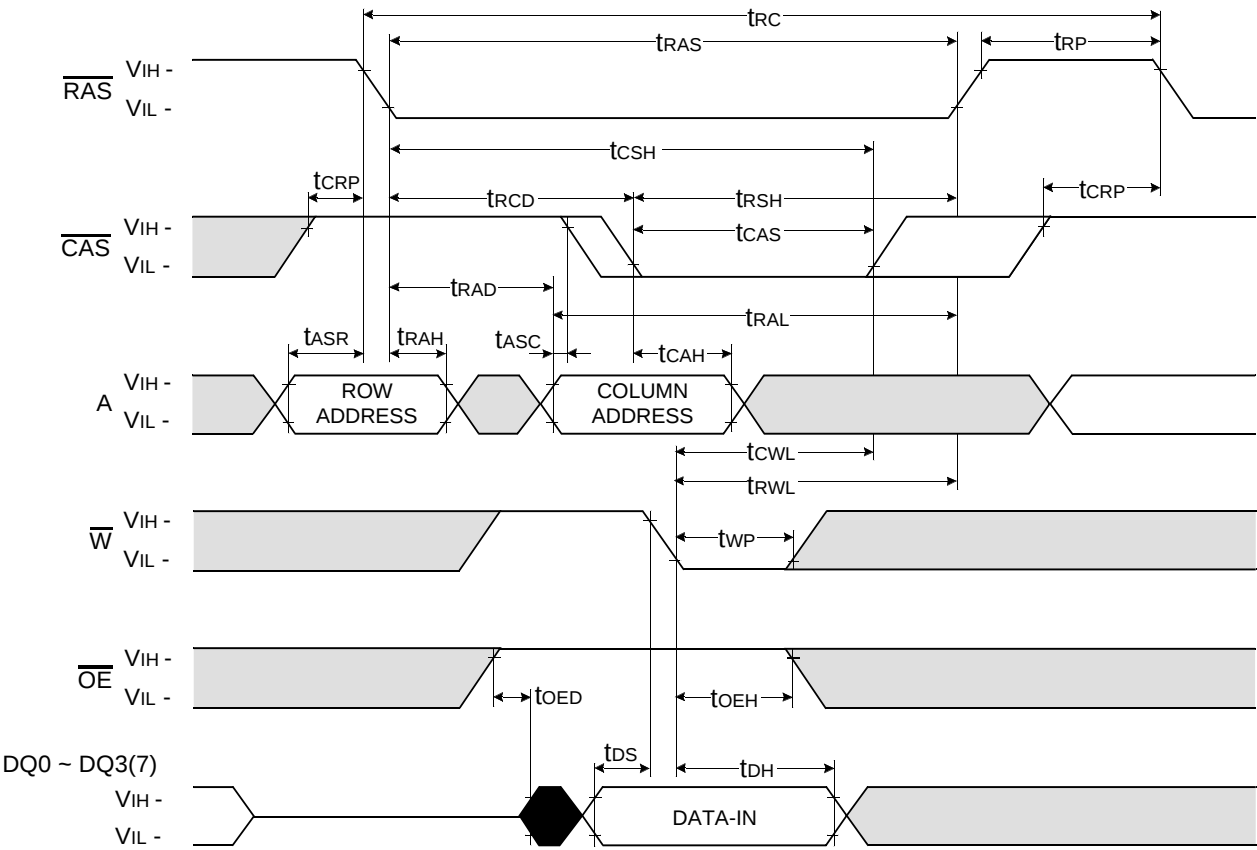
NOTE : DOUT = OPEN



Don't care  
Undefined

WRITE CYCLE (  $\overline{OE}$  CONTROLLED WRITE )

NOTE : DOUT = OPEN



The timing diagram illustrates the relationship between the RAS, CAS, Address (A), Write Enable ( $\overline{W}$ ), Output Enable ( $\overline{OE}$ ), and Data Bus (DQ0 ~ DQ3(7)) signals. Key timing parameters are defined as follows:

- RAS:**  $t_{RAS}$  (RAS to output delay),  $t_{RWC}$  (RAS to output delay),  $t_{RP}$  (RAS pulse width).
- CAS:**  $t_{CRP}$  (CAS to output delay),  $t_{RCD}$  (RAS to CAS delay),  $t_{RSH}$  (RAS to output delay),  $t_{CAS}$  (CAS to output delay),  $t_{RAD}$  (RAS to output delay),  $t_{ASC}$  (RAS to output delay),  $t_{CAH}$  (RAS to output delay),  $t_{CSH}$  (RAS to output delay).
- Address (A):**  $t_{ASR}$  (Address to output delay),  $t_{RAH}$  (Address to output delay),  $t_{ASC}$  (Address to output delay),  $t_{CAH}$  (Address to output delay),  $t_{CSH}$  (Address to output delay).
- Write Enable ( $\overline{W}$ ):**  $t_{AWD}$  (Write Enable to output delay),  $t_{CWD}$  (Write Enable to output delay),  $t_{RWD}$  (Write Enable to output delay),  $t_{WP}$  (Write Enable pulse width).
- Output Enable ( $\overline{OE}$ ):**  $t_{OEA}$  (Output Enable to output delay),  $t_{CLZ}$  (Output Enable to output delay),  $t_{CAC}$  (Output Enable to output delay),  $t_{AA}$  (Output Enable to output delay),  $t_{RAC}$  (Output Enable to output delay),  $t_{OEZ}$  (Output Enable to output delay),  $t_{DS}$  (Output Enable to output delay),  $t_{DH}$  (Output Enable to output delay).
- Data Bus (DQ0 ~ DQ3(7)):**  $t_{VIOH}$  (Data bus to output delay),  $t_{VLOL}$  (Data bus to output delay),  $t_{VIOH}$  (Data bus to output delay),  $t_{VLOL}$  (Data bus to output delay).

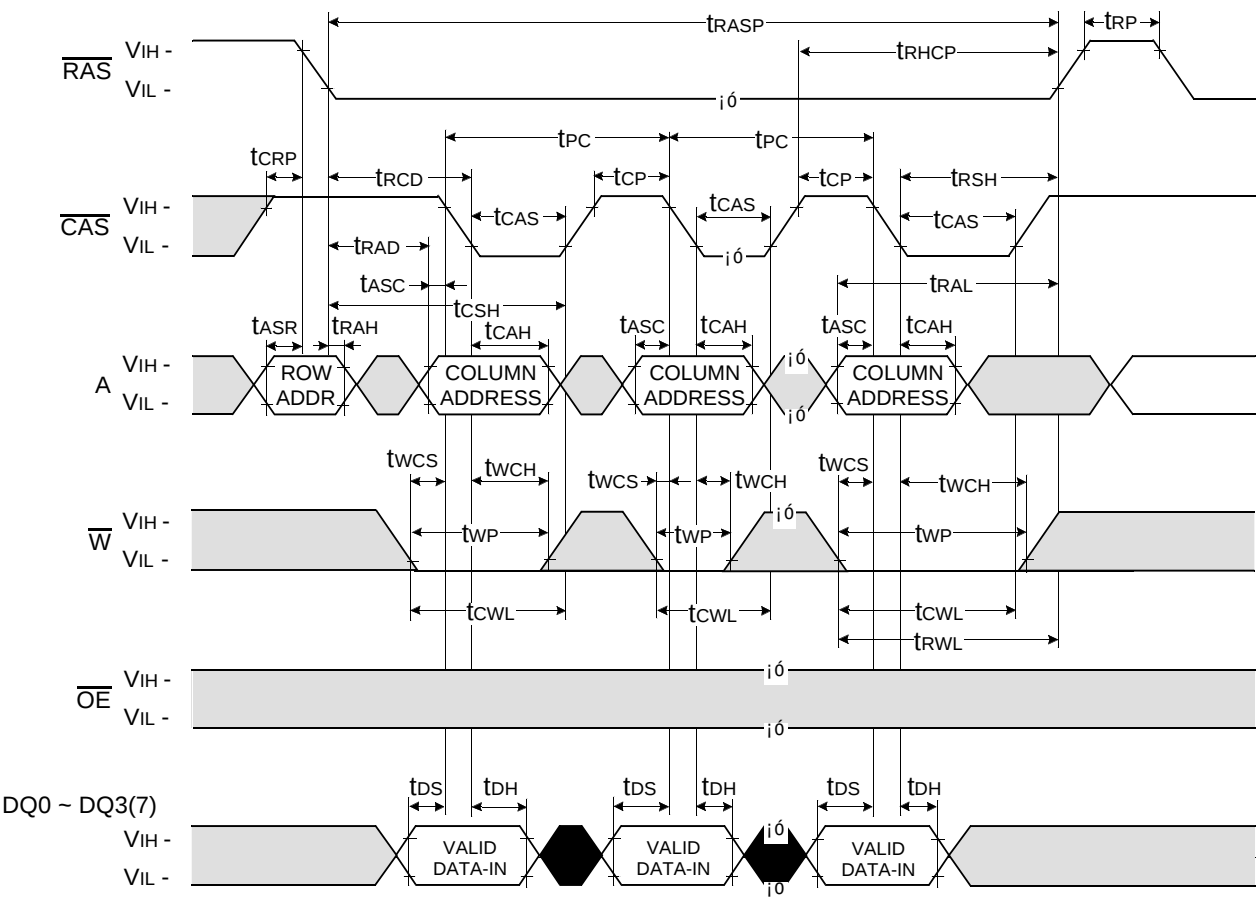
Undefined

[illegible]

Undefined

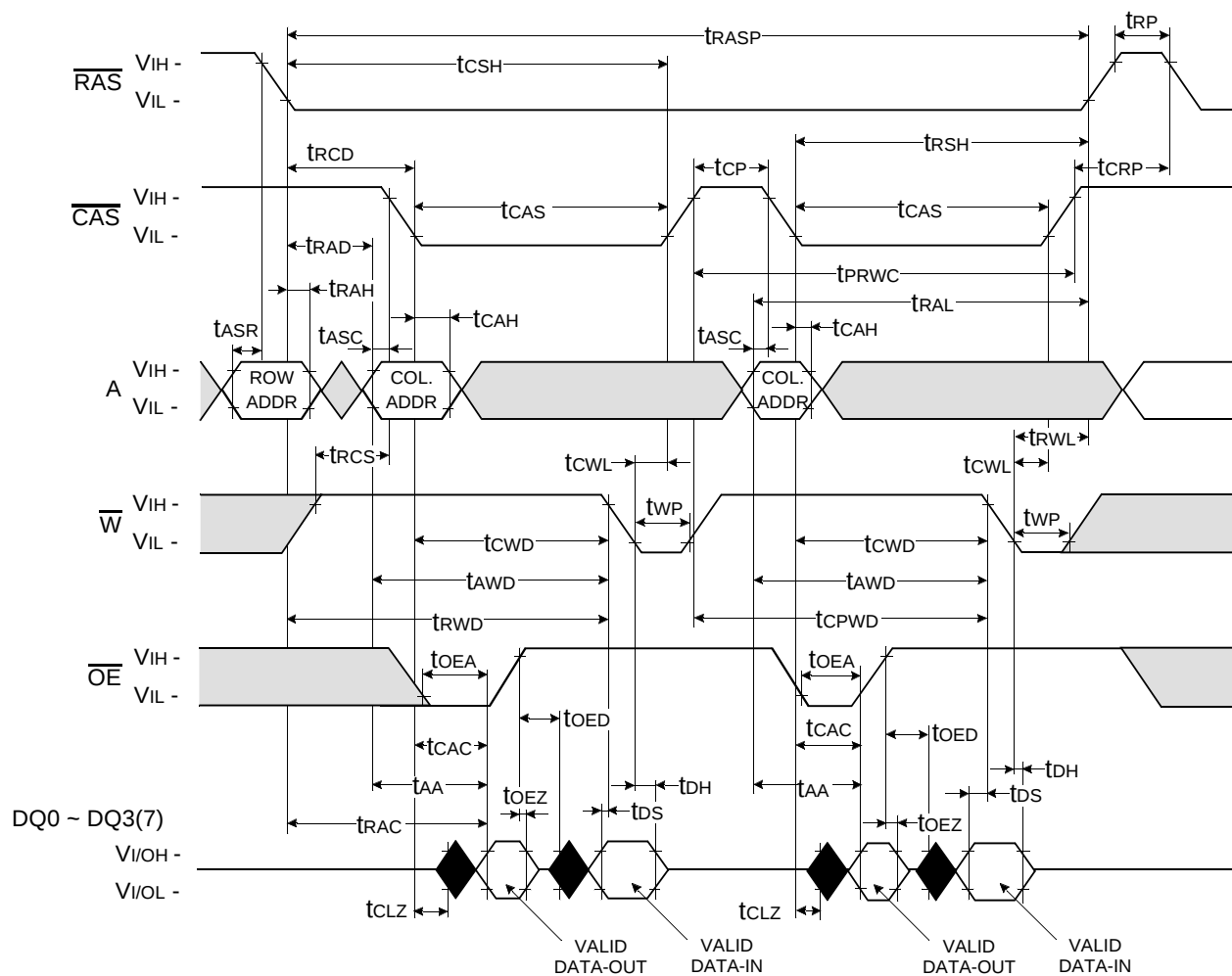
FAST PAGE WRITE CYCLE ( EARLY WRITE )

NOTE : DOUT = OPEN



Don't care  
Undefined

## FAST PAGE READ - MODIFY - WRITE CYCLE



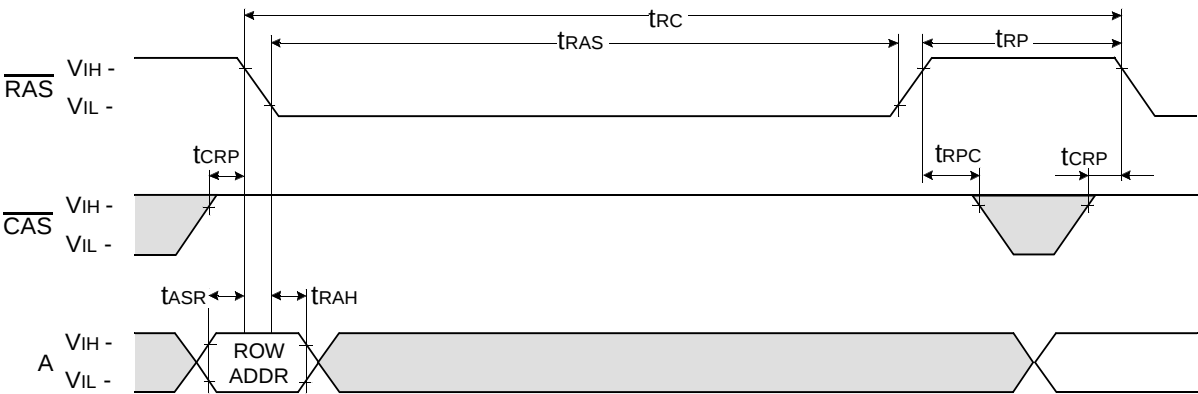
 Don't care

 Undefined

**RAS - ONLY REFRESH CYCLE**

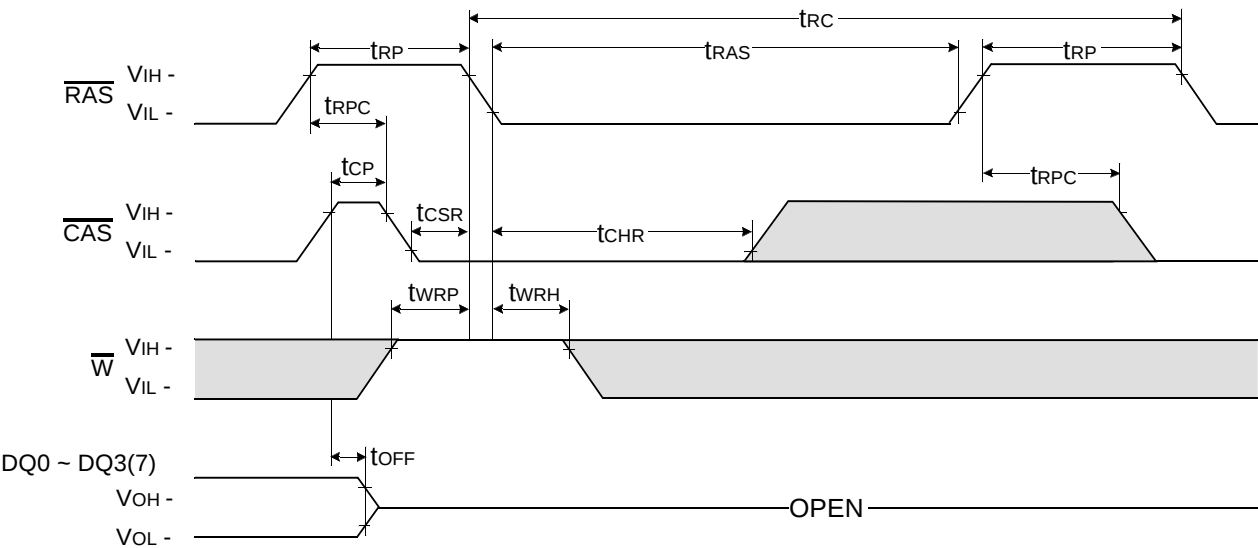
NOTE :  $\overline{W}$ ,  $\overline{OE}$ , DIN = Don't care

DOUT = OPEN



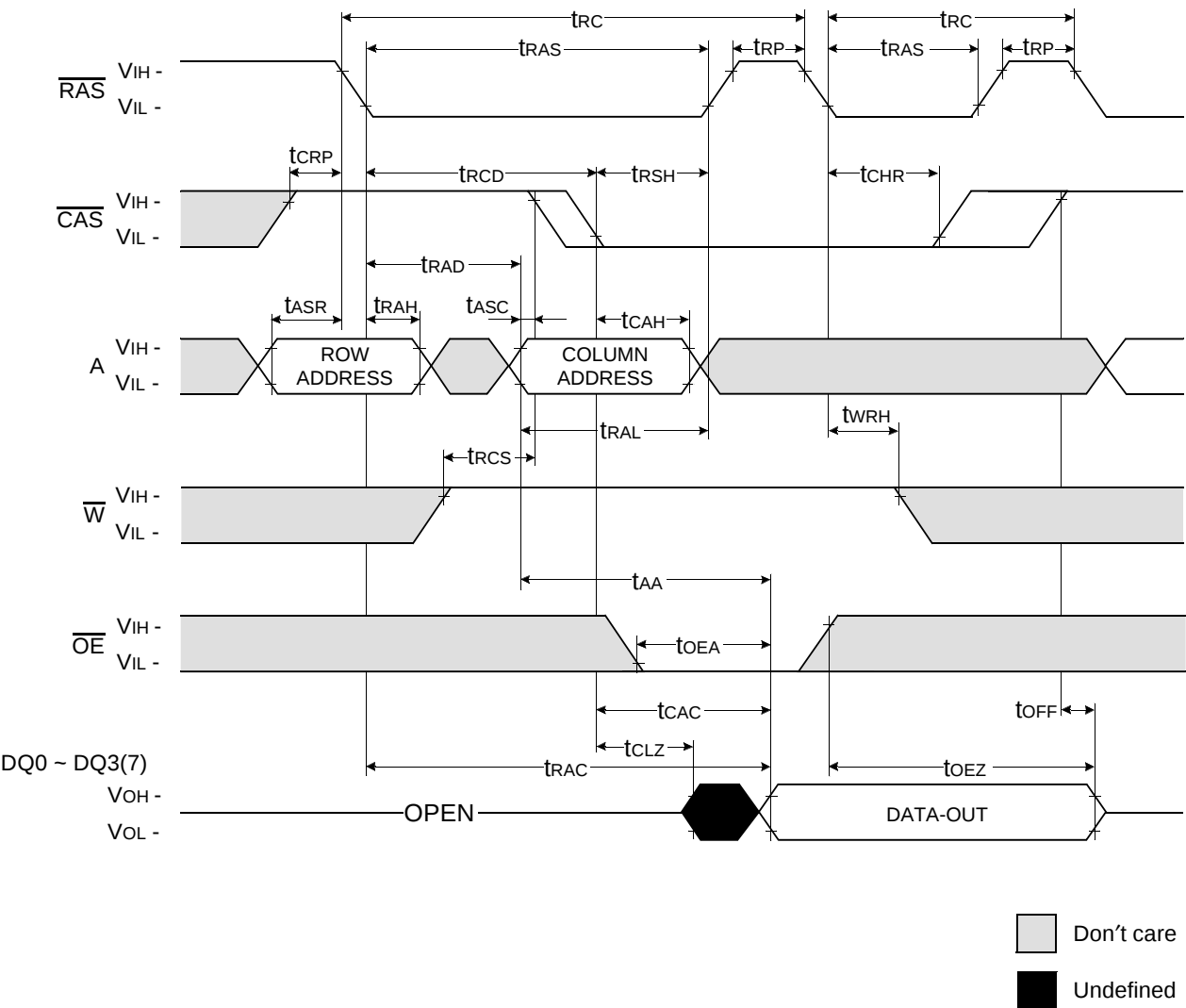
**CAS - BEFORE - RAS REFRESH CYCLE**

NOTE :  $\overline{OE}$ ,  $A$  = Don't care



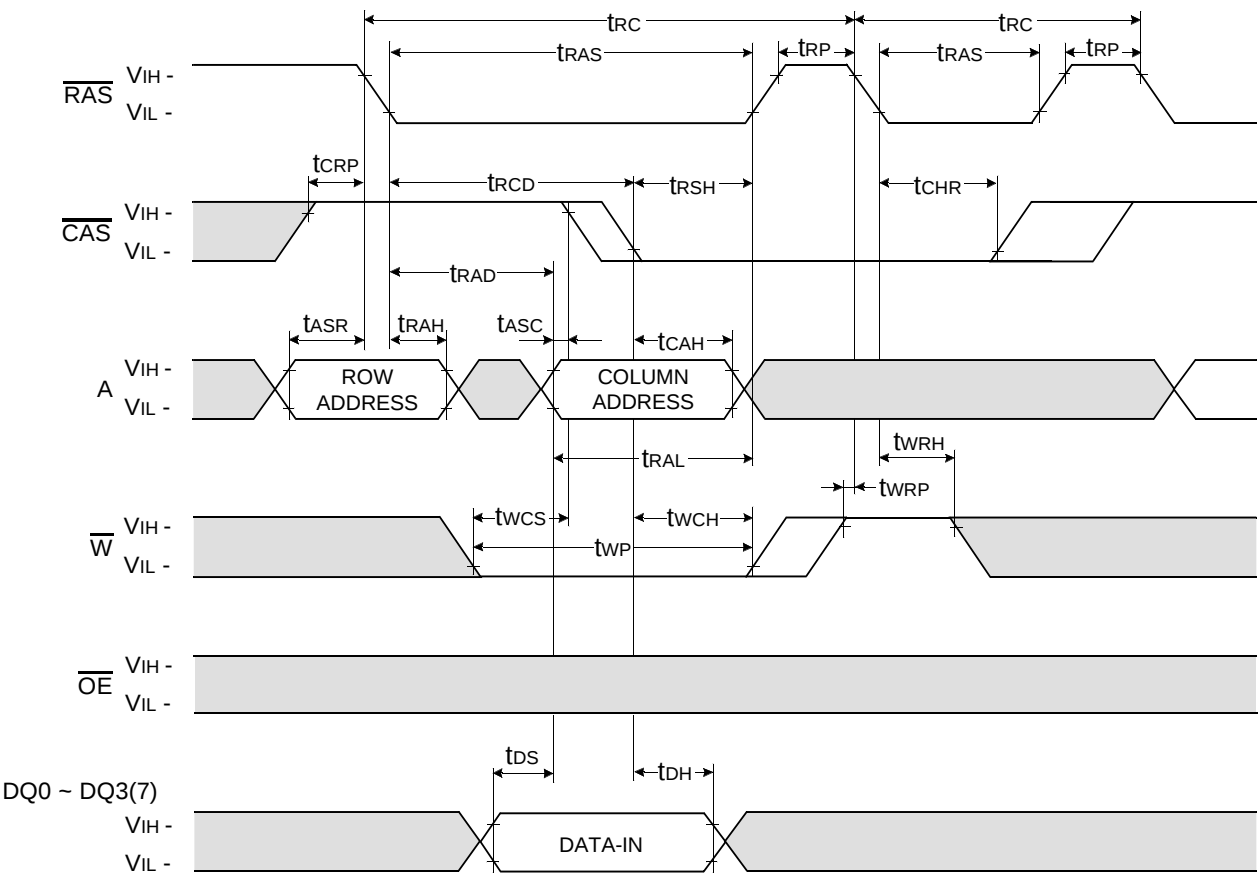
Don't care  
Undefined

HIDDEN REFRESH CYCLE ( READ )



HIDDEN REFRESH CYCLE ( WRITE )

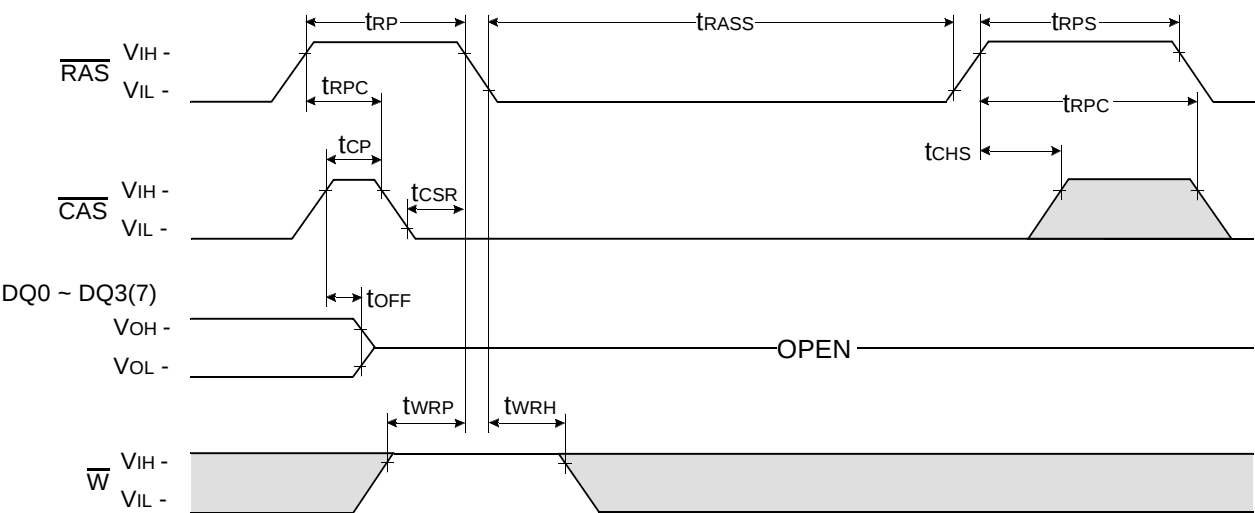
NOTE : DOUT = OPEN



Don't care  
Undefined

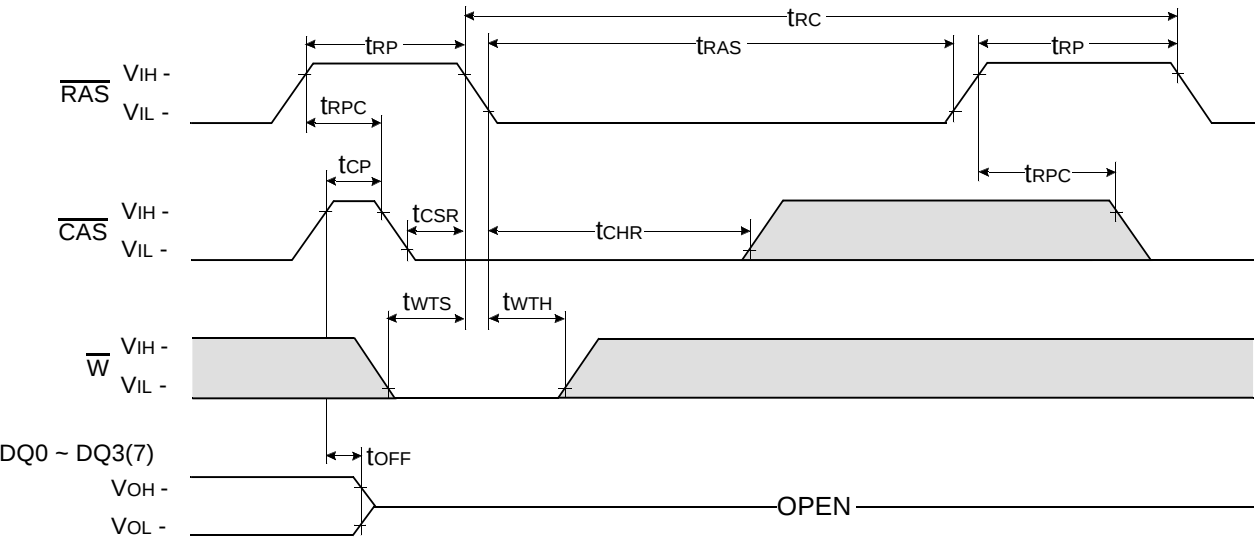
CAS - BEFORE - RAS SELF REFRESH CYCLE

NOTE : OE, A = Don't care



TEST MODE IN CYCLE

NOTE : OE, A = Don't care



Don't care  
Undefined

PACKAGE DIMENSION

