

*16M x 4bit CMOS Dynamic RAM with Fast Page Mode***DESCRIPTION**

This is a family of 16,777,216 x 4 bit Fast Page Mode CMOS DRAMs. Fast Page Mode offers high speed random access of memory cells within the same row. Refresh cycle(4K Ref. or 8K Ref.), access time (-45, -50 or -60), power consumption(Normal or Low power) are optional features of this family. All of this family have $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ -only refresh and Hidden refresh capabilities. Furthermore, Self-refresh operation is available in L-version. This 16Mx4 Fast Page Mode DRAM family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability.

FEATURES• **Part Identification**

- K4F660412B-JC/L(3.3V, 8K Ref., SOJ)
- K4F640412B-JC/L(3.3V, 4K Ref., SOJ)
- K4F660412B-TC/L(3.3V, 8K Ref., TSOP)
- K4F640412B-TC/L(3.3V, 4K Ref., TSOP)

• **Active Power Dissipation**

Unit : mW

Speed	8K	4K
-45	360	468
-50	324	432
-60	288	396

• **Refresh Cycles**

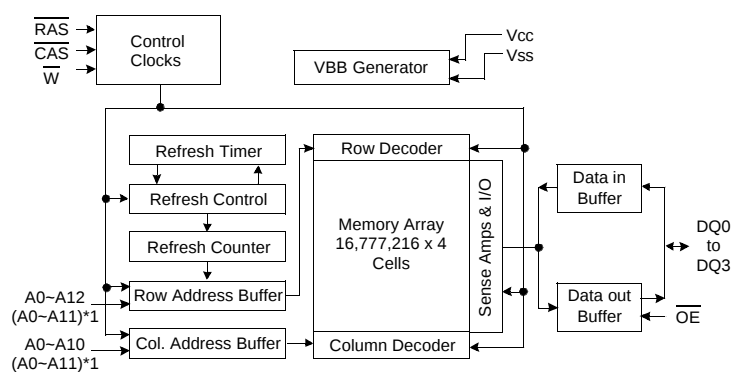
Part NO.	Refresh cycle	Refresh time	
		Normal	L-ver
K4F660412B*	8K	64ms	128ms
K4F640412B	4K		

* Access mode & $\overline{\text{RAS}}$ only refresh mode
 : 8K cycle/64ms(Normal), 8K cycle/128ms(L-ver.)
 $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ & Hidden refresh mode
 : 4K cycle/64ms(Normal), 4K cycle/128ms(L-ver.)

• **Performance Range**

Speed	t _{TRC}	t _{CAC}	t _{RC}	t _{PC}
-45	45ns	12ns	80ns	31ns
-50	50ns	13ns	90ns	35ns
-60	60ns	15ns	110ns	40ns

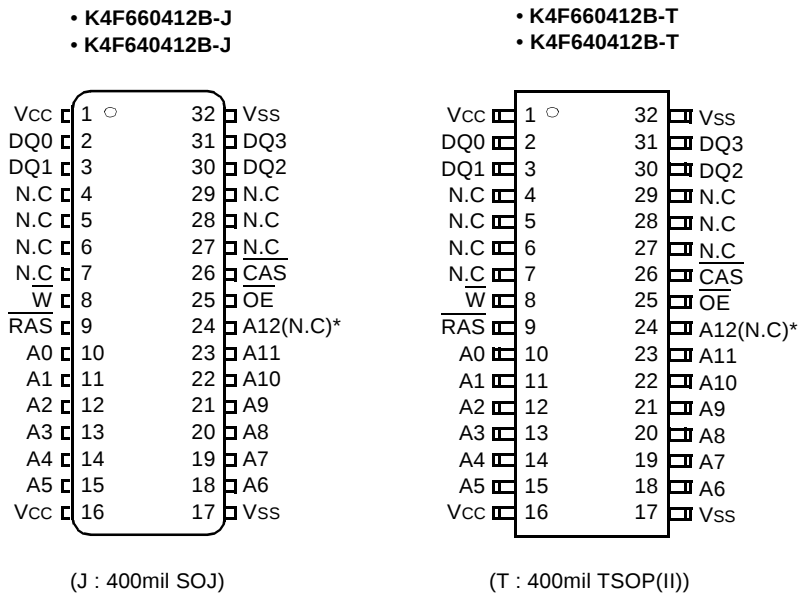
- Fast Page Mode operation
- $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh capability
- $\overline{\text{RAS}}$ -only and Hidden refresh capability
- Self-refresh capability (L-ver only)
- Fast parallel test mode capability
- LVTTTL(3.3V) compatible inputs and outputs
- Early Write or output enable controlled write
- JEDEC Standard pinout
- Available in Plastic SOJ and TSOP(II) packages
- +3.3V±0.3V power supply

FUNCTIONAL BLOCK DIAGRAM

Note) *1 : 4K Refresh

SAMSUNG ELECTRONICS CO., LTD. reserves the right to change products and specifications without notice.

PIN CONFIGURATION (Top Views)



* (N.C) : N.C for 4K Refresh product

Pin Name	Pin Function
A0 - A12	Address Inputs(8K Product)
A0 - A11	Address Inputs(4K Product)
DQ0 - 3	Data In/Out
Vss	Ground
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS}}$	Column Address Strobe
$\overline{\text{W}}$	Read/Write Input
$\overline{\text{OE}}$	Data Output Enable
Vcc	Power(+3.3V)
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-0.5 to +6.5	V
Voltage on Vcc supply relative to Vss	Vcc	-0.5 to +4.6	V
Storage Temperature	Tstg	-55 to +150	°C
Power Dissipation	P _D	1	W
Short Circuit Output Current	I _{os} Address	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, TA= 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Units
Supply Voltage	Vcc	3.0	3.3	3.6	V
Ground	Vss	0	0	0	V
Input High Voltage	V _{IH}	2.0	-	+5.5 ^{*1}	V
Input Low Voltage	V _{IL}	-0.3 ^{*2}	-	0.8	V

*1 : 6.5V at pulse width ≤ 15ns which is measured at Vcc

*2 : -1.3 at pulse width ≤ 15ns which is measured at Vss

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Units
Input Leakage Current (Any input 0 ≤ V _{IN} ≤ Vcc + 0.3V, all other pins not under test = 0 Volt)	I _{I(L)}	-5	5	μA
Output Leakage Current (Data out is disabled, 0V ≤ V _{OUT} ≤ Vcc)	I _{O(L)}	-5	5	μA
Output High Voltage Level (I _{OH} = -2mA)	V _{OH}	2.4	-	V
Output Low Voltage Level (I _{OL} = 2mA)	V _{OL}	-	0.4	V

DC AND OPERATING CHARACTERISTICS (Continued)

Symbol	Power	Speed	Max		Units
			K4F660412B	K4F640412B	
Icc1	Don't care	-45	100	130	mA
		-50	90	120	mA
		-60	80	110	mA
Icc2	Normal L	Don't care	2	2	mA
			2	2	mA
Icc3	Don't care	-45	100	130	mA
		-50	90	120	mA
		-60	80	110	mA
Icc4	Don't care	-45	70	80	mA
		-50	60	70	mA
		-60	50	60	mA
Icc5	Normal L	Don't care	500	500	uA
			300	300	uA
Icc6	Don't care	-45	100	130	mA
		-50	90	120	mA
		-60	80	110	mA
Icc7	L	Don't care	400	400	uA
Iccs	L	Don't care	400	400	uA

Icc1* : Operating Current ($\overline{\text{RAS}}$ and $\overline{\text{CAS}}$, Address cycling @trc=min.)

Icc2 : Standby Current ($\overline{\text{RAS}}=\overline{\text{CAS}}=\overline{\text{W}}=\text{V}_{\text{IH}}$)

Icc3* : RAS-only Refresh Current ($\overline{\text{CAS}}=\text{V}_{\text{IH}}$, $\overline{\text{RAS}}$, Address cycling @trc=min.)

Icc4* : Fast Page Mode Current ($\overline{\text{RAS}}=\text{V}_{\text{IL}}$, $\overline{\text{CAS}}$, Address cycling @tpc=min.)

Icc5 : Standby Current ($\overline{\text{RAS}}=\overline{\text{CAS}}=\overline{\text{W}}=\text{V}_{\text{CC}}-0.2\text{V}$)

Icc6* : CAS-Before-RAS Refresh Current ($\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ cycling @trc=min)

Icc7 : Battery back-up current, Average power supply current, Battery back-up mode

Input high voltage(V_{IH})= $\text{V}_{\text{CC}}-0.2\text{V}$, Input low voltage(V_{IL})= 0.2V , $\overline{\text{CAS}}=\overline{\text{CAS}}$ -before-RAS cycling or 0.2V ,
 $\overline{\text{W}}$, $\overline{\text{OE}}=\text{V}_{\text{IH}}$, Address=Don't care DQ=Open, Trc=31.25us

Iccs : Self Refresh Current

$\overline{\text{RAS}}=\overline{\text{CAS}}=0.2\text{V}$, $\overline{\text{W}}=\overline{\text{OE}}=\text{A0} \sim \text{A12}(\text{A11})=\text{V}_{\text{CC}}-0.2\text{V}$ or 0.2V , DQ0 ~ DQ3= $\text{V}_{\text{CC}}-0.2\text{V}$, 0.2V or Open

***Note :** Icc1, Icc3, Icc4 and Icc6 are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In Icc1, Icc3 and Icc6, address can be changed maximum once while $\overline{\text{RAS}}=\text{V}_{\text{IL}}$. In Icc4, address can be changed maximum once within one fast page mode cycle time, tpc.

K4F660412B, K4F640412B**CMOS DRAM****CAPACITANCE** ($T_A=25^{\circ}\text{C}$, $V_{CC}=3.3\text{V}$, $f=1\text{MHz}$)

Parameter	Symbol	Min	Max	Units
Input capacitance [A0 ~ A12]	C _{IN1}	-	5	pF
Input capacitance [$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{W}}$, $\overline{\text{OE}}$]	C _{IN2}	-	7	pF
Output capacitance [DQ0 - DQ3]	C _{DQ}	-	7	pF

AC CHARACTERISTICS ($0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$, See note 1,2)Test condition : $V_{CC}=3.3\text{V} \pm 0.3\text{V}$, $V_{IH}/V_{IL}=2.2/0.7\text{V}$, $V_{OH}/V_{OL}=2.0/0.8\text{V}$

Parameter	Symbol	-45		-50		-60		Units	Note
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t _{RC}	80		90		110		ns	
Read-modify-write cycle time	t _{RWC}	115		133		153		ns	
Access time from $\overline{\text{RAS}}$	t _{RAC}		45		50		60	ns	3,4,10
Access time from $\overline{\text{CAS}}$	t _{CAC}		12		13		15	ns	3,4,5
Access time from column address	t _{AA}		23		25		30	ns	3,10
$\overline{\text{CAS}}$ to output in Low-Z	t _{CLZ}	0		0		0		ns	3
Output buffer turn-off delay	t _{OFF}	0	13	0	13	0	13	ns	6
Transition time (rise and fall)	t _T	1	50	1	50	1	50	ns	2
$\overline{\text{RAS}}$ precharge time	t _{RP}	25		30		40		ns	
$\overline{\text{RAS}}$ pulse width	t _{RAS}	45	10K	50	10K	60	10K	ns	
$\overline{\text{RAS}}$ hold time	t _{RSH}	12		13		15		ns	
$\overline{\text{CAS}}$ hold time	t _{CSH}	45		50		60		ns	
$\overline{\text{CAS}}$ pulse width	t _{CAS}	12	10K	13	10K	15	10K	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	t _{RCD}	18	33	20	37	20	45	ns	4
$\overline{\text{RAS}}$ to column address delay time	t _{RAD}	13	22	15	25	15	30	ns	10
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	t _{CRP}	5		5		5		ns	
Row address set-up time	t _{ASR}	0		0		0		ns	
Row address hold time	t _{RAH}	8		10		10		ns	
Column address set-up time	t _{ASC}	0		0		0		ns	
Column address hold time	t _{CAH}	8		10		10		ns	
Column address to $\overline{\text{RAS}}$ lead time	t _{RAL}	23		25		30		ns	
Read command set-up time	t _{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{\text{CAS}}$	t _{RCH}	0		0		0		ns	8
Read command hold time referenced to $\overline{\text{RAS}}$	t _{RRH}	0		0		0		ns	8
Write command hold time	t _{WCH}	8		10		10		ns	
Write command pulse width	t _{WP}	8		10		10		ns	
Write command to $\overline{\text{RAS}}$ lead time	t _{RWL}	13		15		15		ns	
Write command to $\overline{\text{CAS}}$ lead time	t _{CWL}	12		13		15		ns	
Data set-up time	t _{DS}	0		0		0		ns	9
Data hold time	t _{DH}	10		10		10		ns	9

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-45		-50		-60		Units	Note
		Min	Max	Min	Max	Min	Max		
Refresh period (Normal)	tREF		64		64		64	ms	
Refresh period (L-ver)	tREF		128		128		128	ms	
Write command set-up time	tWCS	0		0		0		ns	7
CAS to $\overline{W}$ delay time	tCWD	32		36		38		ns	7
RAS to $\overline{W}$ delay time	tRWD	67		73		83		ns	7
Column address to $\overline{W}$ delay time	tAWD	43		48		53		ns	7
CAS precharge $\overline{W}$ delay time	tCPWD	48		53		60		ns	
CAS set-up time ($\overline{CAS}$ -before- $\overline{RAS}$ refresh)	tCSR	5		5		5		ns	
CAS hold time ($\overline{CAS}$ -before- $\overline{RAS}$ refresh)	tCHR	10		10		10		ns	
RAS to CAS precharge time	tRPC	5		5		5		ns	
Access time from $\overline{CAS}$ precharge	tCPA		26		30		35	ns	3
Fast Page mode cycle time	tPC	31		35		40		ns	
Fast Page mode read-modify-write cycle time	tPRWC	70		76		85		ns	
CAS precharge time (Fast page cycle)	tCP	9		10		10		ns	
RAS pulse width (Fast page cycle)	tRASP	45	200K	50	200K	60	200K	ns	
RAS hold time from CAS precharge	tRHCP	28		30		35		ns	
$\overline{OE}$ access time	tOEA		12		13		15	ns	
$\overline{OE}$ to data delay	tOED	12		13		13		ns	
Output buffer turn off delay time from $\overline{OE}$	tOEZ	0	13	0	13	0	13	ns	6
$\overline{OE}$ command hold time	tOEH	12		13		15		ns	
Write command set-up time (Test mode in)	tWTS	10		10		10		ns	11
Write command hold time (Test mode in)	tWTH	15		15		15		ns	11
$\overline{W}$ to RAS precharge time ($\overline{C}$ -B- $\overline{R}$ refresh)	tWRP	10		10		10		ns	
$\overline{W}$ to RAS hold time ($\overline{C}$ -B- $\overline{R}$ refresh)	tWRH	10		10		10		ns	
RAS pulse width ($\overline{C}$ -B- $\overline{R}$ self refresh)	tRASS	100		100		100		us	13,14,15
RAS precharge time ($\overline{C}$ -B- $\overline{R}$ self refresh)	tRPS	80		90		110		ns	13,14,15
CAS hold time ($\overline{C}$ -B- $\overline{R}$ self refresh)	tCHS	-50		-50		-50		ns	13,14,15

TEST MODE CYCLE

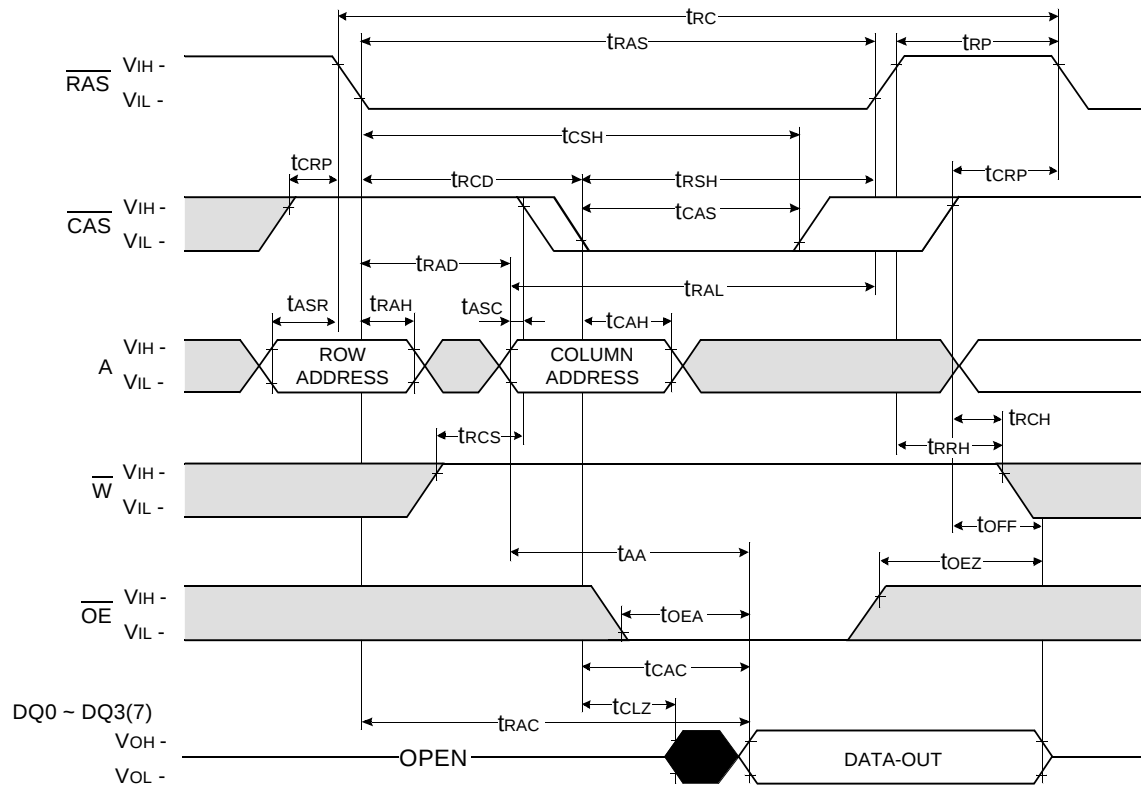
(Note 11)

Parameter	Symbol	-45		-50		-60		Units	Note
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t _{RC}	85		95		115		ns	
Read-modify-write cycle time	t _{RWC}	120		138		160		ns	
Access time from $\overline{\text{RAS}}$	t _{RAC}		50		55		65	ns	3,4,10,12
Access time from $\overline{\text{CAS}}$	t _{CAC}		17		18		20	ns	3,4,5,12
Access time from column address	t _{AA}		28		30		35	ns	3,10,12
$\overline{\text{RAS}}$ pulse width	t _{RAS}	50	10K	55	10K	65	10K	ns	
$\overline{\text{CAS}}$ pulse width	t _{CAS}	17	10K	18	10K	20	10K	ns	
$\overline{\text{RAS}}$ hold time	t _{RSH}	17		18		20		ns	
$\overline{\text{CAS}}$ hold time	t _{CSH}	50		55		65		ns	
Column Address to $\overline{\text{RAS}}$ lead time	t _{RAL}	28		30		35		ns	
$\overline{\text{CAS}}$ to $\overline{\text{W}}$ delay time	t _{CWD}	37		41		43		ns	7
$\overline{\text{RAS}}$ to $\overline{\text{W}}$ delay time	t _{RWD}	72		78		88		ns	7
Column Address to $\overline{\text{W}}$ delay time	t _{AWD}	48		53		58		ns	7
Fast Page mode cycle time	t _{PC}	36		40		45		ns	
Fast Page mode read-modify-write cycle time	t _{PRWC}	75		81		90		ns	
$\overline{\text{RAS}}$ pulse width (Fast Page cycle)	t _{RASP}	50	200K	55	200K	65	200K	ns	
Access time from $\overline{\text{CAS}}$ precharge	t _{CPA}		31		35		40	ns	3
$\overline{\text{OE}}$ access time	t _{OE A}		17		18		20	ns	
$\overline{\text{OE}}$ to data delay	t _{OE D}	17		18		18		ns	
$\overline{\text{OE}}$ command hold time	t _{OE H}	17		18		20		ns	

NOTES

1. An initial pause of 200 μ s is required after power-up followed by any 8 $\overline{\text{RAS}}$ -only refresh or $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycles before proper device operation is achieved.
2. $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 1 TTL load and 100pF.
4. Operation within the $t_{\text{RCD}}(\text{max})$ limit insures that $t_{\text{RAC}}(\text{max})$ can be met. $t_{\text{RCD}}(\text{max})$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{\text{RCD}}(\text{max})$ limit, then access time is controlled exclusively by t_{CAC} .
5. Assumes that $t_{\text{RCD}} \geq t_{\text{RCD}}(\text{max})$.
6. $t_{\text{OFF}}(\text{min})$ and $t_{\text{OEZ}}(\text{max})$ define the time at which the output achieves the open circuit condition and are not referenced V_{OH} or V_{OL} .
7. t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{\text{WCS}} \geq t_{\text{WCS}}(\text{min})$, the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{\text{CWD}} \geq t_{\text{CWD}}(\text{min})$, $t_{\text{RWD}} \geq t_{\text{RWD}}(\text{min})$ and $t_{\text{AWD}} \geq t_{\text{AWD}}(\text{min})$, then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9. These parameters are referenced to $\overline{\text{CAS}}$ falling edge in early write cycles and to $\overline{\text{W}}$ falling edge in read-modify-write cycles.
10. Operation within the $t_{\text{RAD}}(\text{max})$ limit insures that $t_{\text{RAC}}(\text{max})$ can be met. $t_{\text{RAD}}(\text{max})$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{\text{RAD}}(\text{max})$ limit, then access time is controlled by t_{AA} .
11. These specifications are applied in the test mode.
12. In test mode read cycle, the value of t_{RAC} , t_{AA} , t_{CAC} is delayed by 2ns to 5ns for the specified values. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
13. If $t_{\text{RAS}} \geq 100\mu\text{s}$, then $\overline{\text{RAS}}$ precharge time must use t_{RPS} instead of t_{RP} .
14. For $\overline{\text{RAS}}$ -only refresh and burst $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh mode, 4096(4K/8K) cycles of burst refresh must be executed within 64ms before and after self refresh, in order to meet refresh specification.
15. For distributed $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ with 15.6 μ s interval $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh should be executed with in 15.6 μ s immediately before and after self refresh in order to meet refresh specification.

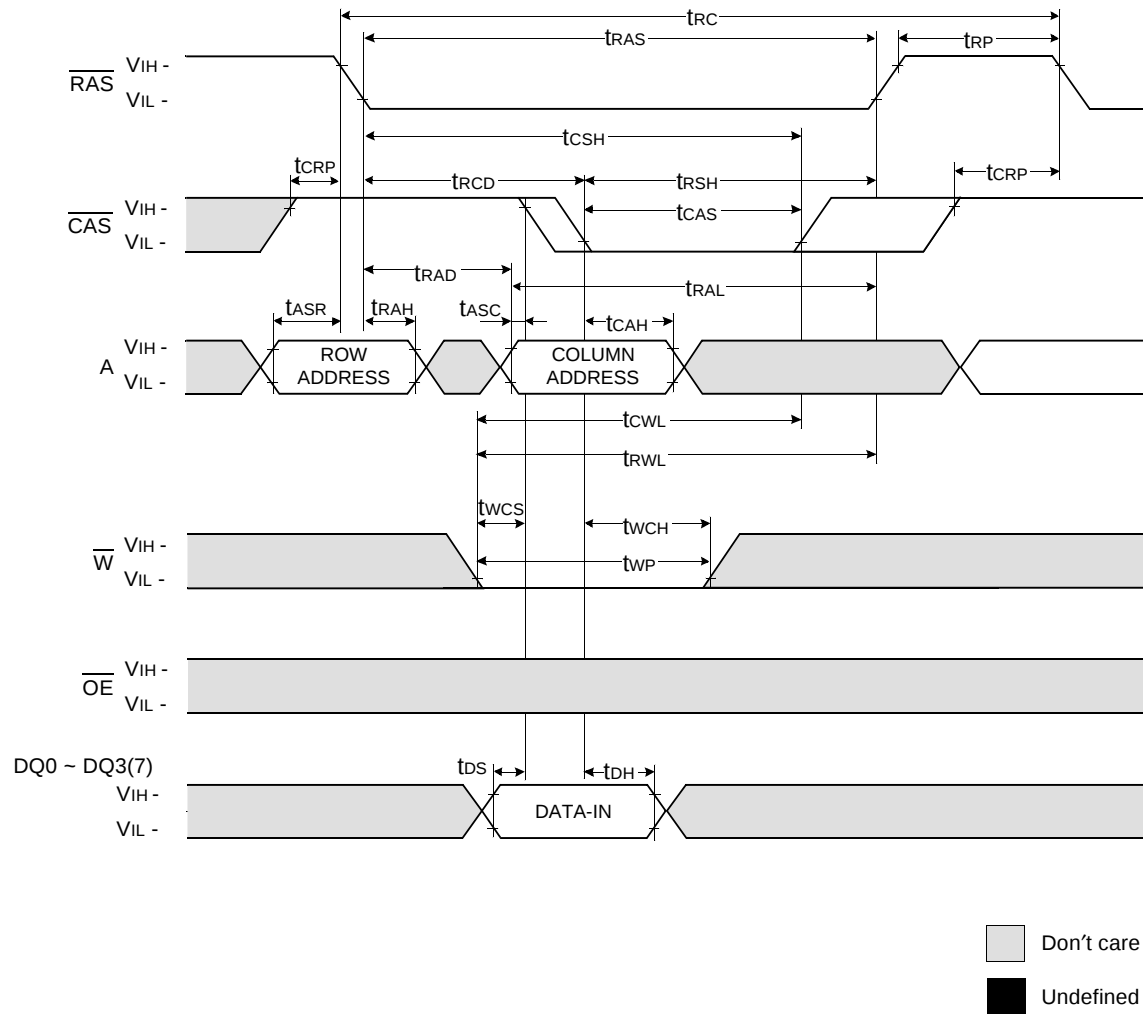
READ CYCLE



Don't care
Undefined

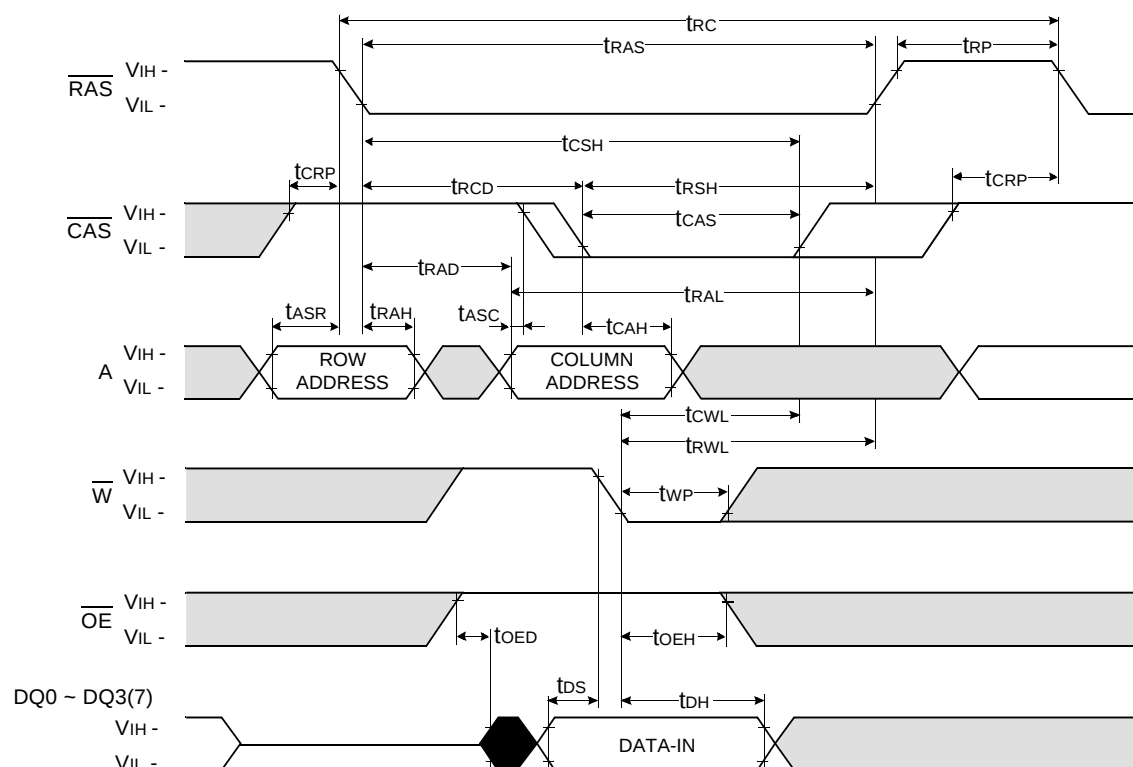
WRITE CYCLE (EARLY WRITE)

NOTE : DOUT = OPEN



WRITE CYCLE ($\overline{\text{OE}}$ CONTROLLED WRITE)

NOTE : DOUT = OPEN



The diagram illustrates the timing relationships for a memory device. The signals shown are:

- RAS**: Row Address Strobe (active low)
- CAS**: Column Address Strobe (active low)
- A**: Address bus
- W**: Write Enable (active low)
- OE**: Output Enable (active low)
- DQ0 ~ DQ3(7)**: Data bus

Key timing parameters are indicated by arrows:

- t_{CRP}**: RAS to CAS precharge time
- t_{RAS}**: RAS pulse width
- t_{TRP}**: RAS to next RAS precharge time
- t_{RCD}**: RAS to CAS delay
- t_{TRSH}**: RAS to next RAS setup time
- t_{CAS}**: CAS pulse width
- t_{RAD}**: RAS to data access time
- t_{ASR}**: Address to RAS setup time
- t_{RAH}**: Address to RAS hold time
- t_{ASC}**: Address to CAS setup time
- t_{CAH}**: Address to CAS hold time
- t_{CSH}**: CAS to next CAS setup time
- t_{AWD}**: Address to data output delay
- t_{CWD}**: CAS to data output delay
- t_{RWL}**: RAS to data output delay
- t_{CWL}**: CAS to data output delay
- t_{WP}**: Write pulse width
- t_{RWD}**: RAS to data output delay
- t_{OE}**: Output enable pulse width
- t_{CLZ}**: Output enable to data output delay
- t_{CAC}**: CAS to data output delay
- t_{AA}**: Address to data output delay
- t_{RAC}**: RAS to data output delay
- t_{OEZ}**: Output enable to data output delay
- t_{DS}**: Data output delay
- t_{DH}**: Data output delay

 Don't care

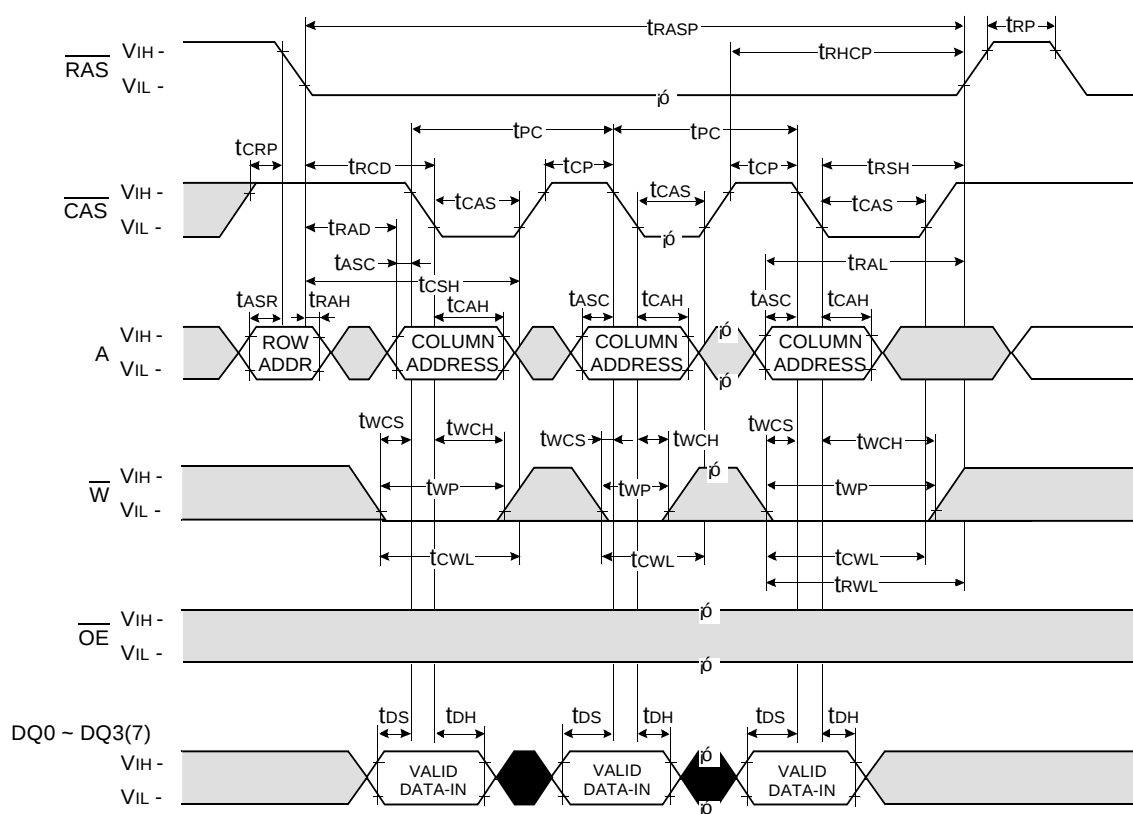
 Undefined

 Don't care

 Undefined

FAST PAGE WRITE CYCLE (EARLY WRITE)

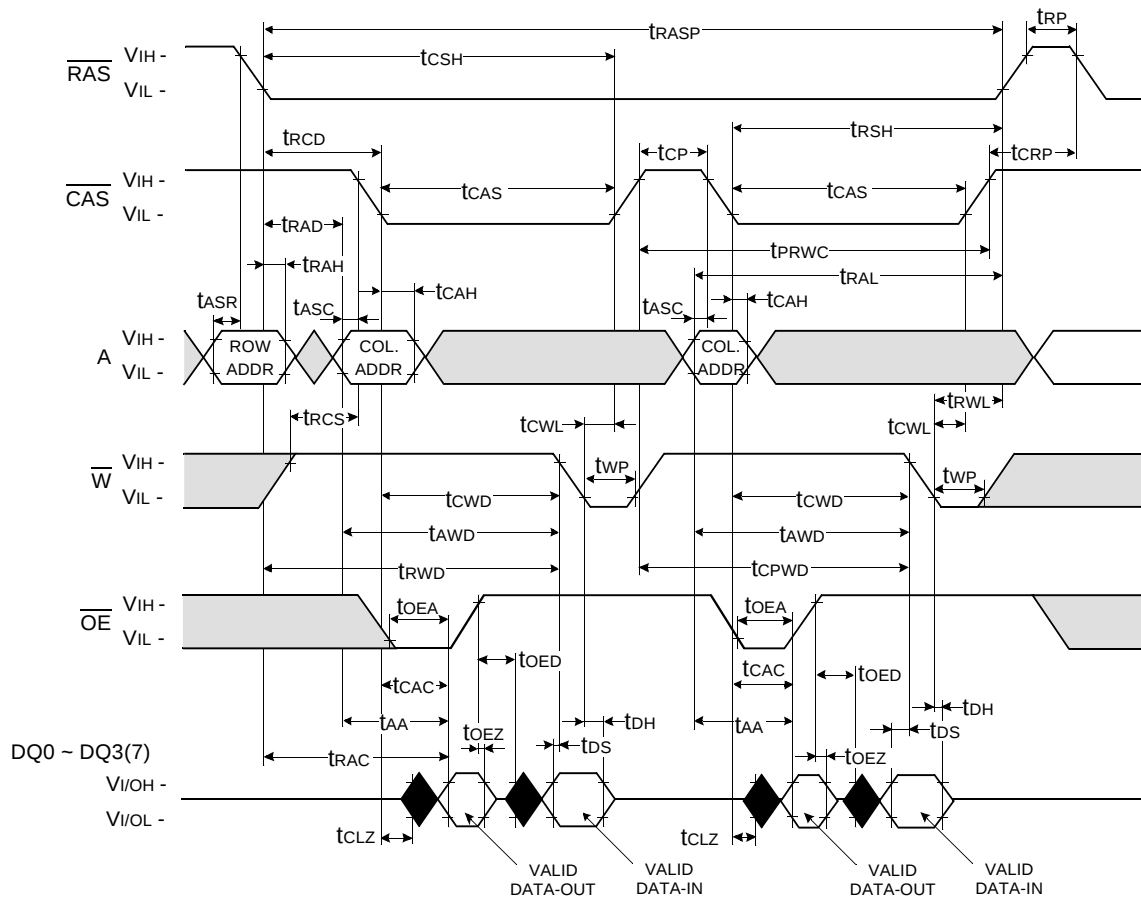
NOTE : DOUT = OPEN



Don't care

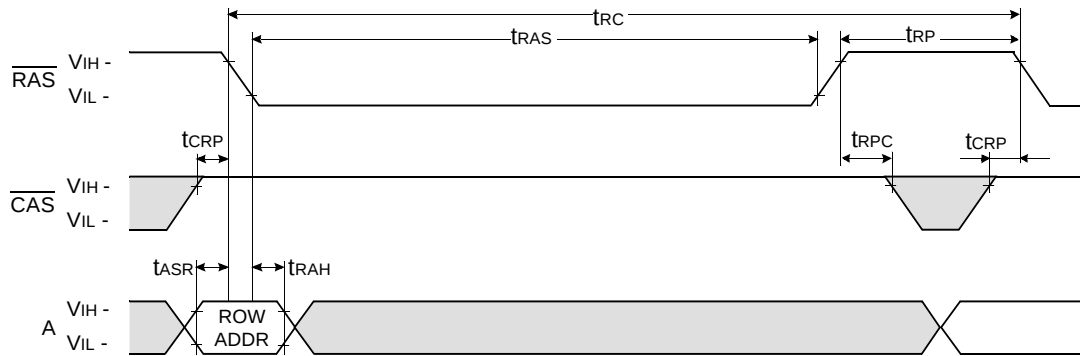
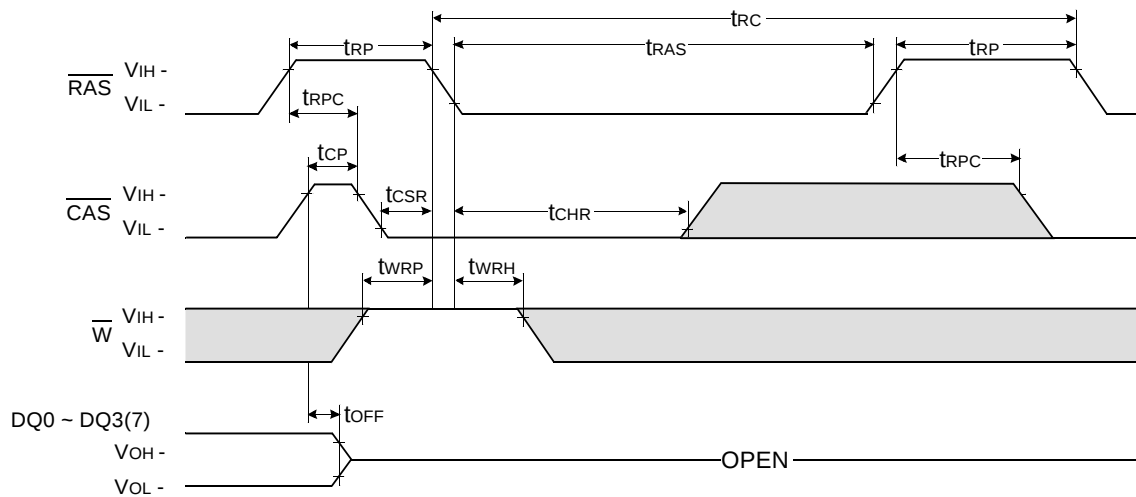
Undefined

FAST PAGE READ - MODIFY - WRITE CYCLE



RAS - ONLY REFRESH CYCLENOTE : $\overline{W}$, $\overline{OE}$, $\overline{DIN}$ = Don't care

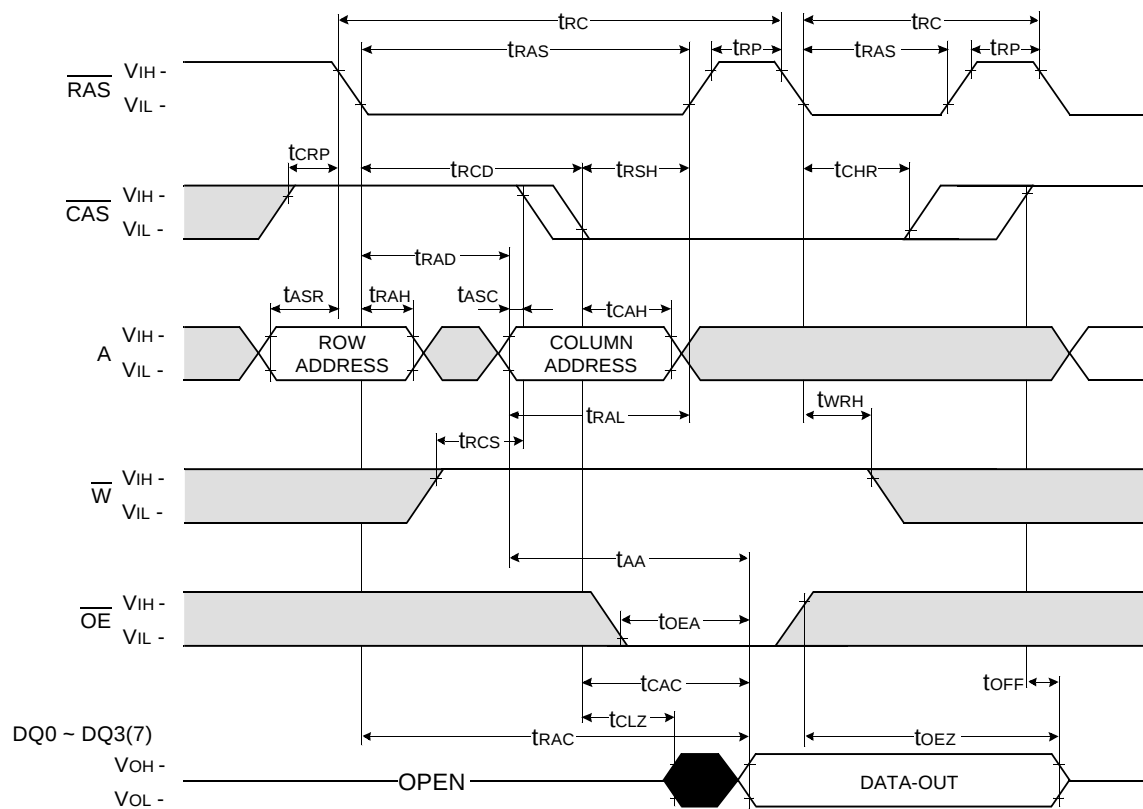
DOUT = OPEN

**CAS - BEFORE - RAS REFRESH CYCLE**NOTE : $\overline{OE}$, $\overline{A}$ = Don't care

Don't care

Undefined

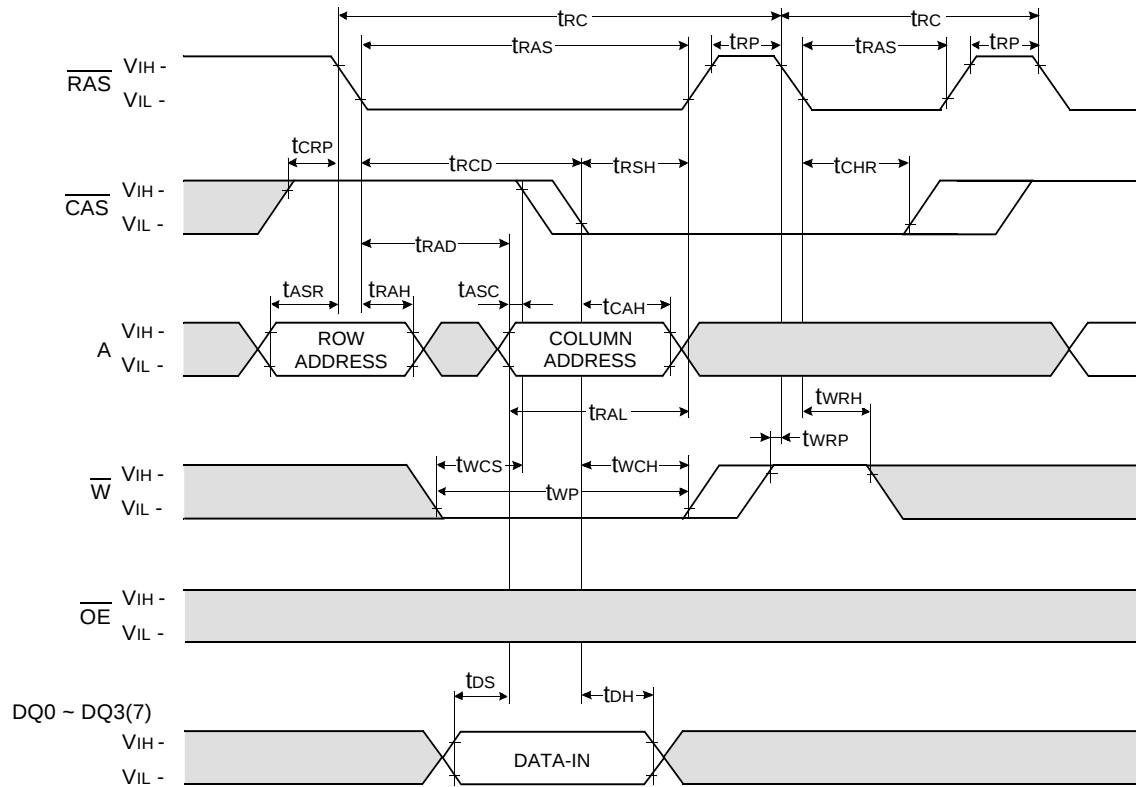
HIDDEN REFRESH CYCLE (READ)



Don't care
Undefined

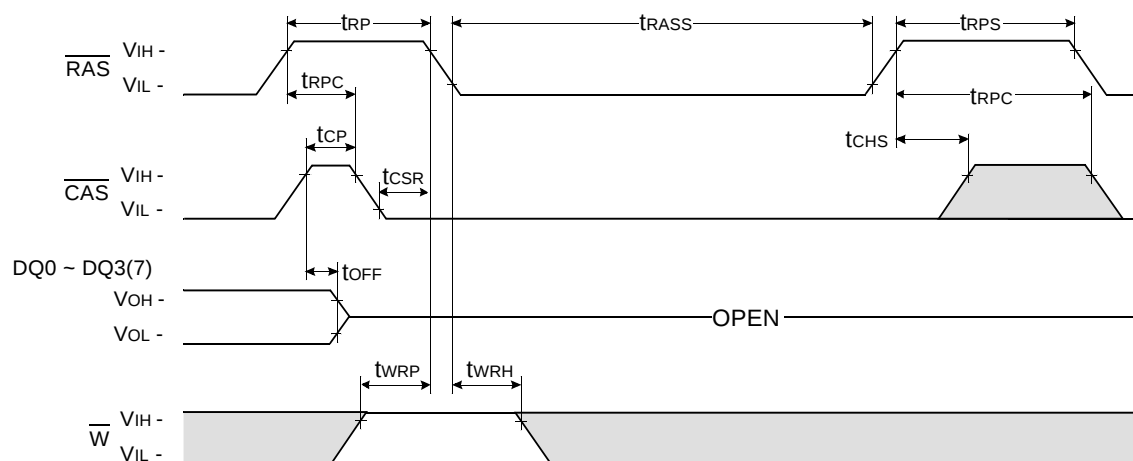
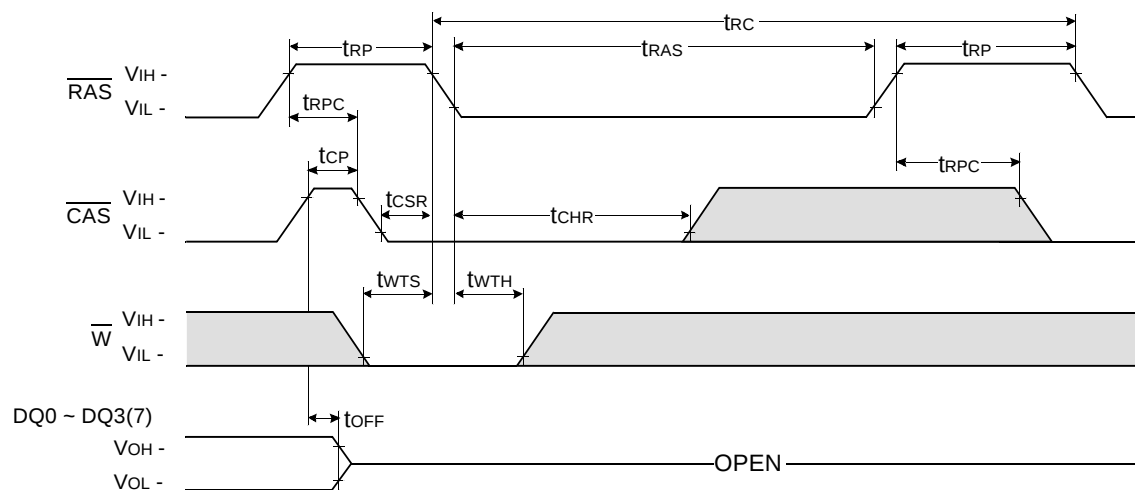
HIDDEN REFRESH CYCLE (WRITE)

NOTE : DOUT = OPEN



Don't care

Undefined

CAS - BEFORE - RAS SELF REFRESH CYCLENOTE : $\overline{\text{OE}}$, A = Don't care**TEST MODE IN CYCLE**NOTE : $\overline{\text{OE}}$, A = Don't care

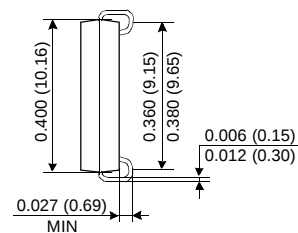
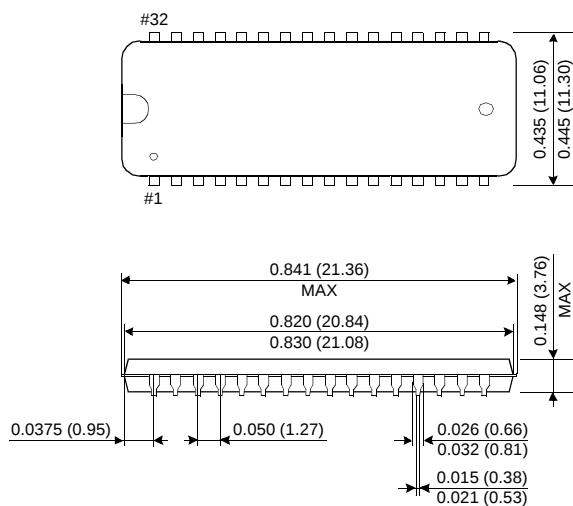
Don't care

Undefined

PACKAGE DIMENSION

32 SOJ 400mil

Units : Inches (millimeters)



32 TSOP(II) 400mil

Units : Inches (millimeters)

