High Speed 256K x 16Bit CMOS Dynamic RAM with Extended Data Out

DESCRIPTION

This is a family of 262,144 x 16 bit Extended Data Out Mode CMOS DRAMs. Extended Data Out Mode offers high speed random access of memory cells within the same row. Access time (-4), power consumption(Normal or Low power) and package type(SOJ or TSOP-II) are optional features of this family. All of this family have $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh and Hidden refresh capabilities. Furthermore, Self-refresh operation is available in L-version. This 256Kx16 EDO Mode DRAM family is fabricated using Samsung′s advanced CMOS process to realize high band-width, low power consumption and high reliability.
It may be used as graphic memory unit for microcomputer, personal computer and portable machines.

FEATURES

- **Part Identification**

  - KM416C254D/DL (5V, 512 Ref.)

- **Active Power Dissipation**

Unit : mW

Speed	Active Power Dissipation
-4	990

- **Refresh Cycles**

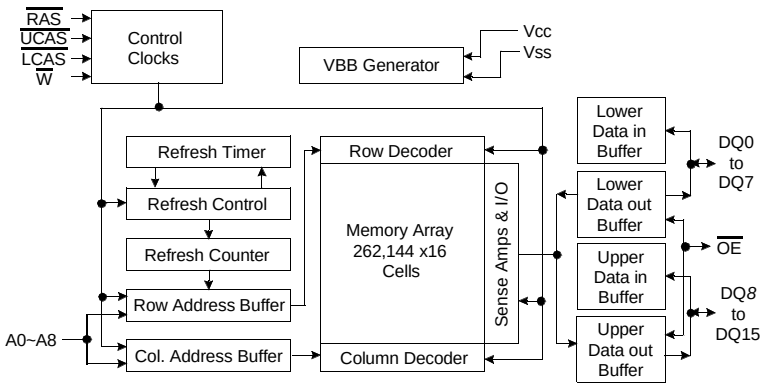
Part NO.	V_{CC}	Refresh cycle	Refresh period	
			Normal	L-ver
C254D	5V	512	8ms	128ms

- **Perfomance Range**

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{HPC}
-4	40ns	13ns	69ns	17ns

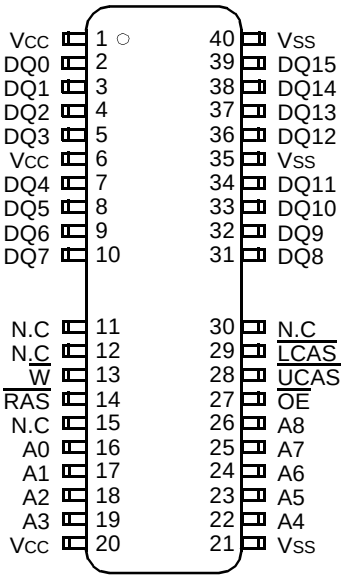
- Extended Data Out Mode operation
- 2 $\overline{CAS}$ Byte/Wrod Read/Write operation
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- Self-refresh capability (L-ver only)
- TTL compatible inputs and outputs
- Early Write or output enable controlled write
- JEDEC Standard pinout
- Available in 40-pin SOJ 400mil and 44(40)-pin TSOP(II) 400mil packages
- Triple +5V±10% power supply

FUNCTIONAL BLOCK DIAGRAM



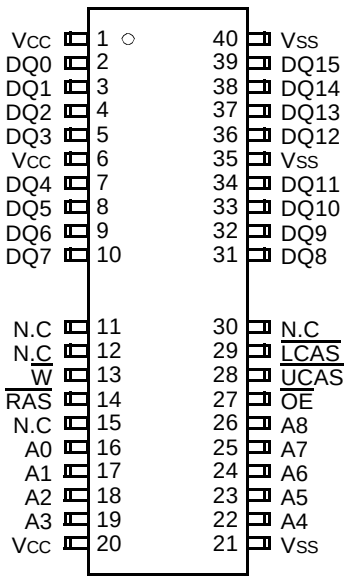
PIN CONFIGURATION (Top Views)

• KM416C254DJ



(SOJ)

• KM416C254DT



(TSOP-II)

Pin Name	Pin Function
A0 - A8	Address Inputs
DQ0 - 15	Data In/Out
VSS	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{UCAS}$	Upper Column Address Strobe
$\overline{LCAS}$	Lower Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
VCC	Power(+5V)
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on any pin relative to V_{SS}	V_{IN},V_{OUT}	-1.0 to +7.0	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-1.0 to +7.0	V
Storage Temperature	Tstg	-55 to +150	°C
Power Dissipation	P_D	1.1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, T_A= 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Units
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	V_{CC}+1.0*1	V
Input Low Voltage	V_{IL}	-1.0*2	-	0.8	V

*1 : V_{CC}+2.0V/20ns(5V), Pulse width is measured at V_{CC}
*2 : -2.0V/20ns(5V), Pulse width is measured at V_{SS}

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Units
Input Leakage Current (Any input 0≤V_{IN}≤V_{IN}+0.5V, all other input pins not under test=0 Volt)	$I_{I(L)}$	-5	5	uA
Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤V_{CC})	$I_{O(L)}$	-5	5	uA
Output High Voltage Level(I_{OH}=-5mA)	V_{OH}	2.4	-	V
Output Low Voltage Level(I_{OL}=4.2mA)	V_{OL}	-	0.4	V

DC AND OPERATING CHARACTERISTICS (Continued)

Symbol	Power	Max	Units
I_{CC1}	Don't care	180	mA
I_{CC2}	Don't care	2	mA
I_{CC3}	Don't care	180	mA
I_{CC4}	Don't care	145	mA
I_{CC5}	Normal L	1 150	mA uA
I_{CC6}	Don't care	180	mA
I_{CC7}	L	300	uA
I_{CCS}	L	200	uA

I_{CC1}* : Operating Current ($\overline{RAS}$ and $\overline{UCAS}$, $\overline{LCAS}$, Address cycling @t_{RC}=min.)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=$\overline{W}$=V_{IH})

I_{CC3}* : $\overline{RAS}$-only Refresh Current ($\overline{UCAS}$=$\overline{LCAS}$=V_{IH}, $\overline{RAS}$, Address cycling @t_{RC}=min.)

I_{CC4}* : Extended Data Out Mode Current ($\overline{RAS}$=V_{IL}, $\overline{UCAS}$ or $\overline{LCAS}$, Address cycling @t_{HPC}=min.)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=$\overline{W}$=V_{CC}-0.2V)

I_{CC6}* : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current ($\overline{RAS}$ and $\overline{UCAS}$ or $\overline{LCAS}$ cycling @t_{RC}=min.)

I_{CC7} : Battery back-up current, Average power supply current, Battery back-up mode
Input high voltage(V_{IH})=V_{CC}-0.2V, Input low voltage(V_{IL})=0.2V, $\overline{UCAS}$, $\overline{LCAS}$=0.2V,
DQ=Don't care, T_{RC}=31.25us, T_{RAS}=T_{RAS}min~300ns

I_{CCS} : Self Refresh Current
$\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=V_{IL}, $\overline{W}$=$\overline{OE}$=A0 ~ A12(A11)=V_{CC}-0.2V or 0.2V,
DQ0 ~ DQ15=V_{CC}-0.2V, 0.2V or Open

***Note :** I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1}, I_{CC3}, I_{CC6} and I_{CC7}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one Hyper page mode cycle time, t_{HPC}.

CAPACITANCE (T_A=25°C, V_{CC}=5V, f=1MHz)

Parameter	Symbol	Min	Max	Units
Input capacitance [A0 ~ A12]	C_{IN1}	-	5	pF
Input capacitance [$\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$, $\overline{W}$, $\overline{OE}$]	C_{IN2}	-	7	pF
Output capacitance [DQ0 - DQ15]	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤60°C, See note 1,2)

Test condition : V_{CC}=5.0V±10%, Vih/Vil=2.8/0.4V, Voh/Vol=2.0/0.8V

Parameter	Symbol	-4		Units	Notes
		Min	Max		
Random read or write cycle time	t_{RC}	69		ns	
Read-modify-write cycle time	t_{RWC}	94		ns	
Access time from $\overline{RAS}$	t_{RAC}		40	ns	3,4,10
Access time from $\overline{CAS}$	t_{CAC}		13	ns	3,4,5
Access time from column address	t_{AA}		20	ns	3,10
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	3		ns	3
Output buffer turn-off delay from $\overline{CAS}$	t_{CEZ}	3	11	ns	6,12
Transition time (rise and fall)	t_T	2	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	25		ns	
$\overline{RAS}$ pulse width	t_{RAS}	40	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	9		ns	
$\overline{CAS}$ hold time	t_{CSH}	34		ns	
$\overline{CAS}$ pulse width	t_{CAS}	6.5	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	18	27	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	13	20	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		ns	
Row address set-up time	t_{ASR}	0		ns	
Row address hold time	t_{RAH}	8		ns	
Column address set-up time	t_{ASC}	0		ns	13
Column address hold time	t_{CAH}	6.5		ns	13
Column address to $\overline{RAS}$ lead time	t_{RAL}	20		ns	
Read command set-up time	t_{RCS}	0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		ns	8
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		ns	8
Write command set-up time	t_{WCS}	0		ns	7
Write command hold time	t_{WCH}	7		ns	
Write command pulse width	t_{WP}	7		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	8		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	6		ns	16

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-4		Units	Notes
		Min	Max		
Data set-up time	t_{DS}	0		ns	9,19
Data hold time	t_{DH}	6.5		ns	19
Refresh period (Normal)	t_{REF}		8	ms	
Refresh period (L-ver)	t_{REF}		128	ms	
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	28		ns	7,15
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	55		ns	7
Column address to $\overline{W}$ delay time	t_{AWD}	35		ns	7
$\overline{CAS}$ precharge to $\overline{W}$ delay time	t_{CPWD}	38		ns	7
$\overline{CAS}$ set-up time ($\overline{CAS}$ -before-$\overline{RAS}$ refresh)	t_{CSR}	5		ns	17
$\overline{CAS}$ hold time ($\overline{CAS}$ -before-$\overline{RAS}$ refresh)	t_{CHR}	10		ns	18
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	t_{CPT}	20		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		23	ns	3
Hyper Page mode cycle time	t_{HPC}	17		ns	11
Hyper Page read-modify-write cycle time	t_{HPRWC}	48		ns	11
$\overline{CAS}$ precharge time (Hyper Page cycle)	t_{CP}	6.5		ns	14
$\overline{RAS}$ pulse width (Hyper Page cycle)	t_{RASP}	40	100K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	25		ns	
$\overline{OE}$ access time	t_{OEA}		13	ns	12
$\overline{OE}$ to data delay	t_{OED}	11		ns	
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	3	11	ns	6
$\overline{OE}$ command hold time	t_{OEH}	13		ns	
Output data hold time	t_{DOH}	4		ns	
Output buffer turn off delay from $\overline{RAS}$	t_{REZ}	3	15	ns	6,12
Output buffer turn off delay from $\overline{W}$	t_{WEZ}	3	11	ns	6
$\overline{W}$ to data delay	t_{WED}	11		ns	
$\overline{OE}$ to $\overline{CAS}$ hold time	t_{OCH}	5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	t_{CHO}	5		ns	
$\overline{OE}$ precharge time	t_{OEP}	5		ns	
$\overline{W}$ pulse width (Hyper Page Cycle)	t_{WPE}	5		ns	
$\overline{RAS}$ pulse width ($\overline{C}$-B-$\overline{R}$ self refresh)	t_{RASS}	100		us	20,21,22
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	t_{RPS}	74		ns	20,21,22
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	t_{CHS}	-50		ns	20,21,22

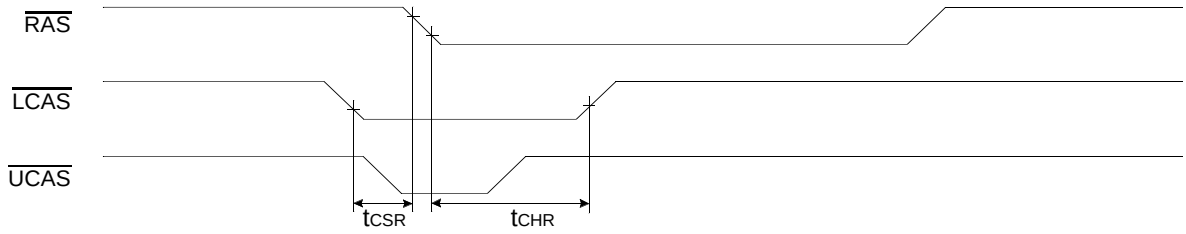
NOTES

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only refresh or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals.
   Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 2ns for all inputs.
3. Measured with a load equivalent to 2 TTL load and 30pF. Dout reference level : Voh/Vol=2.0V/0.8V
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only.
   If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{oh} or V_{ol}.
7. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min), the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min), $t_{AWD} \geq t_{AWD}$(min) and $t_{CPWD} \geq t_{CPWD}$(min) then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9. These parameters are referenced to the first $\overline{CAS}$ falling edge in early write cycles and to $\overline{W}$ falling edge in $\overline{OE}$ controlled write cycle and read-modify-write cycles.
10. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only.
    If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
11. $t_{ASC} \geq 5$ns, Assume t_T = 2.0ns
12. If $\overline{RAS}$ goes high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes high before $\overline{RAS}$ high going, the open circuit condition of the output is achieved by $\overline{RAS}$ going

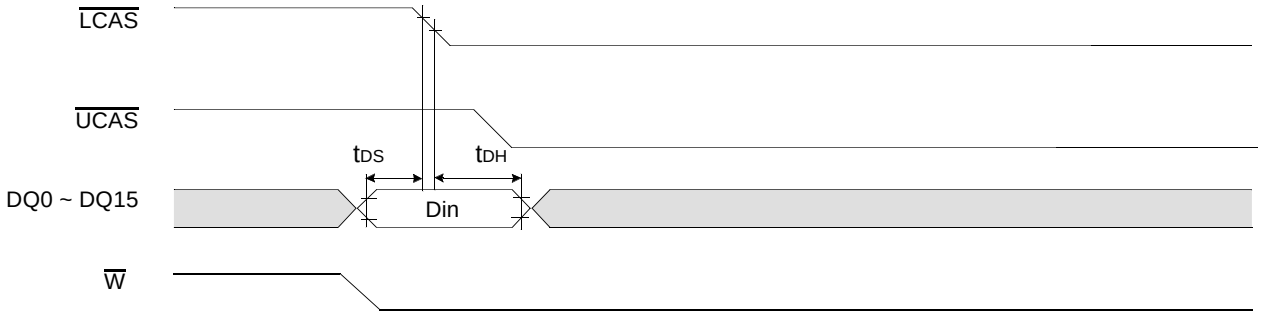
KM416C254D/DL Truth Table

$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{W}$	$\overline{OE}$	DQ0 - DQ7	DQ8-DQ15	STATE
H	H	H	H	H	Hi-Z	Hi-Z	Standby
L	H	H	H	H	Hi-Z	Hi-Z	Refresh
L	L	H	H	L	DQ-OUT	Hi-Z	Byte Read
L	H	L	H	L	Hi-Z	DQ-OUT	Byte Read
L	L	L	H	L	DQ-OUT	DQ-OUT	Word Read
L	L	H	L	H	DQ-IN	-	Byte Write
L	H	L	L	H	-	DQ-IN	Byte Write
L	L	L	L	H	DQ-IN	DQ-IN	Word Write
L	L	L	H	H	Hi-Z	Hi-Z	-

13. t_{ASC}, t_{CAH} are referenced to the earlier $\overline{CAS}$ rising edge.
14. t_{CP} is specified from the last $\overline{CAS}$ rising edge in the previous cycle to the first $\overline{CAS}$ falling edge in the next cycle.
15. t_{CWD} is referenced to the later $\overline{CAS}$ falling edge at word red-modify-write cycle.
16. t_{CWL} is specified from $\overline{W}$ falling edge to the earlier $\overline{CAS}$ rising edge.
17. t_{CSR} is referenced to earlier $\overline{CAS}$ falling low before $\overline{RAS}$ transition low.
18. t_{CHR} is referenced to the later $\overline{CAS}$ rising high after $\overline{RAS}$ transition low.

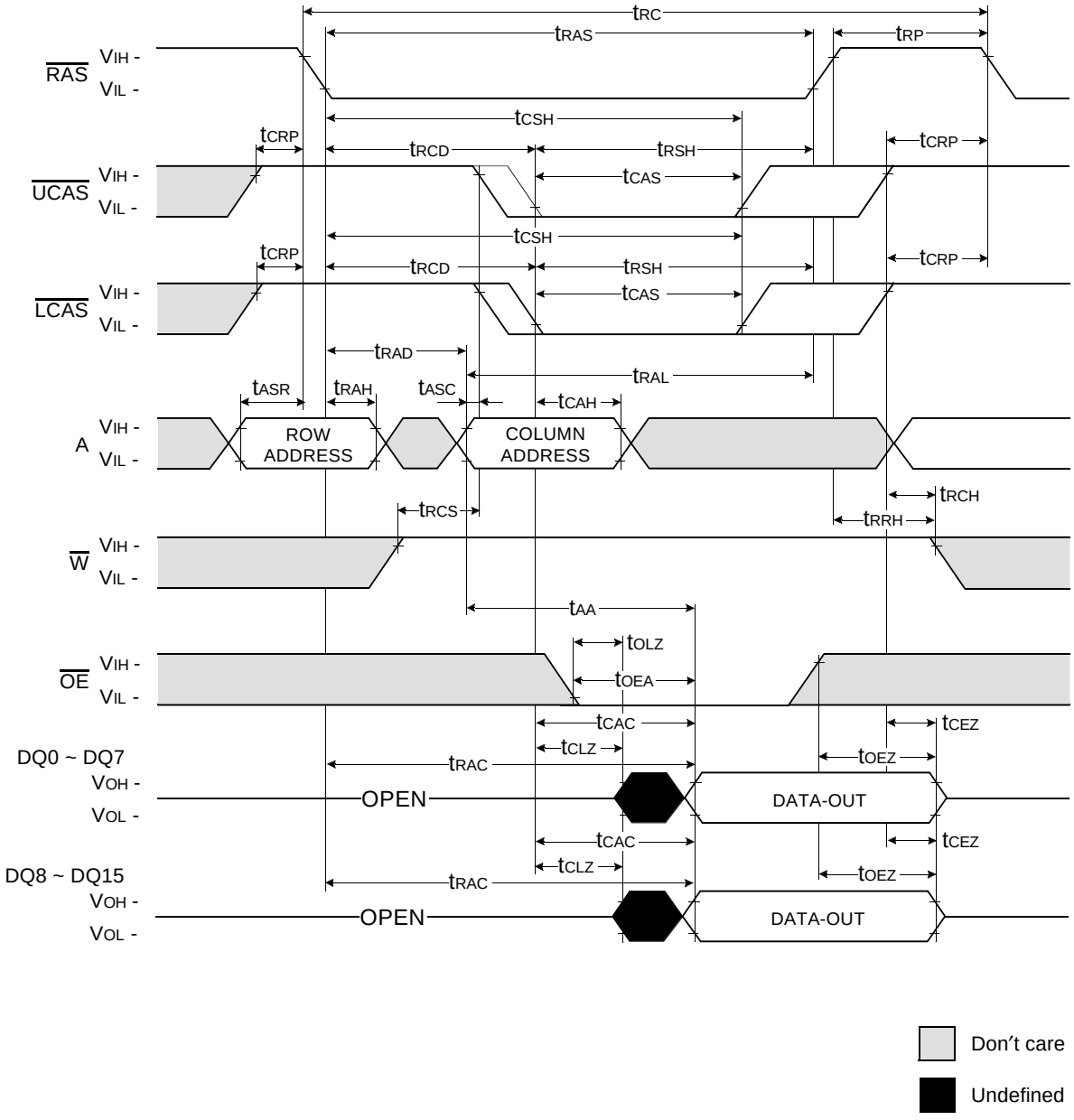


19. t_{DS}, t_{DH} are specified for earlier $\overline{CAS}$ falling low.



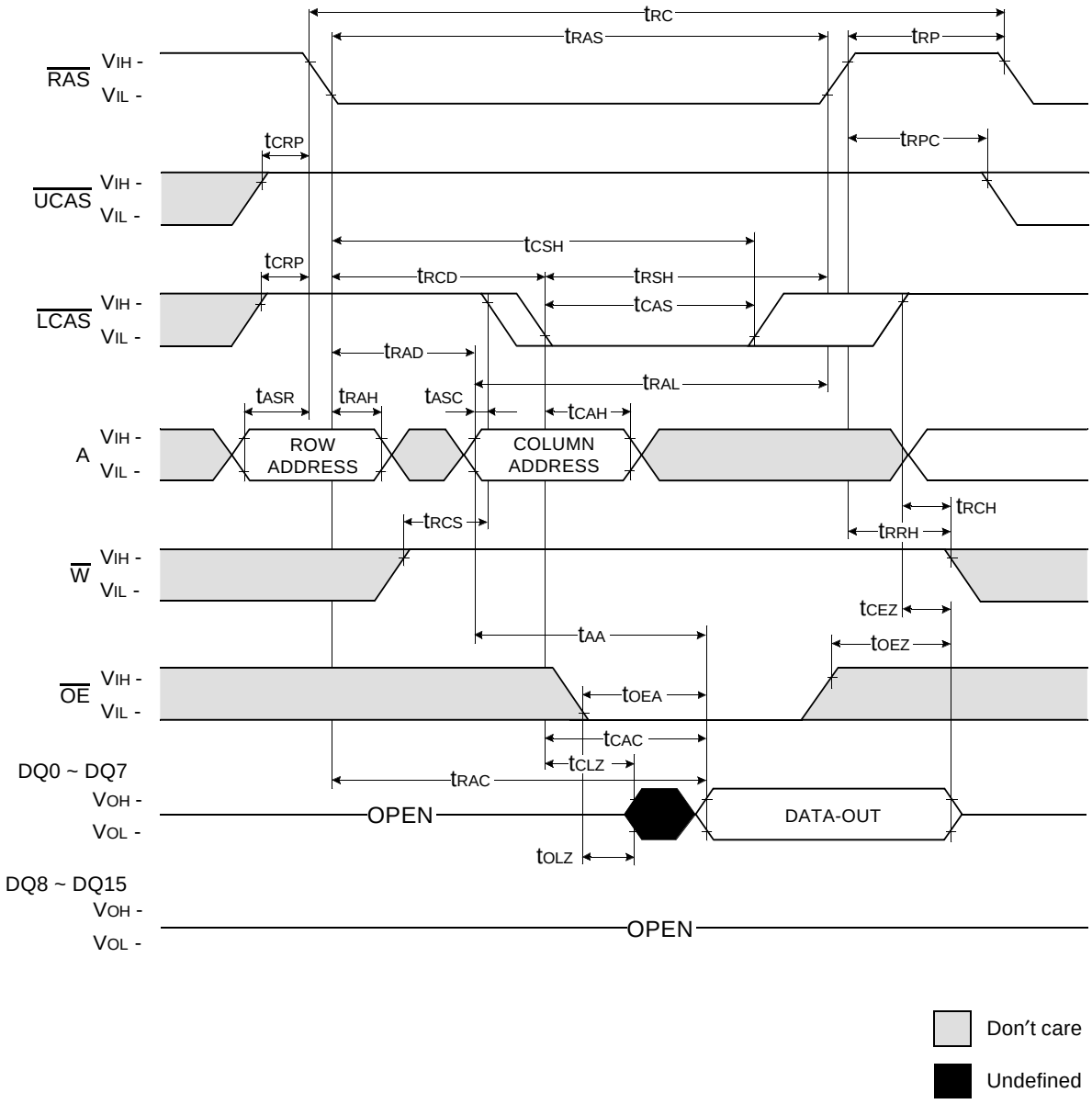
20. If $t_{RASS} \geq 100us$, then $\overline{RAS}$ precharge time must use t_{RPS} instead of t_{RP}.
21. For $\overline{RAS}$-only refresh and burst $\overline{CAS}$-before-$\overline{RAS}$ refresh mode, 512(512K) cycle of burst refresh must be executed within 8ms before and after self refresh, in order to meet refresh specification.
22. For distributed $\overline{CAS}$-before-$\overline{RAS}$ with 15.6us interval, $\overline{CAS}$-before-$\overline{RAS}$ refresh should be executed with in 15.6us immediately before and after self refresh in order to meet refresh specification.

WORD READ CYCLE



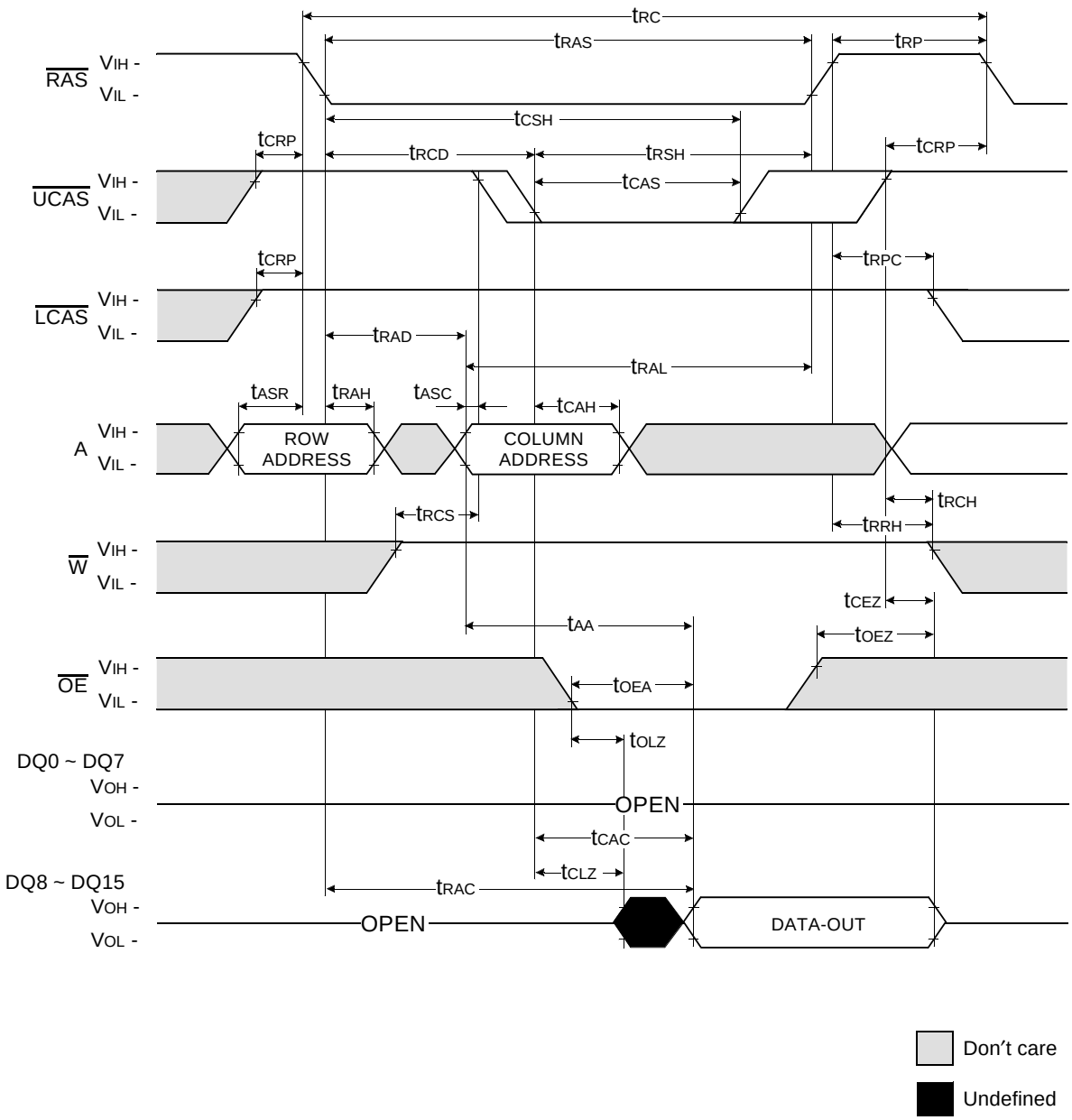
LOWER BYTE READ CYCLE

NOTE : D_{IN} = OPEN



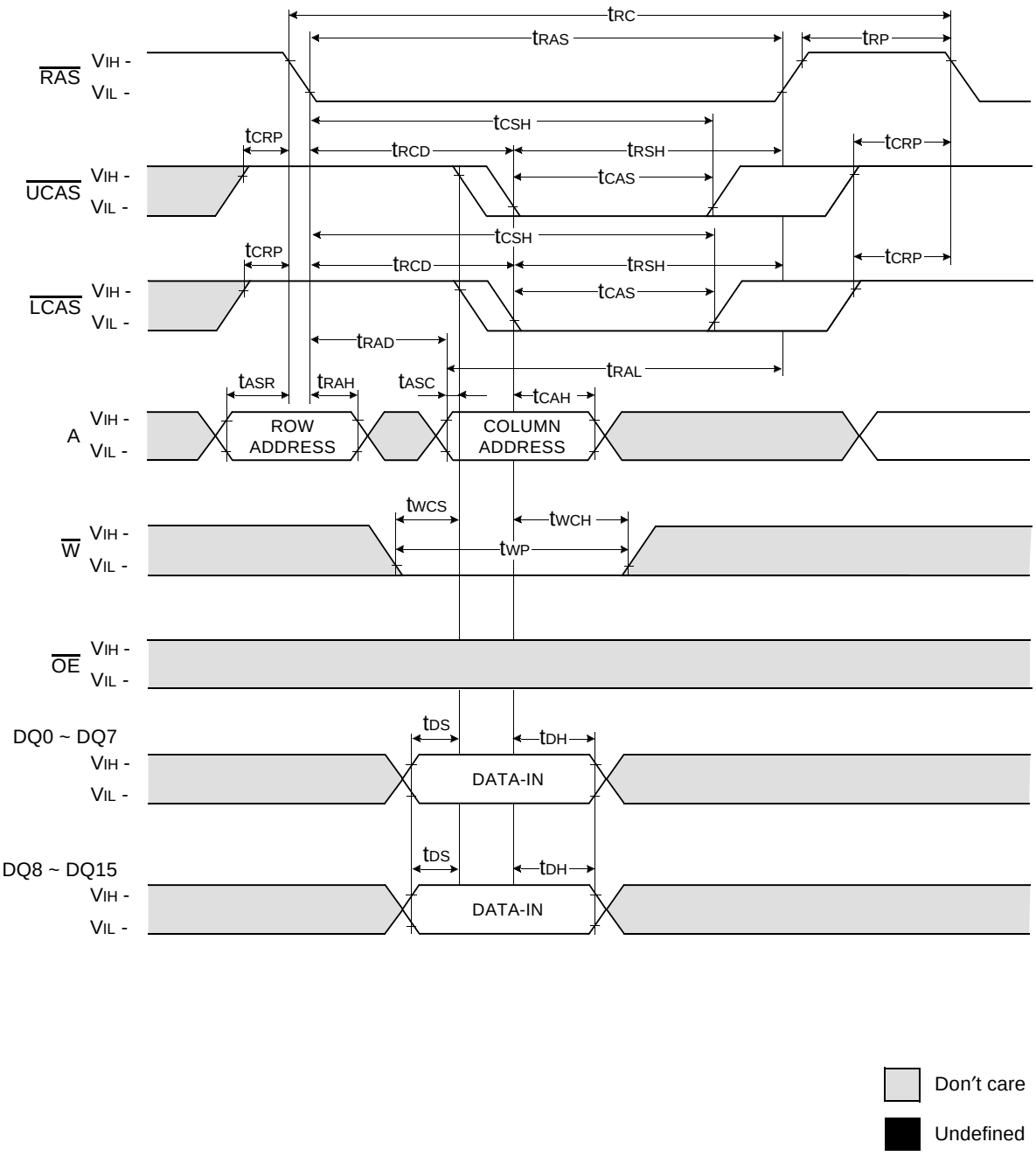
UPPER BYTE READ CYCLE

NOTE : D_{IN} = OPEN



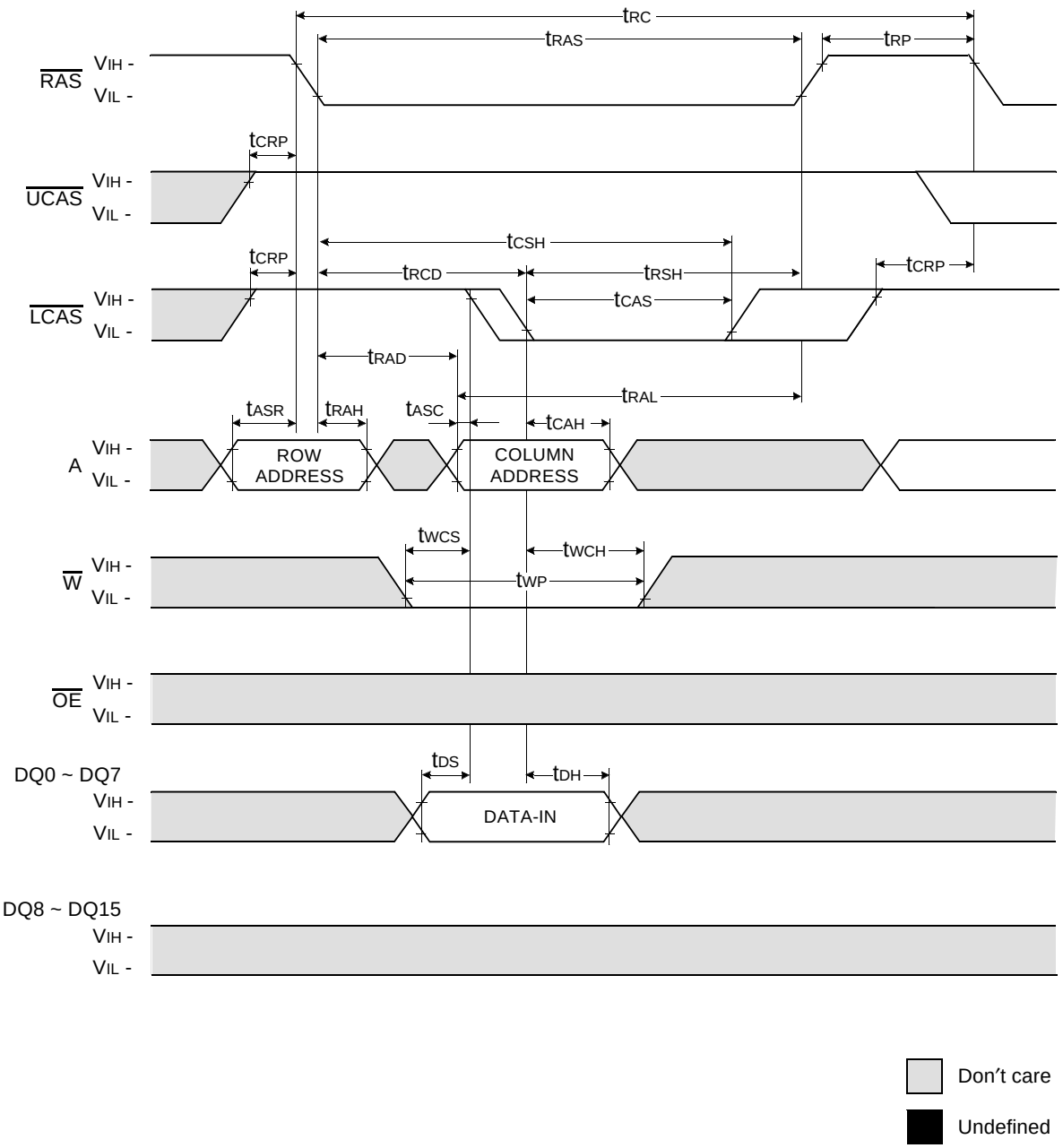
WORD WRITE CYCLE (EARLY WRITE)

NOTE : DOUT = OPEN



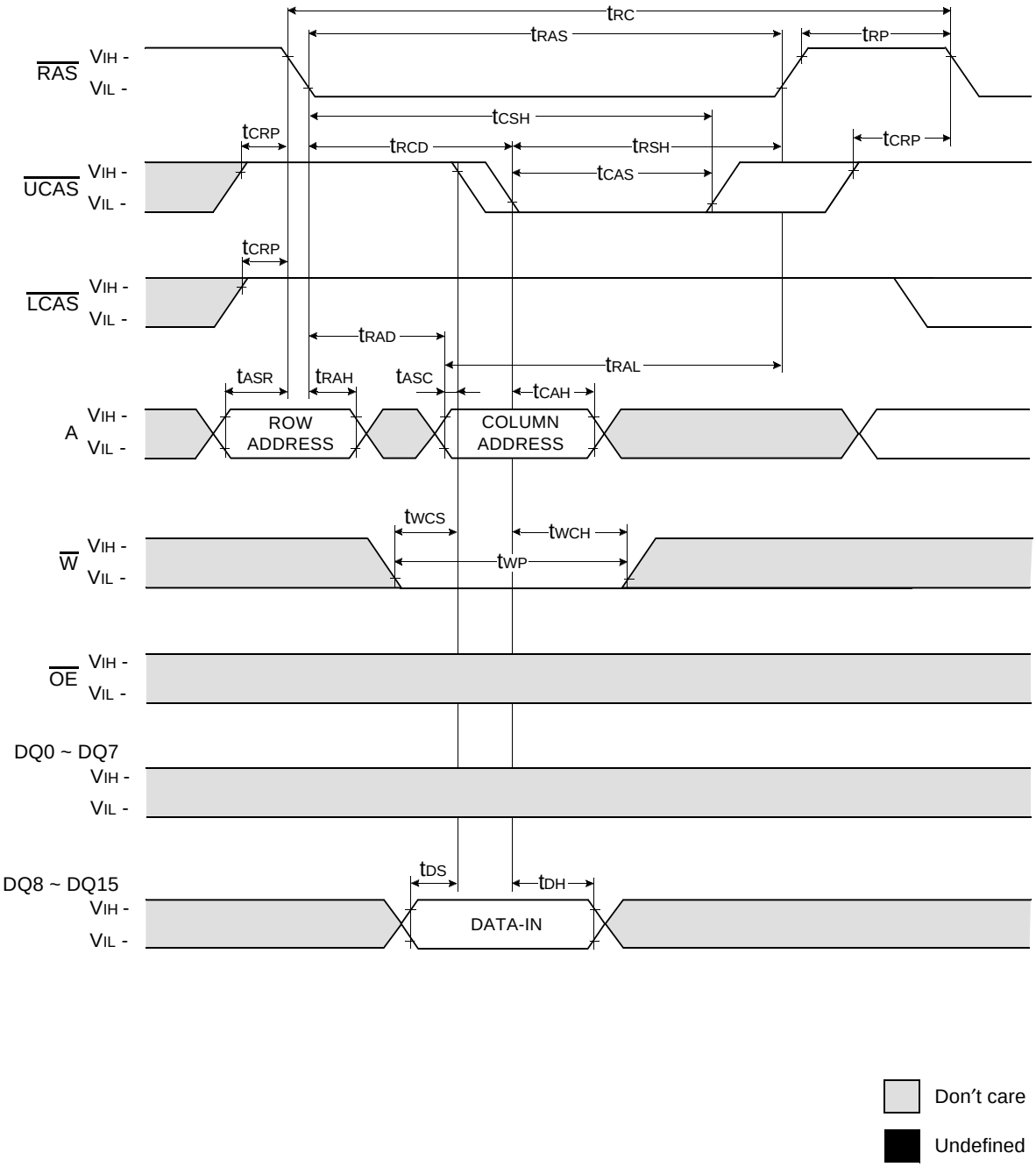
LOWER BYTE WRITE CYCLE (EARLY WRITE)

NOTE : DOUT = OPEN



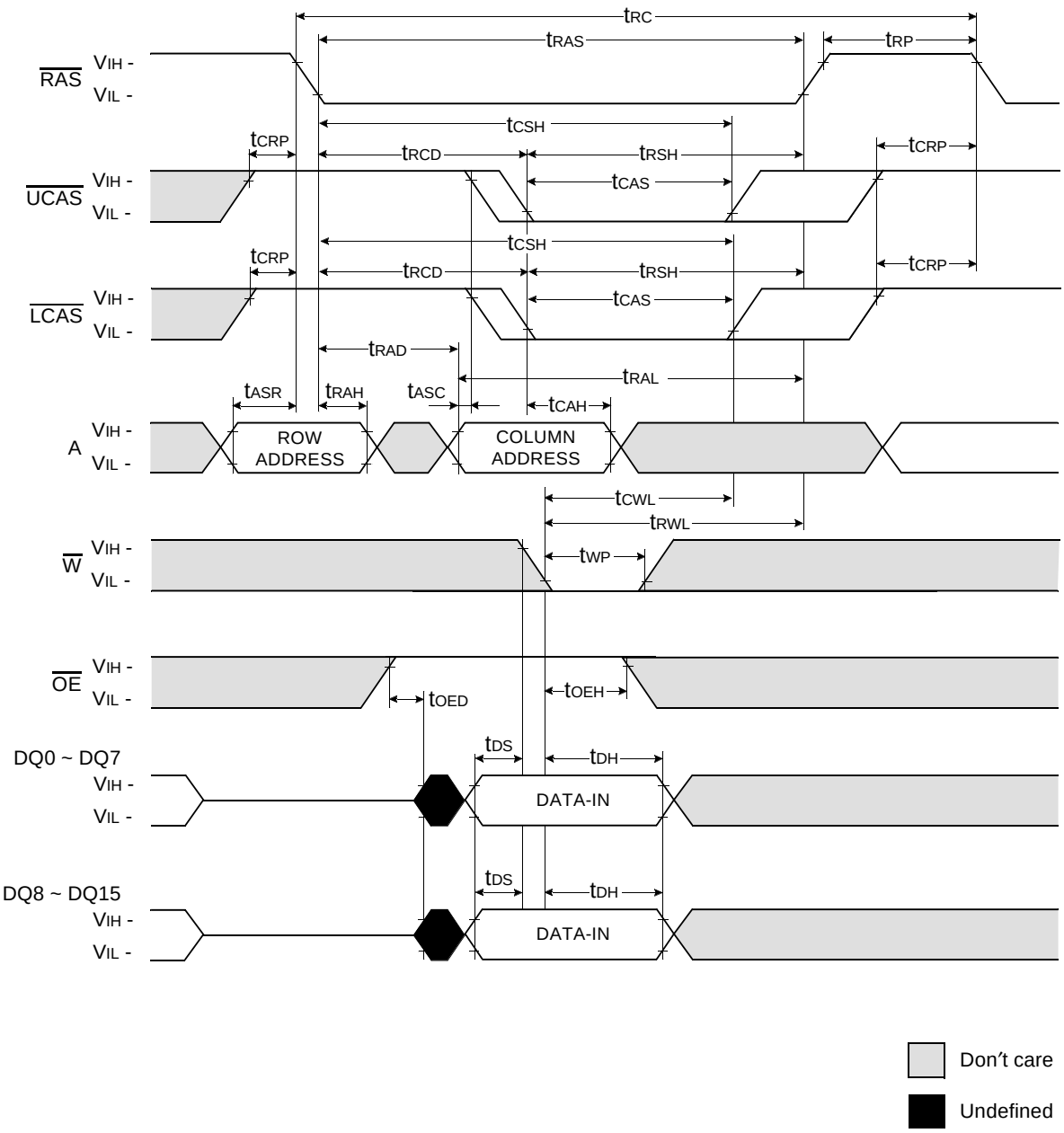
UPPER BYTE WRITE CYCLE (EARLY WRITE)

NOTE : DOUT = OPEN



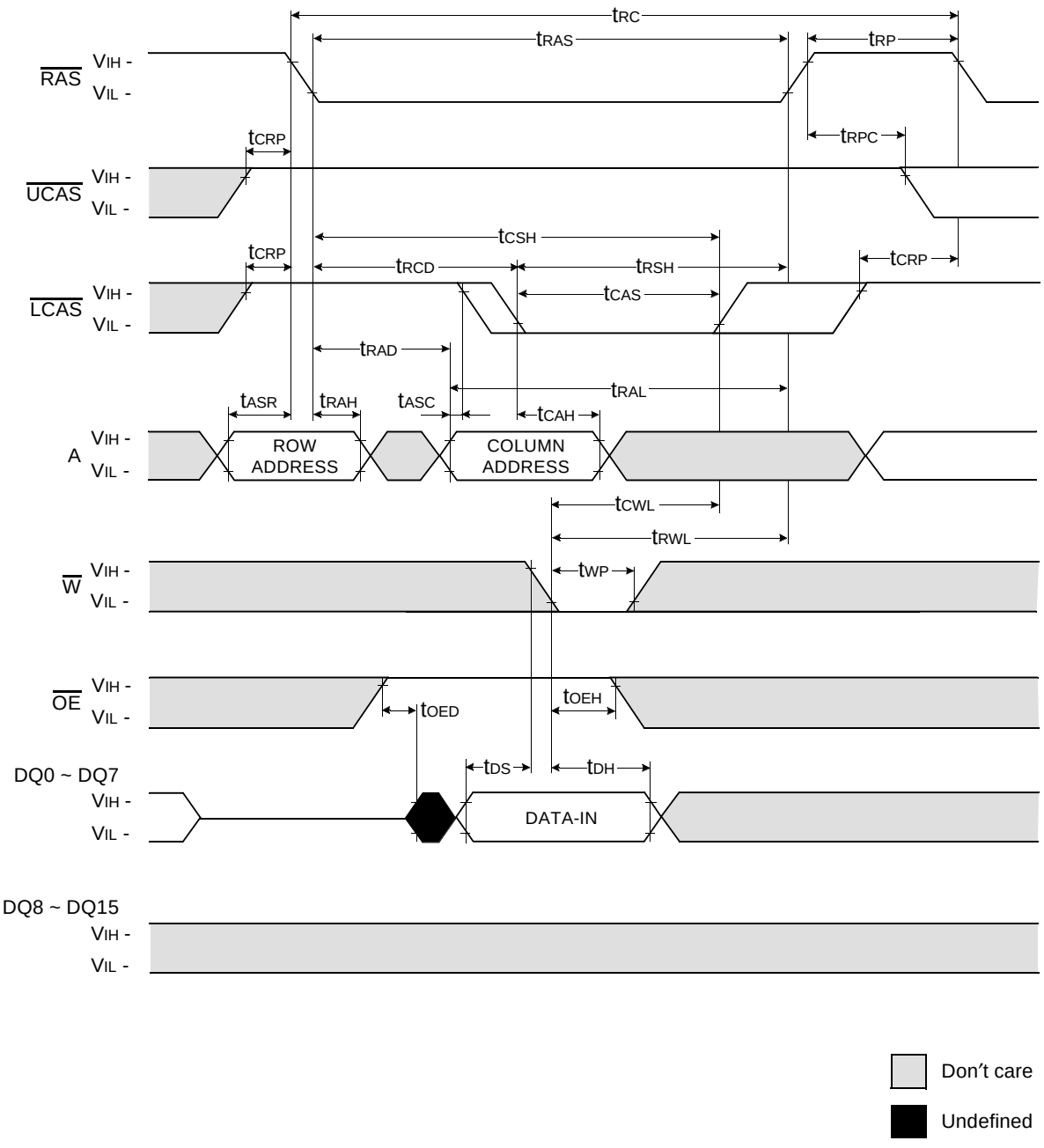
WORD WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

NOTE : DOUT = OPEN



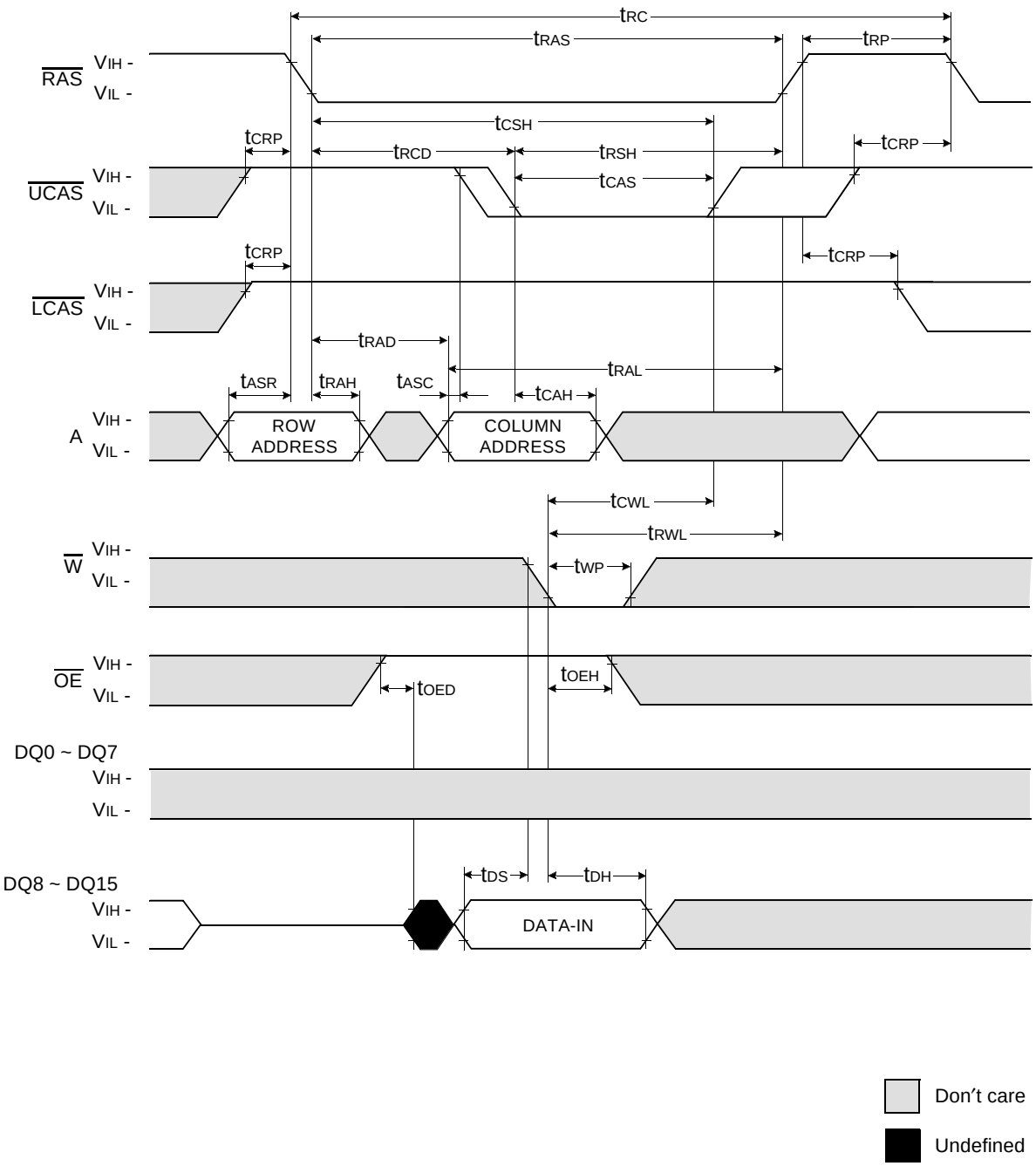
LOWER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

NOTE : DOUT = OPEN

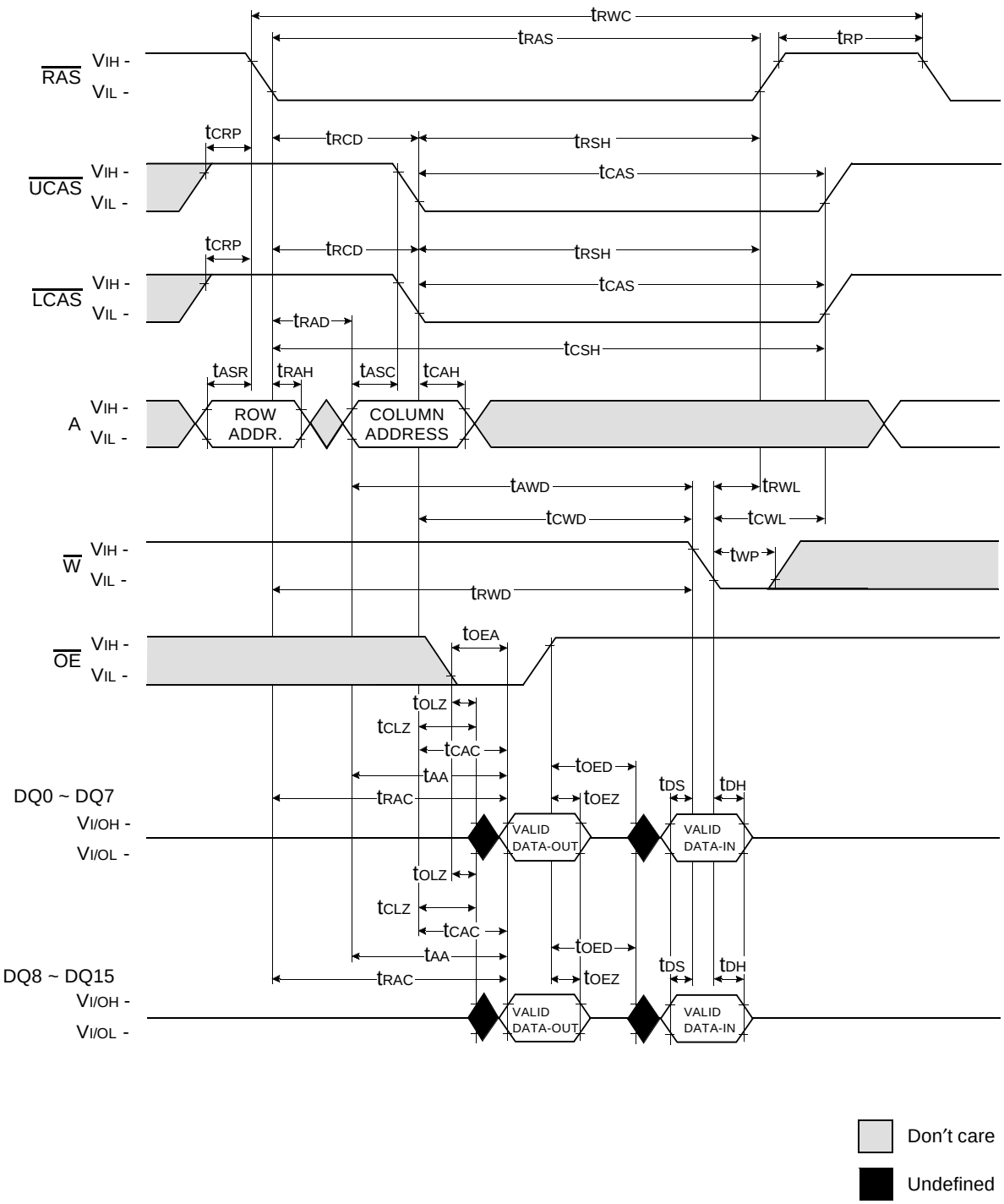


UPPER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

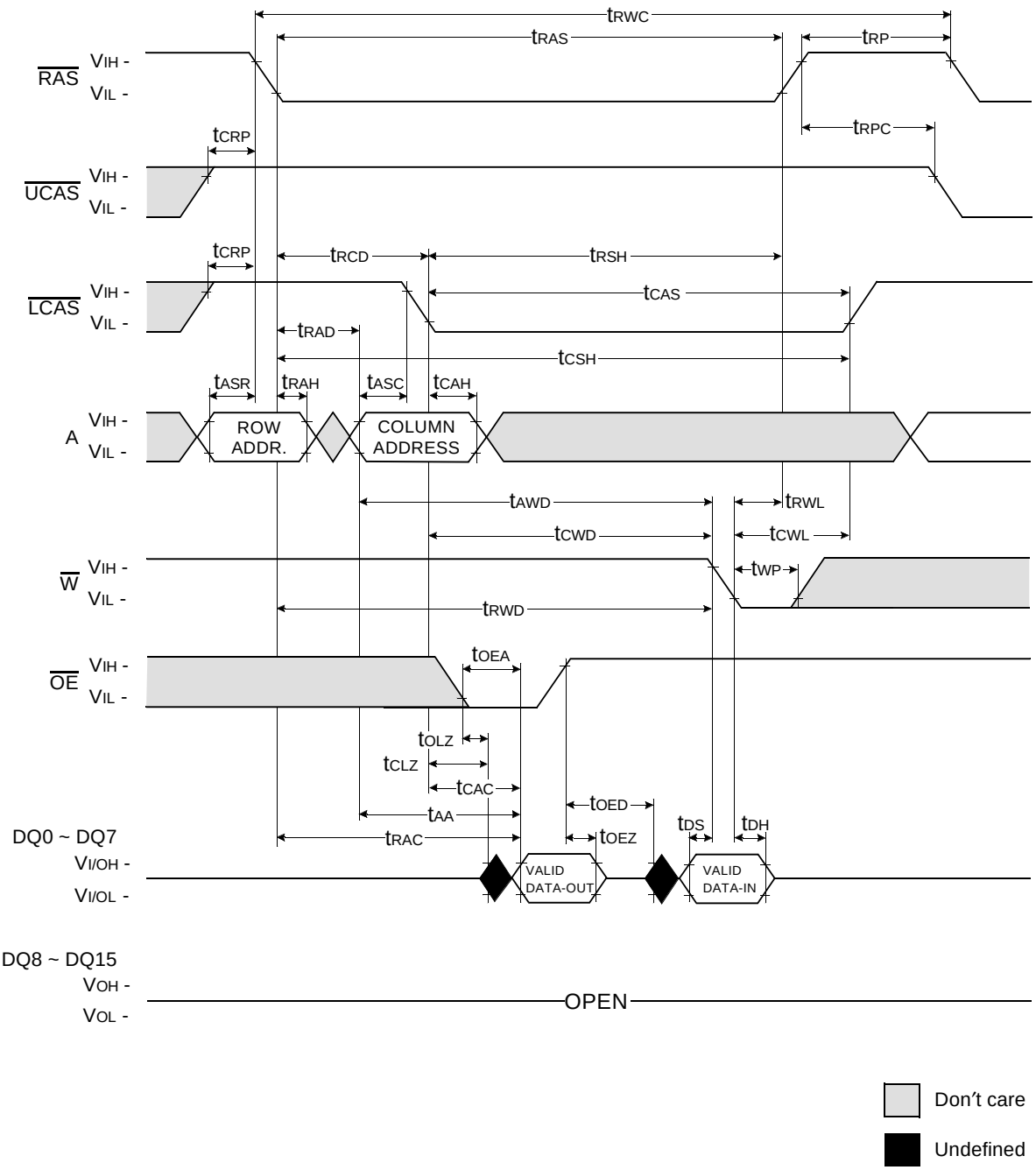
NOTE : DOUT = OPEN



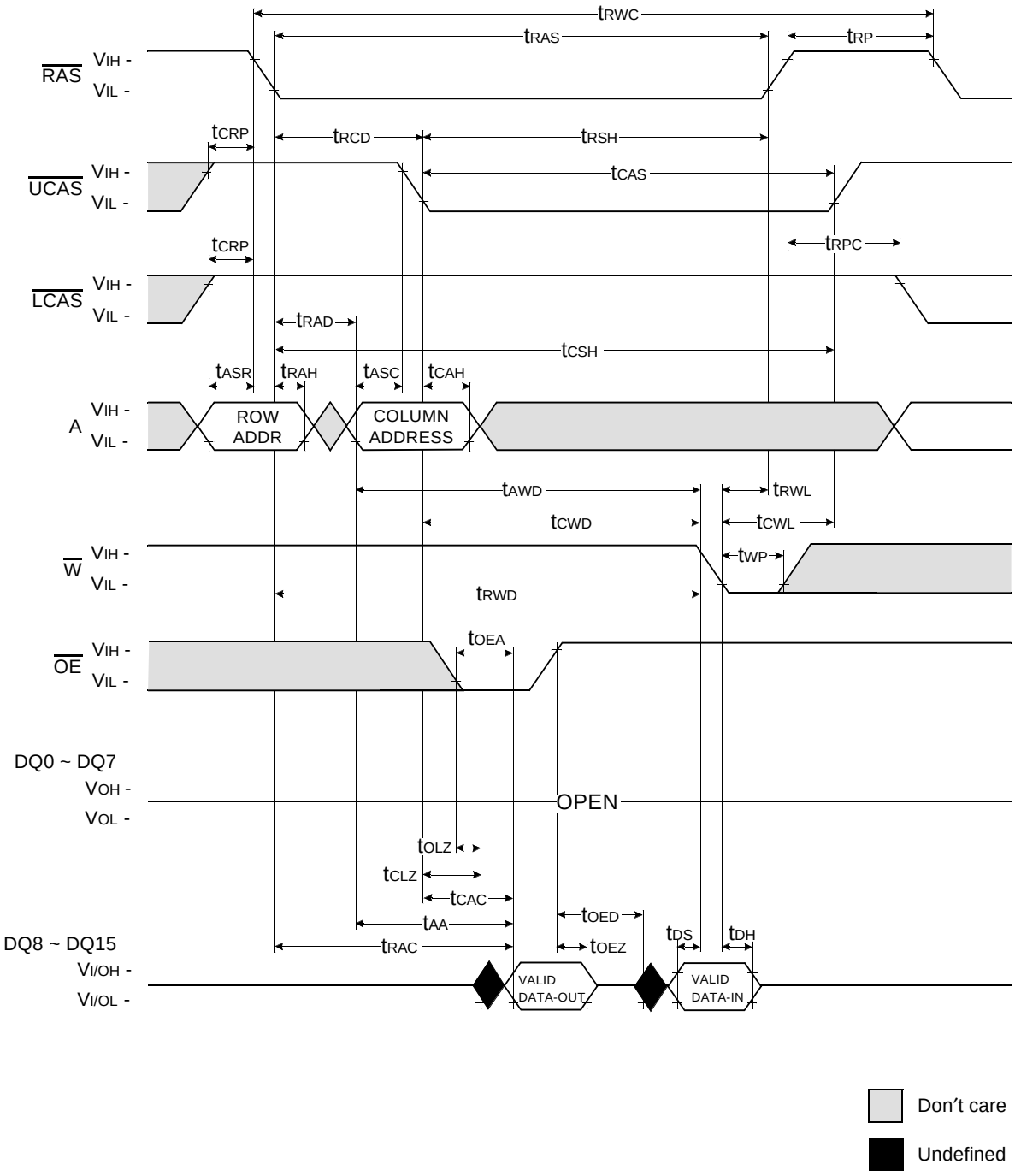
WORD READ - MODIFY - WRITE CYCLE



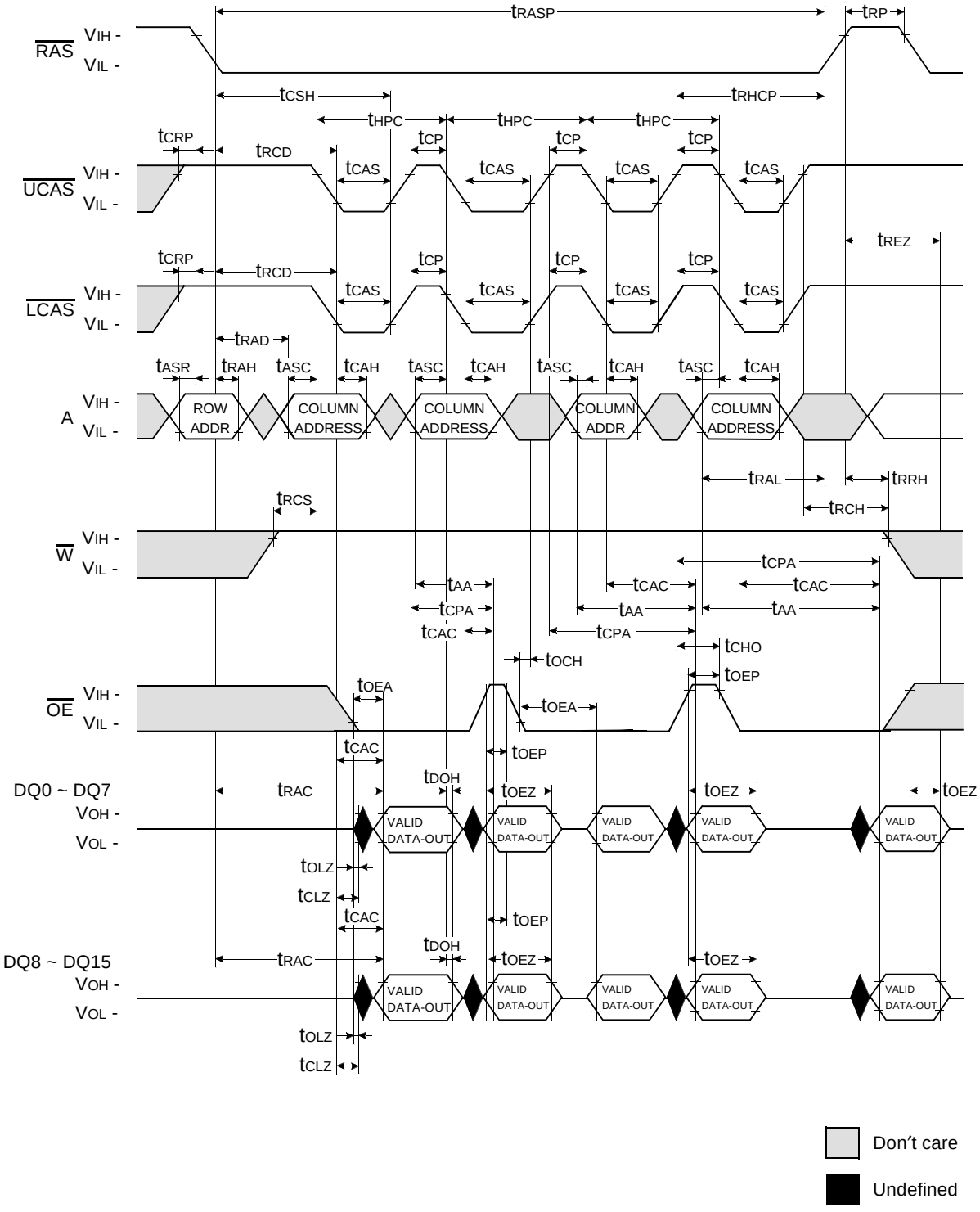
LOWER-BYTE READ - MODIFY - WRITE CYCLE



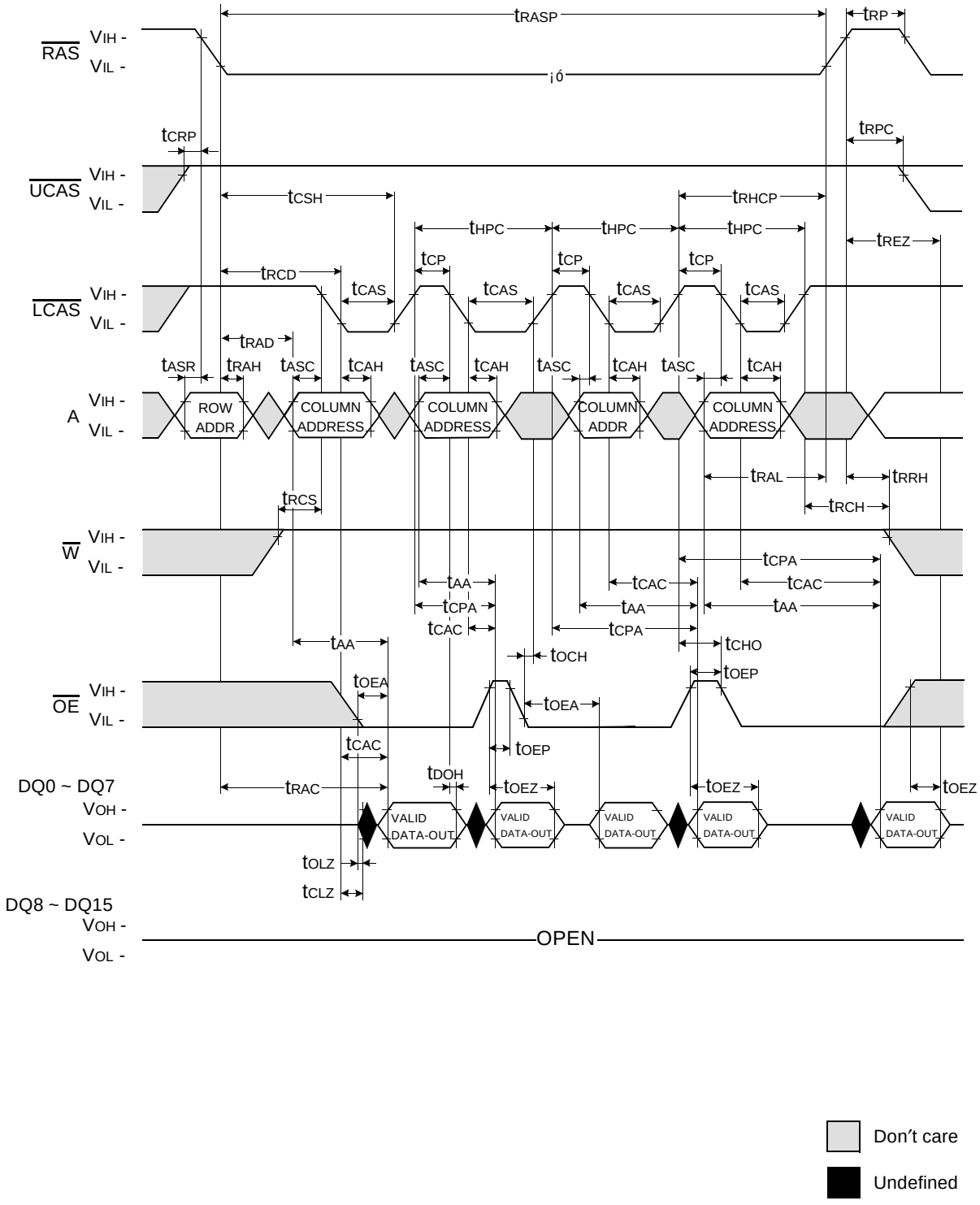
UPPER-BYTE READ - MODIFY - WRITE CYCLE



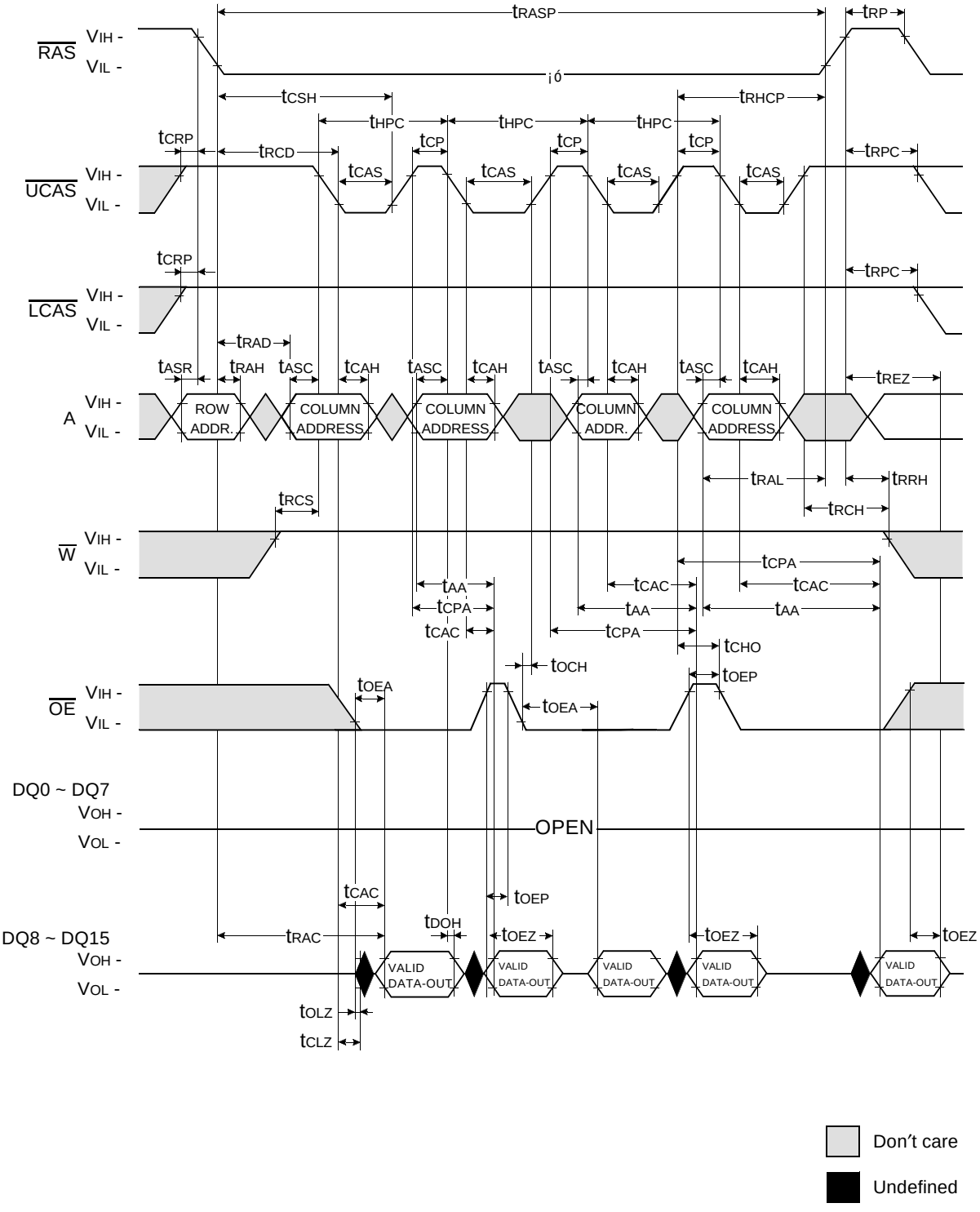
HYPER PAGE MODE WORD READ CYCLE



HYPER PAGE MODE LOWER BYTE READ CYCLE

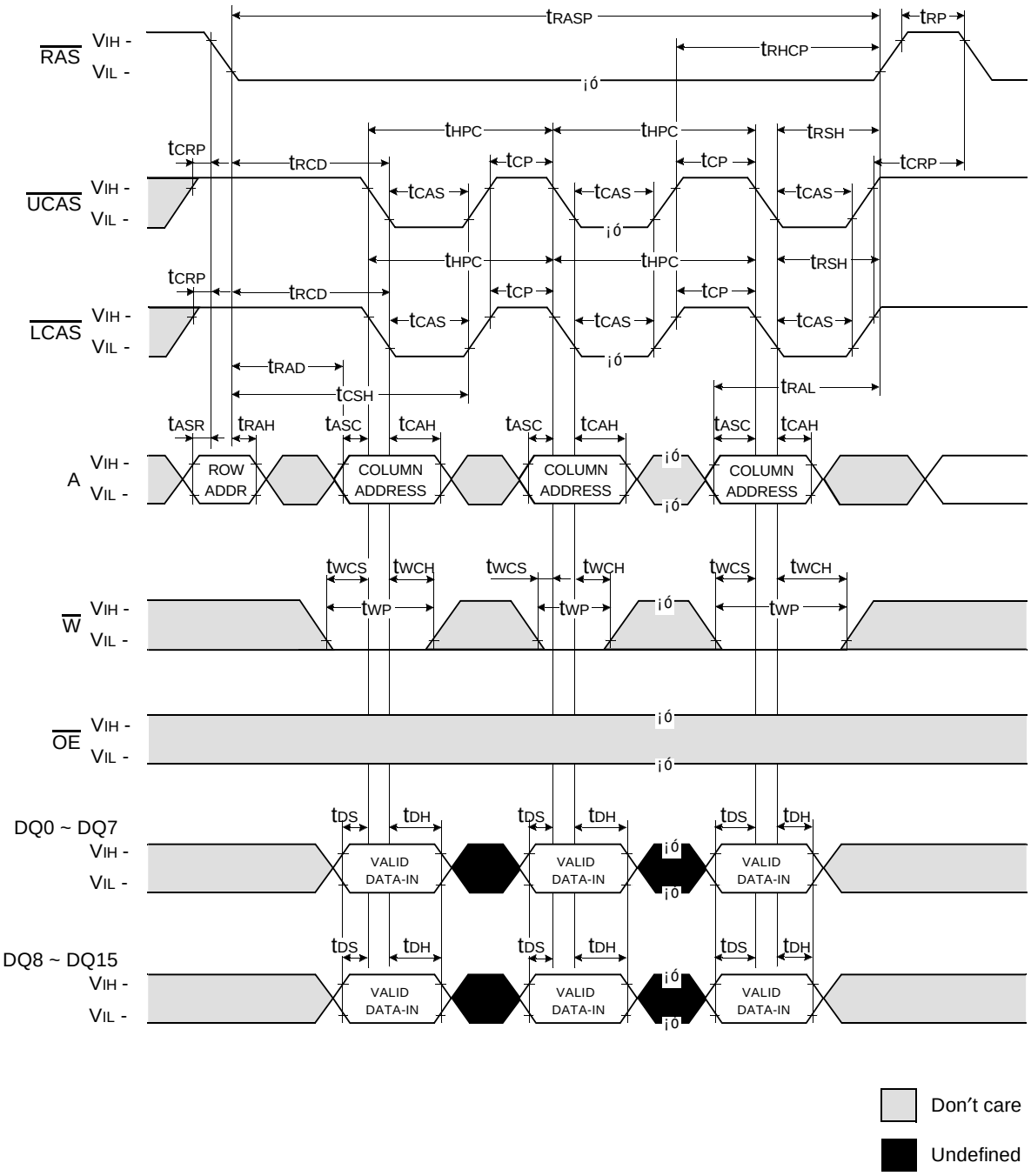


HYPER PAGE MODE UPPER BYTE READ CYCLE



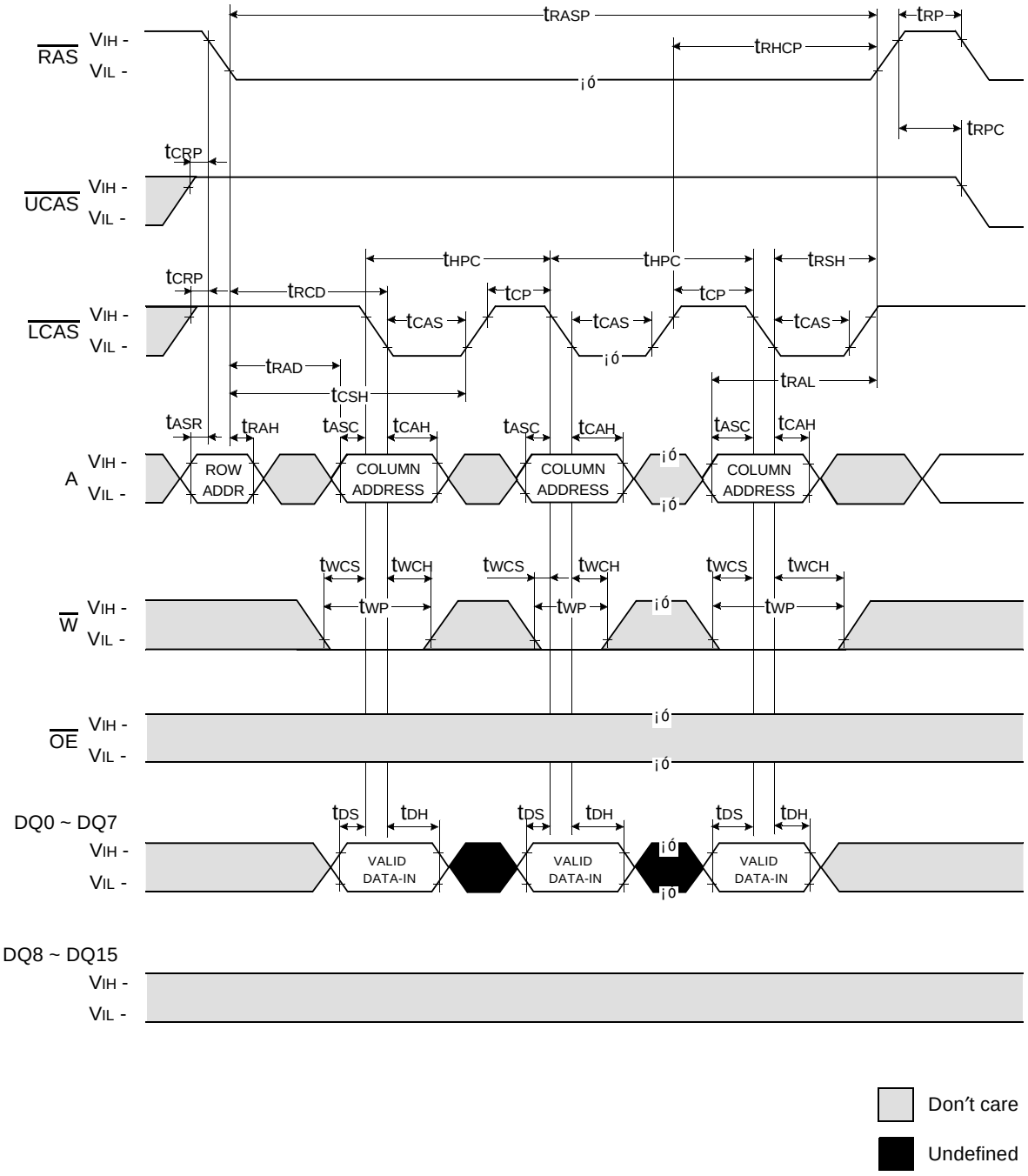
HYPER PAGE MODE WORD WRITE CYCLE (EARLY WRITE)

NOTE : DOUT = OPEN



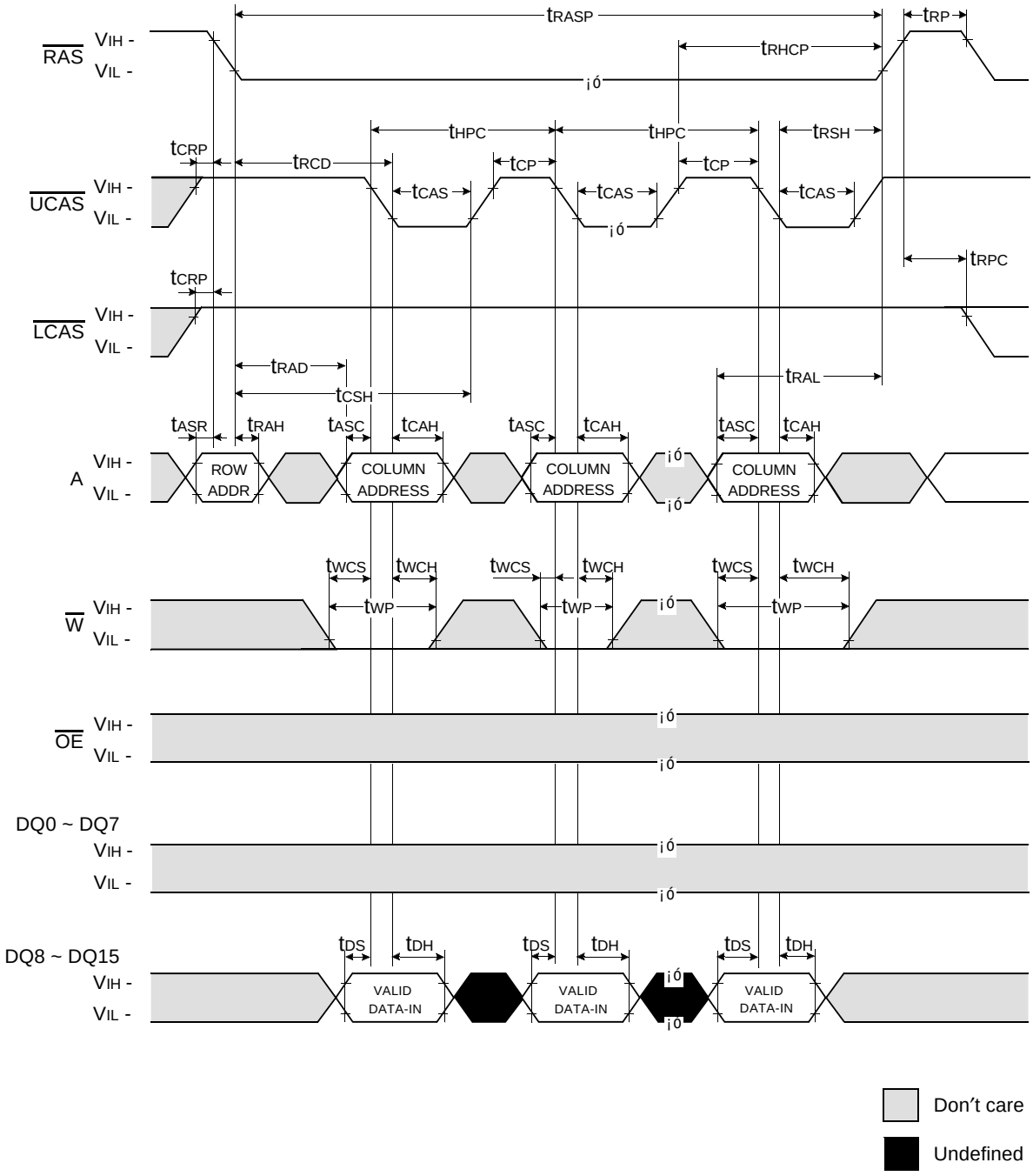
HYPER PAGE MODE LOWER BYTE WRITE CYCLE (EARLY WRITE)

NOTE : DOUT = OPEN

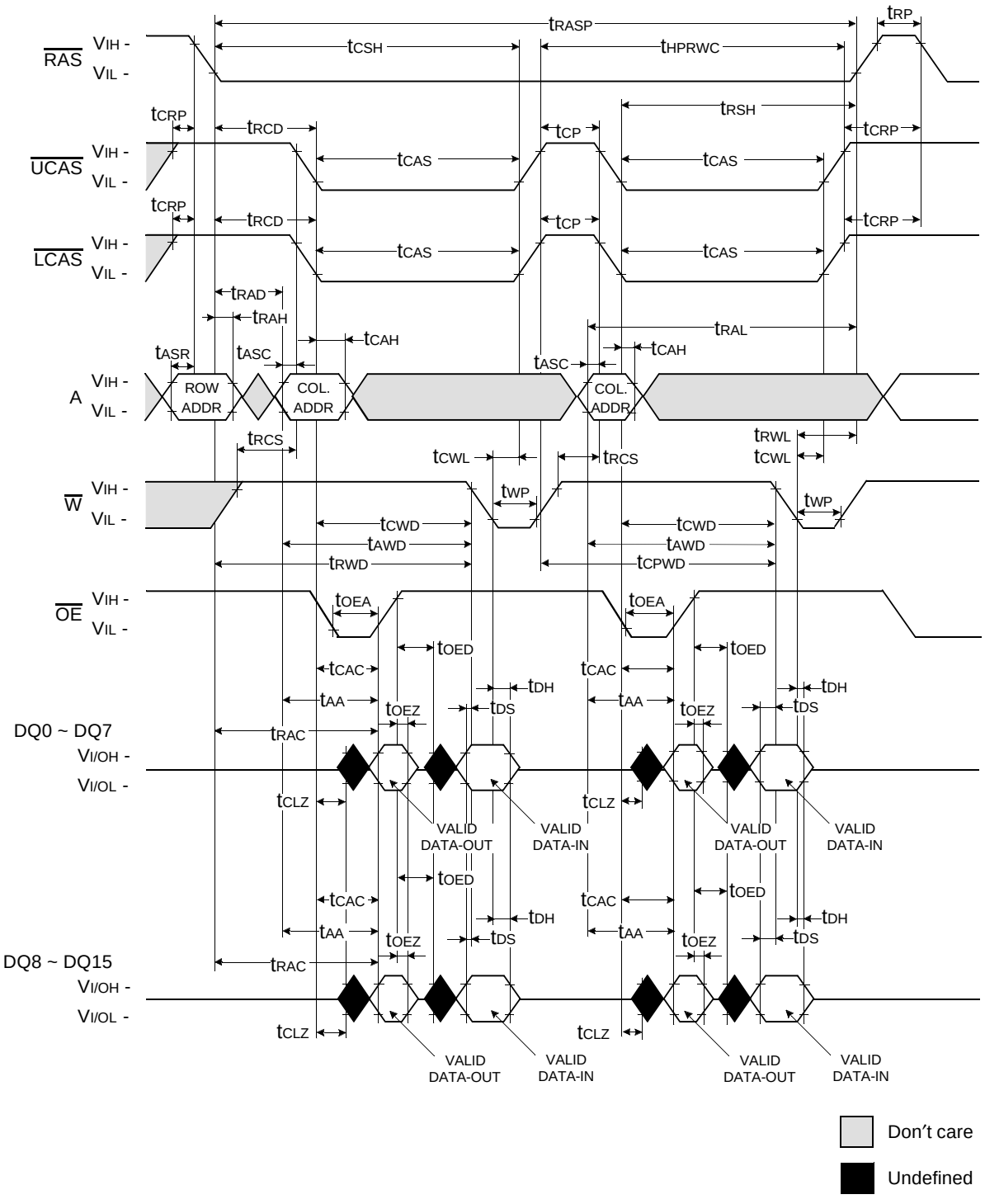


HYPER PAGE MODE UPPER BYTE WRITE CYCLE (EARLY WRITE)

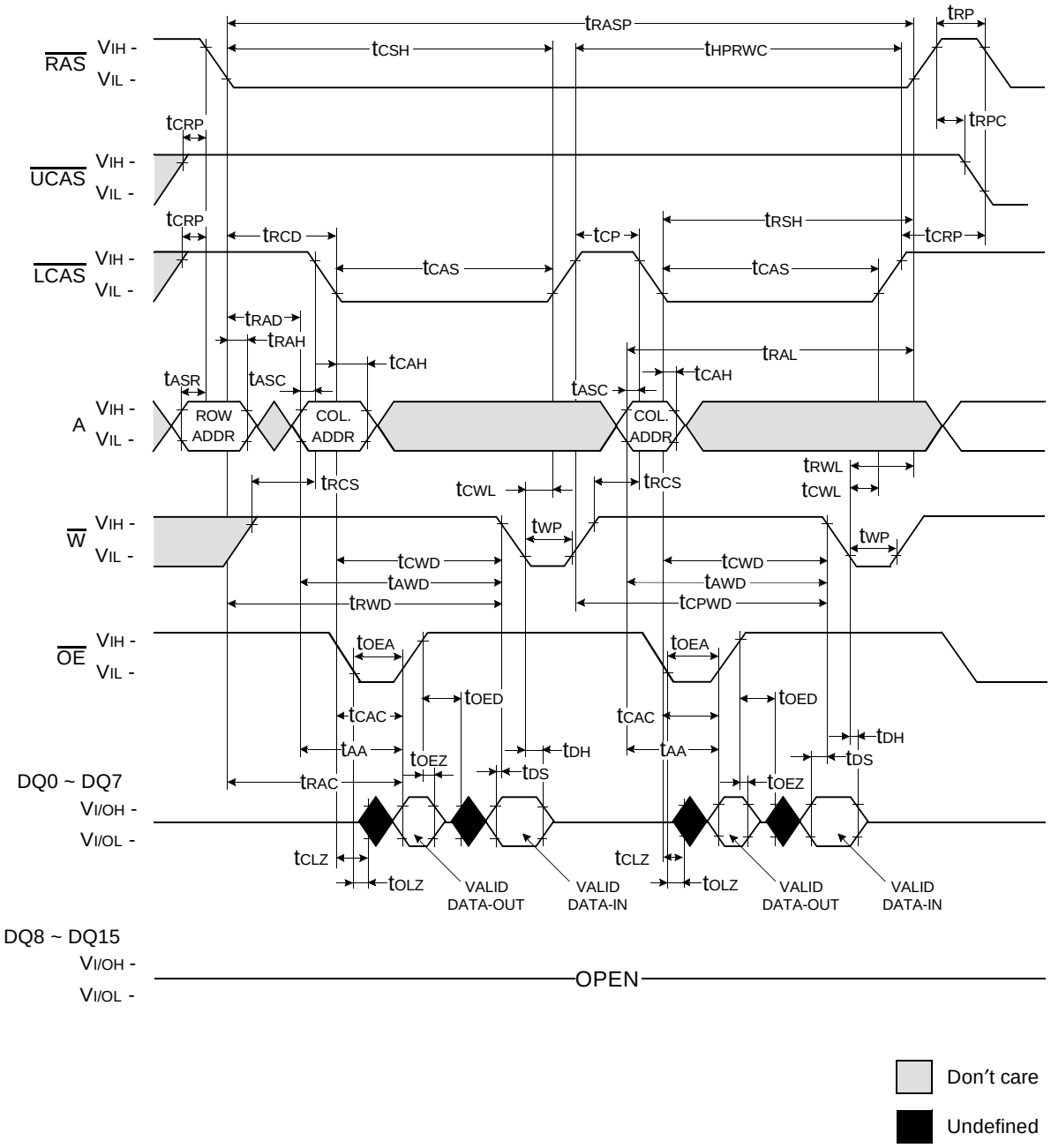
NOTE : DOUT = OPEN



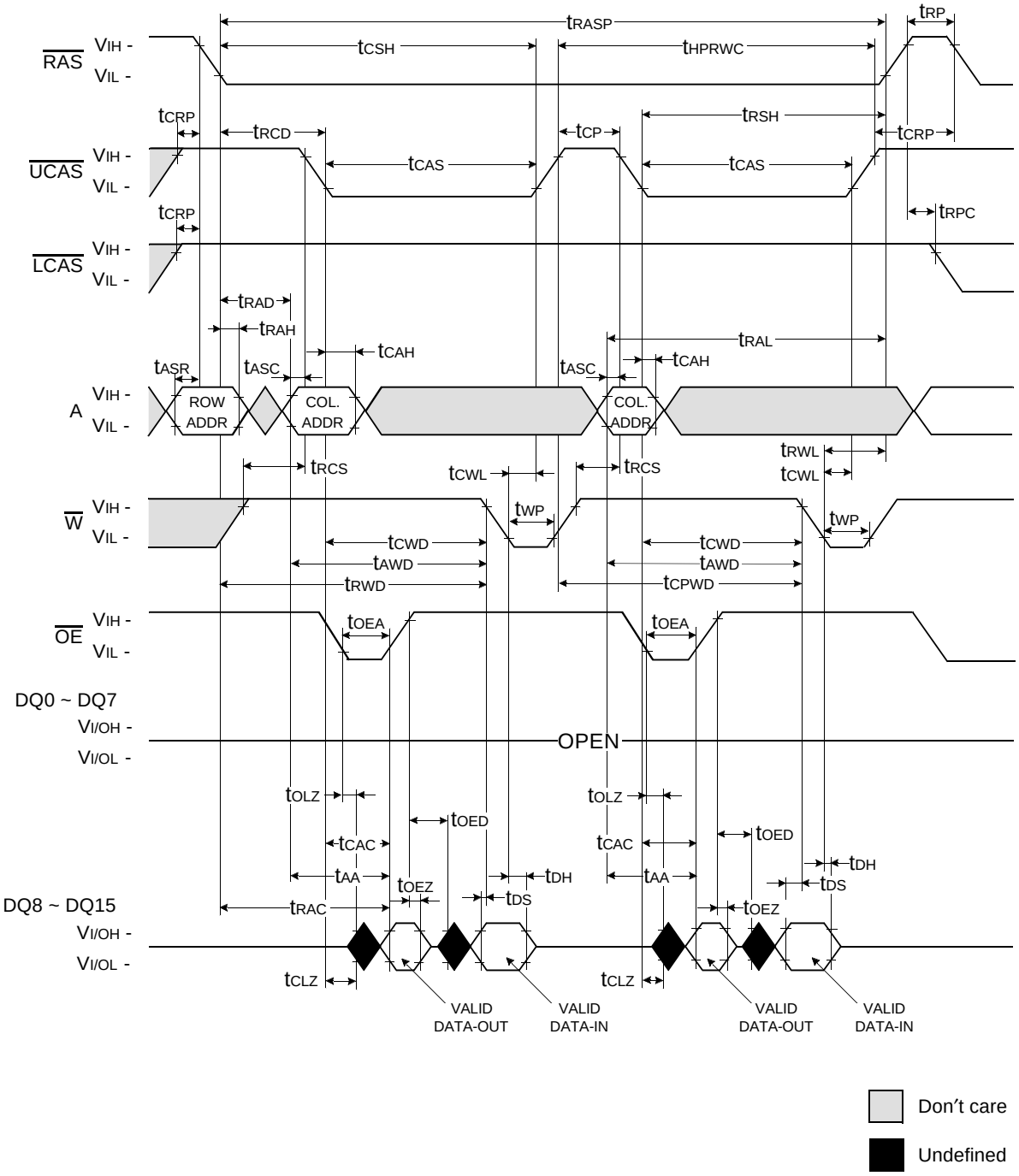
HYPER PAGE MODE WORD READ - MODIFY - WRITE CYCLE



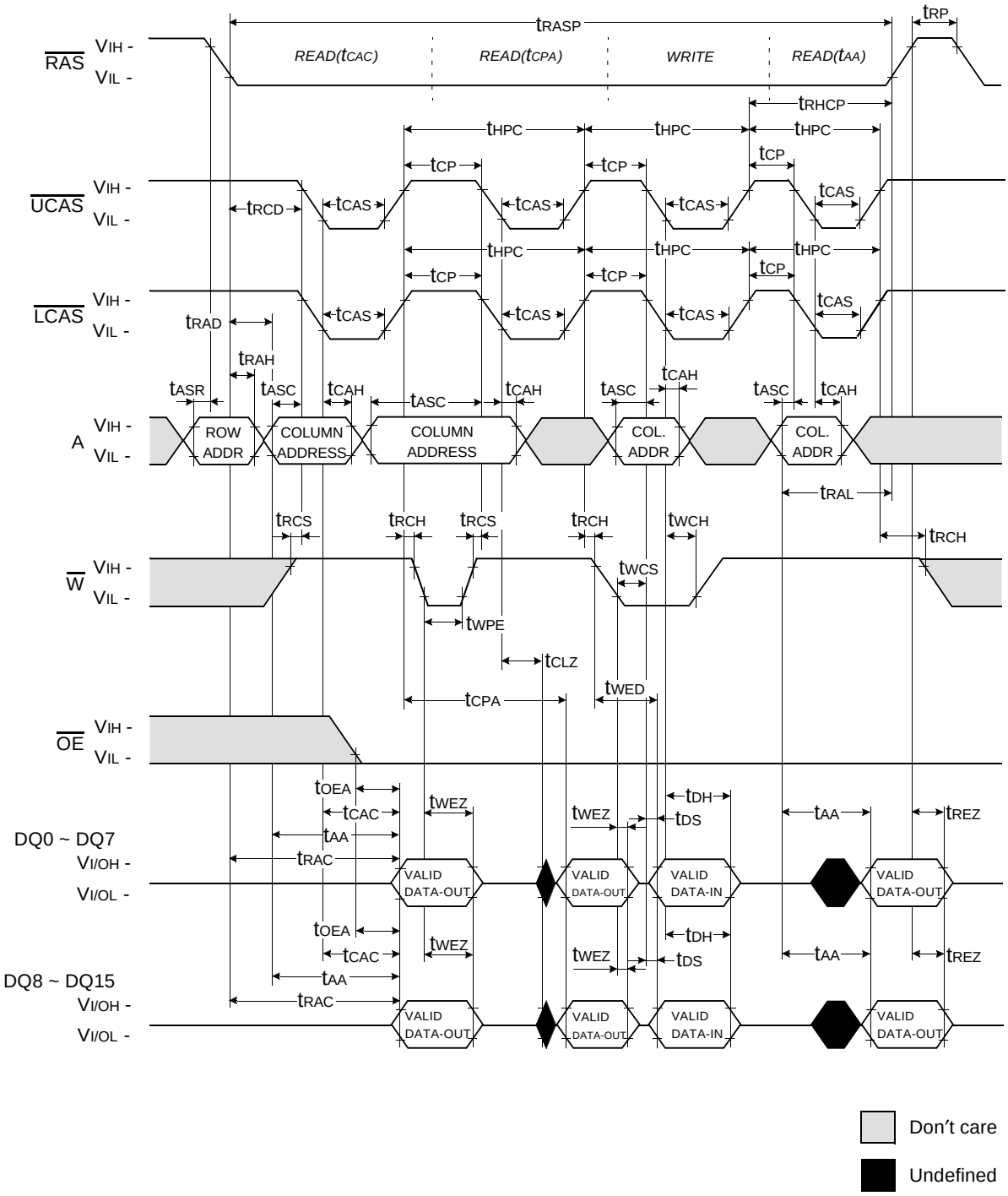
HYPER PAGE MODE LOWER BYTE READ - MODIFY - WRITE CYCLE



HYPER PAGE MODE UPPER BYTE READ - MODIFY - WRITE CYCLE



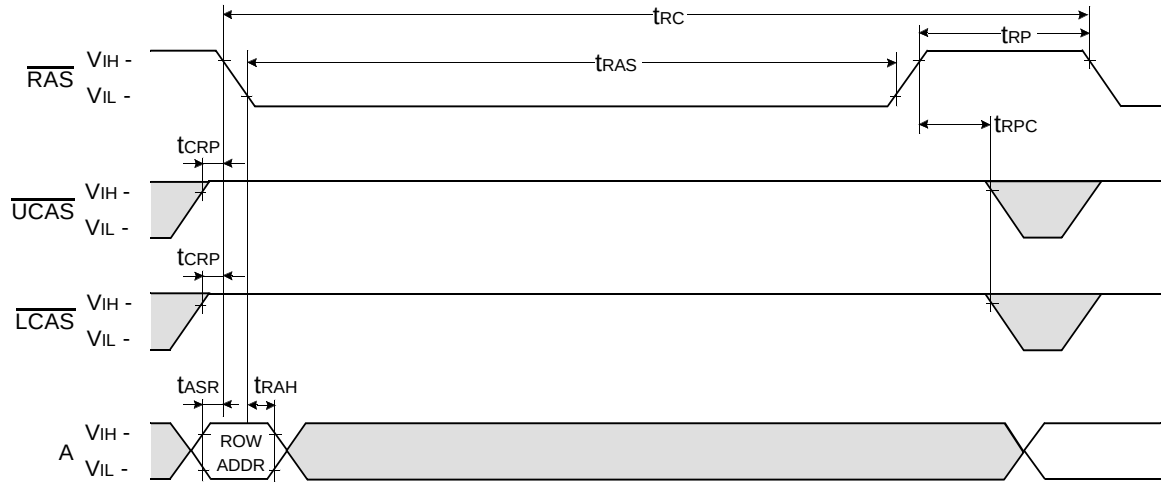
HYPER PAGE READ AND WRITE MIXED CYCLE



$\overline{RAS}$ - ONLY REFRESH CYCLE

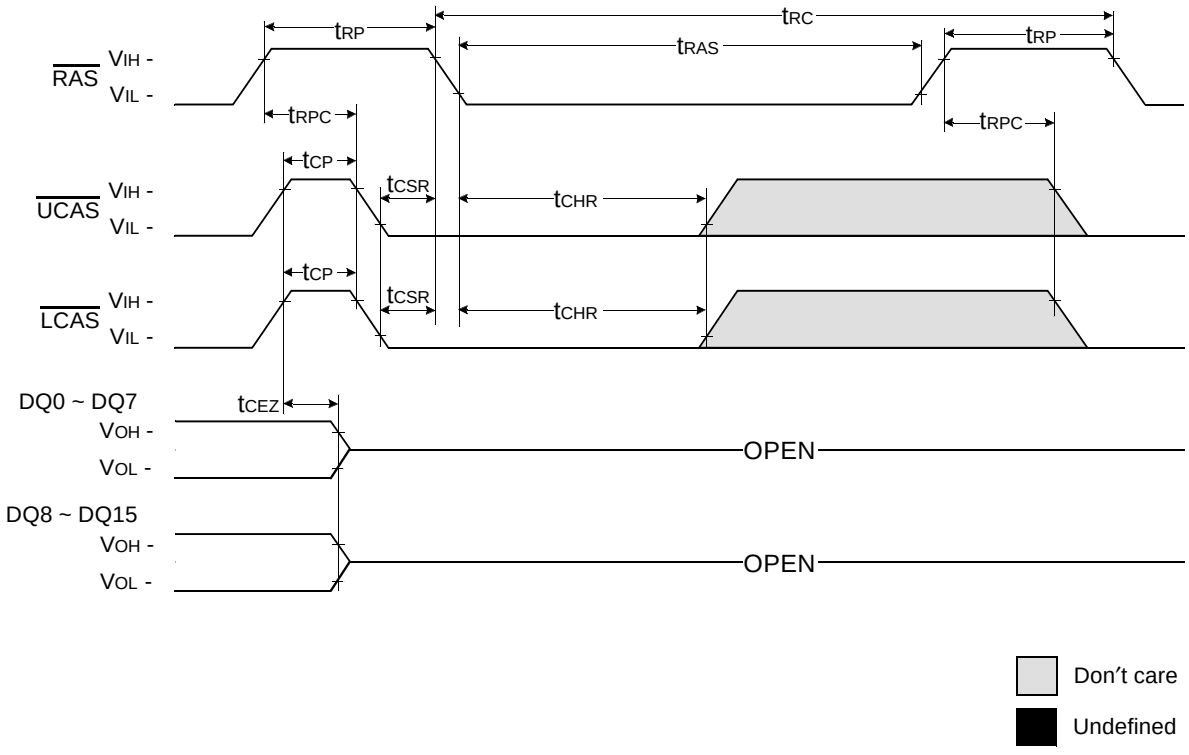
NOTE : $\overline{W}$, $\overline{OE}$, D_{IN} = Don't care

D_{OUT} = OPEN

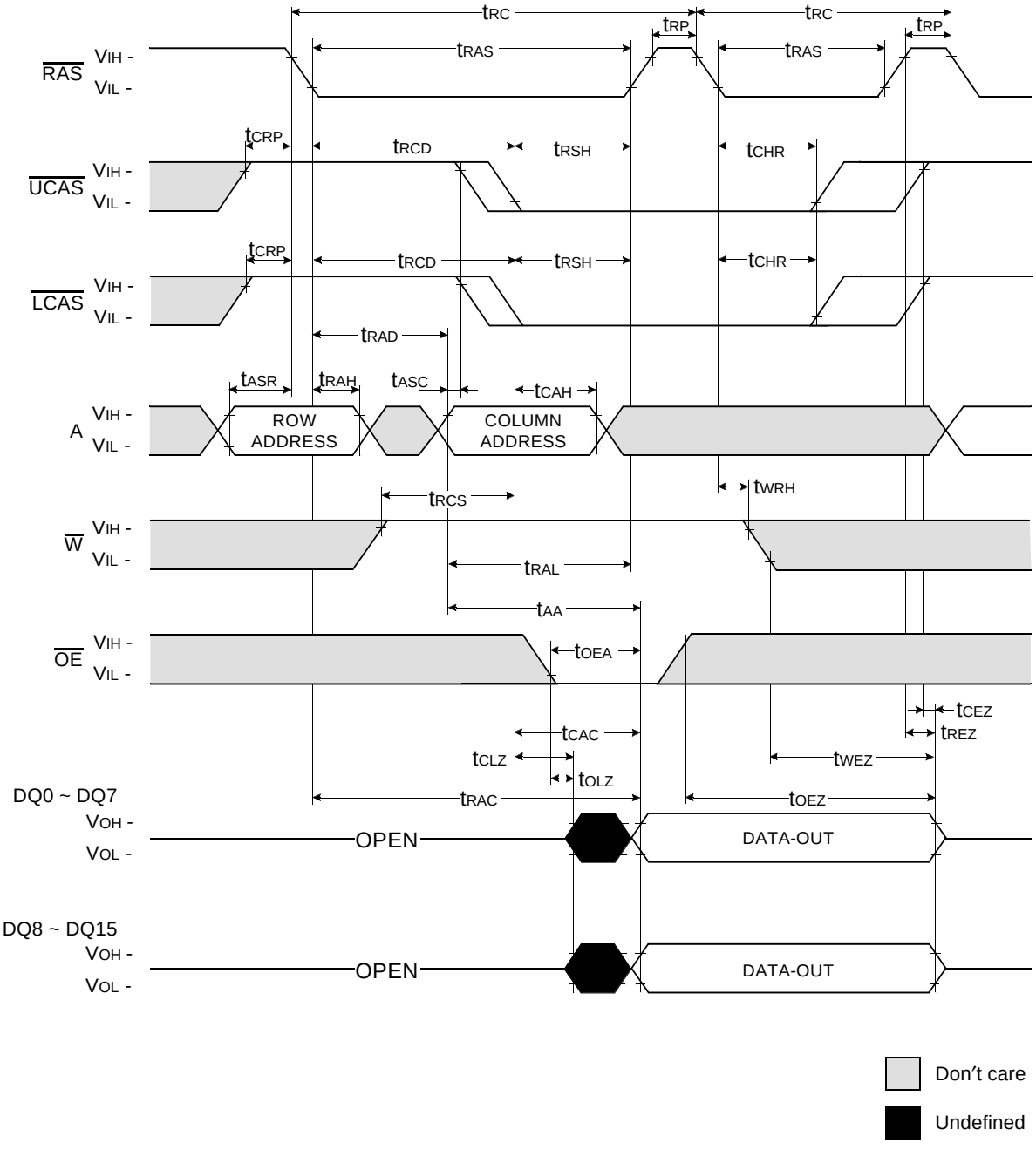


$\overline{CAS}$ - BEFORE - $\overline{RAS}$ REFRESH CYCLE

NOTE : $\overline{OE}$, A = Don't care

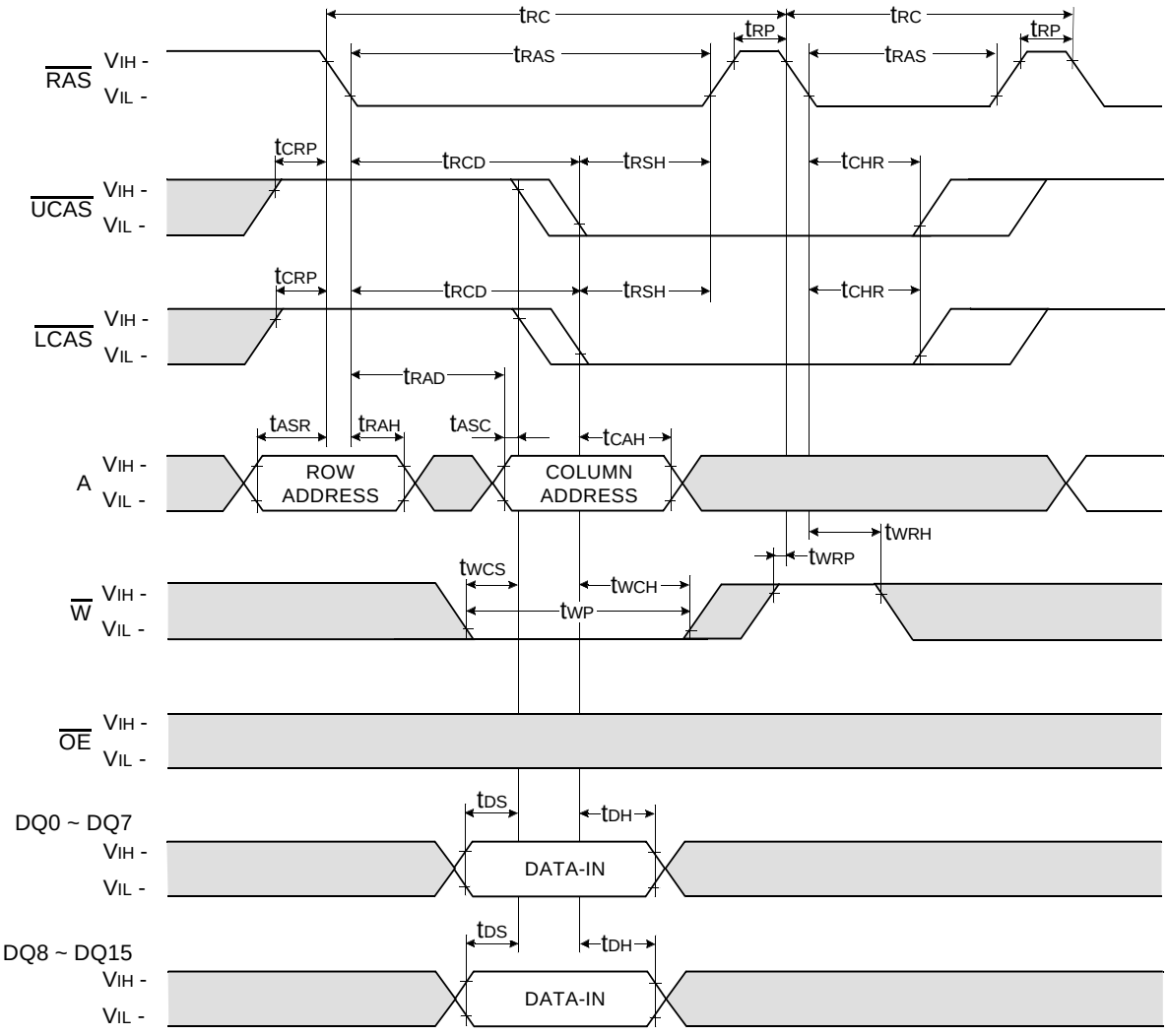


HIDDEN REFRESH CYCLE (READ)

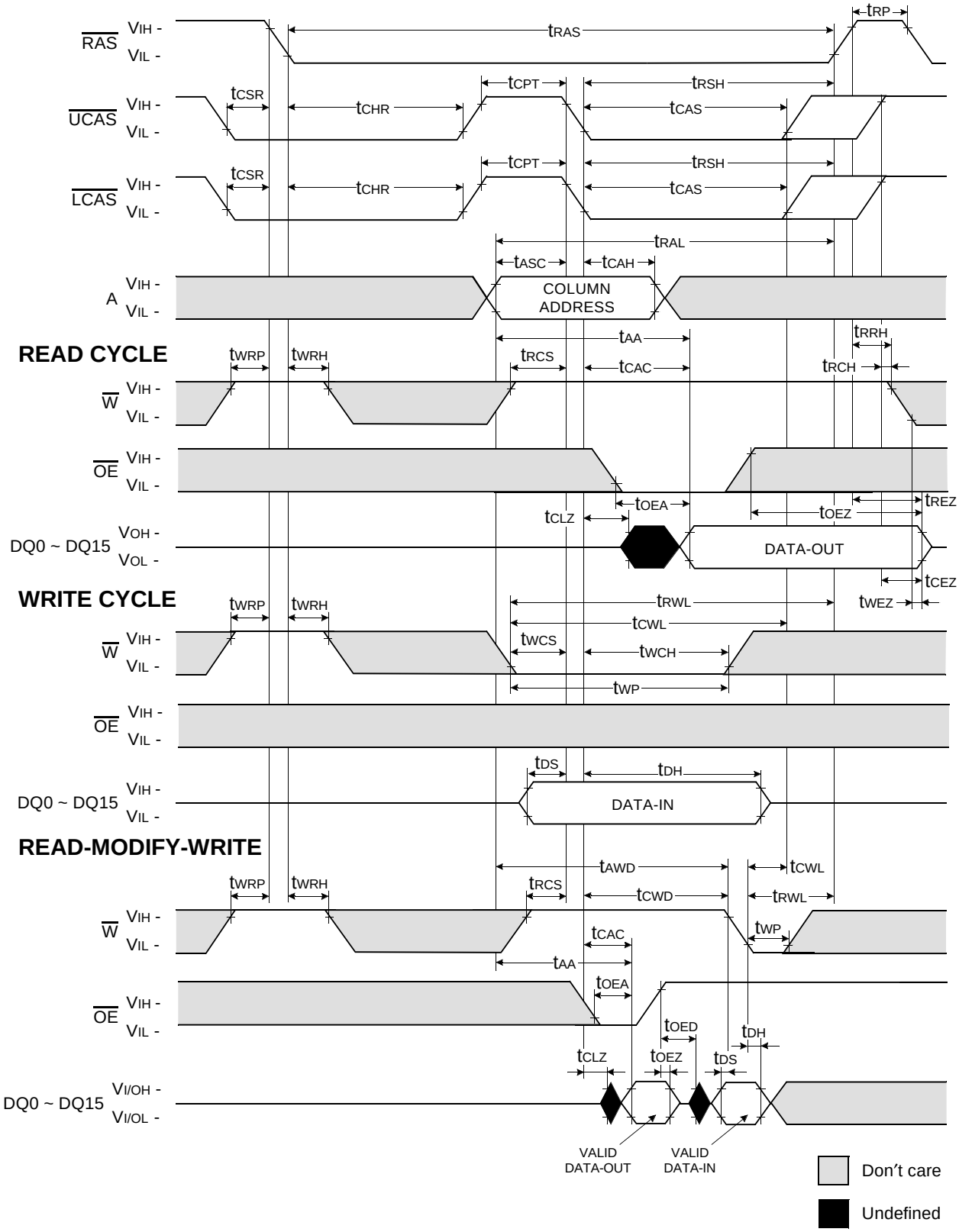


HIDDEN REFRESH CYCLE (WRITE)

NOTE : DOUT = OPEN

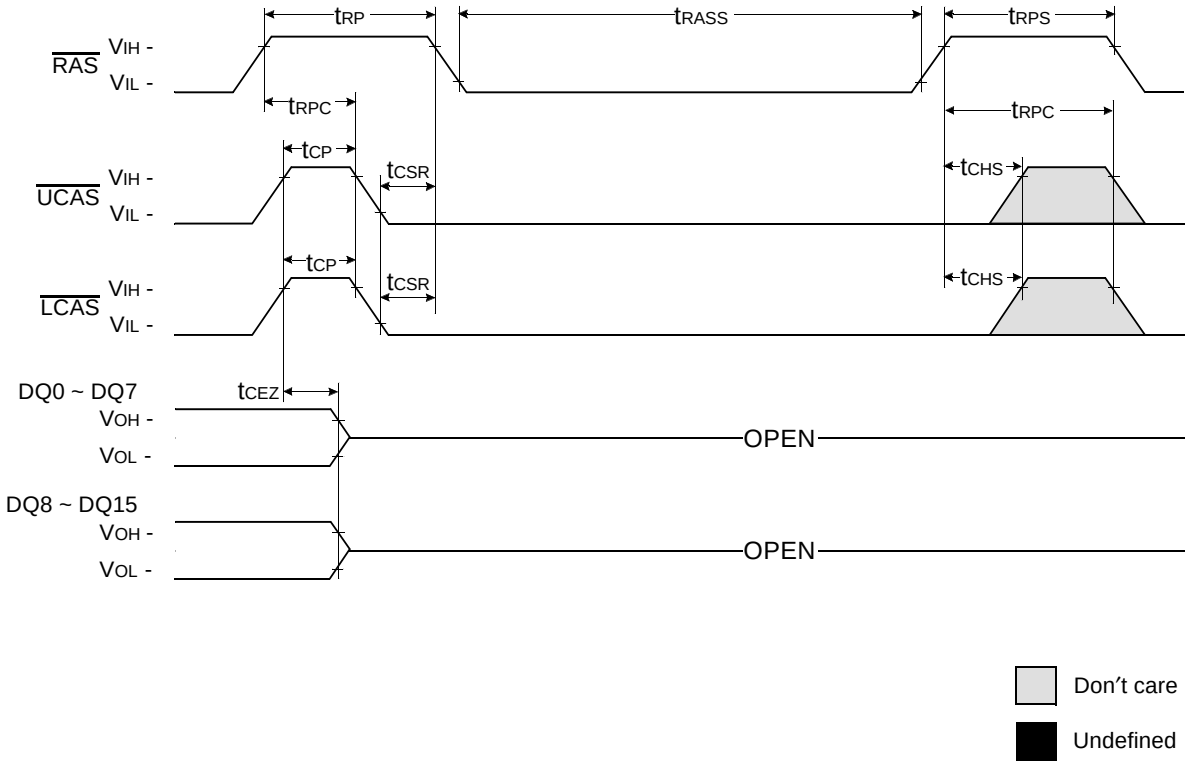


CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



$\overline{CAS}$ - BEFORE - $\overline{RAS}$ SELF REFRESH CYCLE

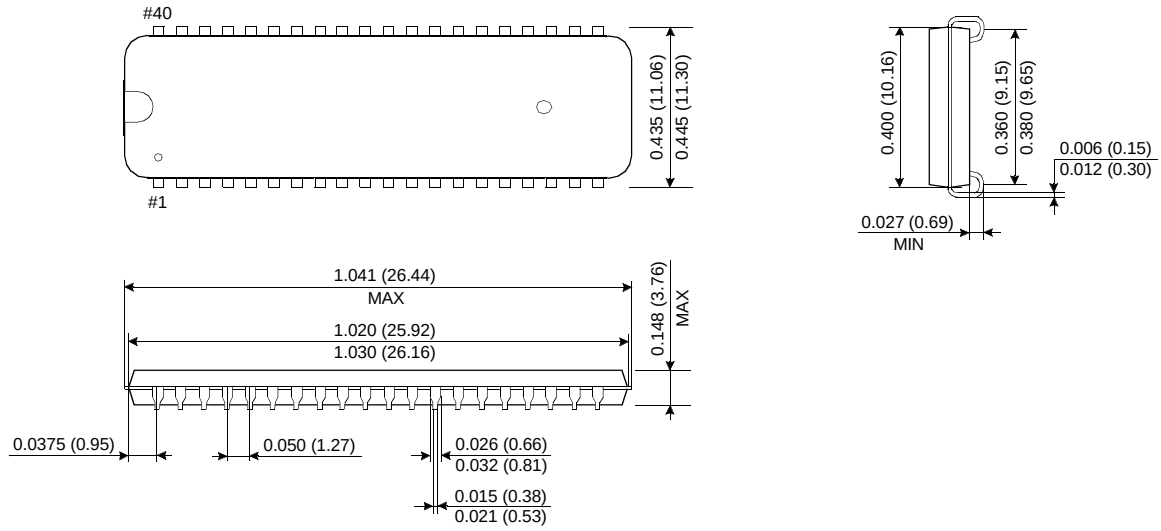
NOTE : $\overline{OE}$, A = Don't care



PACKAGE DIMENSION

40 SOJ 400mil

Units : Inches (millimeters)



44(40) TSOP(II) 400mil

Units : Inches (millimeters)