

*4M x 4Bit CMOS Quad CAS DRAM with Fast Page Mode***DESCRIPTION**

This is a family of 4,194,304 x 4 bit Quad $\overline{\text{CAS}}$ with Fast Page Mode CMOS DRAMs. Fast Page Mode offers high speed random access of memory cells within the same row. Refresh cycle (2K Ref. or 4K Ref.), access time (-50 or -60), power consumption(Normal or Low power) and package type(SOJ or TSOP-II) are optional features of this family. All of this family have $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ -only refresh and Hidden refresh capabilities. Furthermore, Self-refresh operation is available in L-version. Four separate $\overline{\text{CAS}}$ pins provide for separate I/O operation allowing this device to operate in parity mode.

This 4Mx4 Fast Page Mode Quad $\overline{\text{CAS}}$ DRAM family is fabricated using Samsung's advanced CMOS process to realize high bandwidth, low power consumption and high reliability.

FEATURES• **Part Identification**

- K4P170411C-B(F) (5V, 4K Ref.)
- K4P160411C-B(F) (5V, 2K Ref.)

• **Active Power Dissipation**

Unit : mW

Speed	Refresh Cycle	
	4K	2K
-50	495	605
-60	440	550

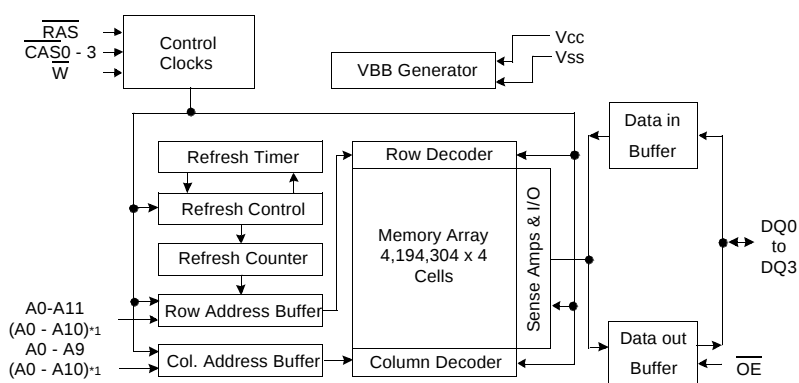
• **Refresh Cycles**

Part NO.	Refresh cycle	Refresh period	
		Normal	L-ver
K4P170411C	4K	64ms	128ms
K4P160411C	2K	32ms	

• **Performance Range**

Speed	t _{RAC}	t _{CAC}	t _{RC}	t _{PC}	Remark
-50	50ns	13ns	90ns	35ns	5V/3.3V
-60	60ns	15ns	110ns	40ns	5V/3.3V

- Fast Page Mode operation
- Four separate $\overline{\text{CAS}}$ pins provide for separate I/O operation
- $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh capability
- $\overline{\text{RAS}}$ -only and Hidden refresh capability
- Self-refresh capability (L-ver only)
- Fast paralleltest mode capability
- TTL compatible inputs and outputs
- Early Write or output enable controlled write
- JEDEC Standard pinout
- Available in Plastic SOJ and TSOP(II) packages
- Single +5V±10% power supply

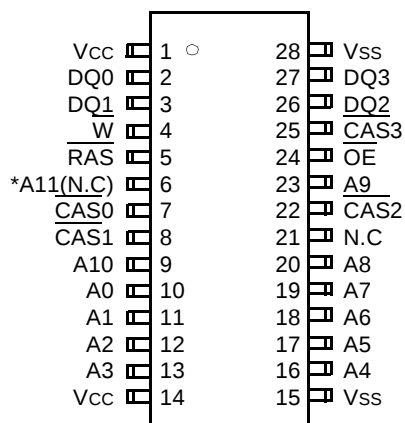
FUNCTIONAL BLOCK DIAGRAM

Note) *1 : 2K Refresh

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PIN CONFIGURATION (Top Views)

- **K4P17(6)0411C-F**



B : 300mil 28 SOJ
F : 300mil 28 TSOP II

Pin Name	Pin Function
A0 - A11	Address Inputs (4K Product)
A0 - A10	Address Inputs (2K Product)
DQ0 - 3	Data In/Out
Vss	Ground
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS0}}-\overline{\text{CAS3}}$	Column Address Strobe
$\overline{\text{W}}$	Read/Write Input
$\overline{\text{OE}}$	Data Output Enable
Vcc	Power(+5.0V)
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on any pin relative to V _{SS}	V _{IN} , V _{OUT}	-1.0 to +7.0	V
Voltage on V _{CC} supply relative to V _{SS}	V _{CC} Inputs	-1.0 to +7.0	V
Storage Temperature	T _{stg}	-55 to +150	°C
Power Dissipation	P _D	1	W
Short Circuit Output Current	I _{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A= 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Units
Supply Voltage	V _{CC}	4.5	5.0	5.5	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.4	-	V _{CC} +1.0 ^{*1}	V
Input Low Voltage	V _{IL}	-1.0 ^{*2}	-	0.8	V

*1 : V_{CC}+2.0V/20ns, Pulse width is measured at V_{CC}

*2 : -2.0/20ns, Pulse width is measured at V_{SS}

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Units
Input Leakage Current (Any input 0≤V _{IN} ≤V _{IN} +0.5V, all other input pins not under test=0 Volt)	I _{I(L)}	-5	5	μA
Output Leakage Current (Data out is disabled, 0V≤V _{OUT} ≤V _{CC})	I _{O(L)}	-5	5	μA
Output High Voltage Level(I _{OH} =-5mA)	V _{OH}	2.4	-	V
Output Low Voltage Level(I _{OL} =4.2mA)	V _{OL}	-	0.4	V

DC AND OPERATING CHARACTERISTICS (Continued)

Symbol	Power	Speed	Max		Units
			K4P170411C	K4P160411C	
I _{CC1}	Don't care	-50 -60	90 80	110 100	mA mA mA
I _{CC2}	Normal L	Don't care	2 1	2 1	mA mA
I _{CC3}	Don't care	-50 -60	90 80	110 100	mA mA mA
I _{CC4}	Don't care	-50 -60	80 70	90 80	mA mA mA
I _{CC5}	Normal L	Don't care	1 250	1 250	mA uA
I _{CC6}	Don't care	-50 -60	90 80	110 100	mA mA mA
I _{CC7}	L	Don't care	300	300	uA
I _{CCS}	L	Don't care	250	250	uA

I_{CC1}* : Operating Current ($\overline{\text{RAS}}$ and $\overline{\text{CAS}}$, Address cycling @ $t_{\text{RC}}=\text{min.}$)

I_{CC2} : Standby Current ($\overline{\text{RAS}}=\overline{\text{CAS}}=\overline{\text{W}}=V_{\text{IH}}$)

I_{CC3}* : RAS-only Refresh Current ($\overline{\text{CAS}}=V_{\text{IH}}$, $\overline{\text{RAS}}$, Address cycling @ $t_{\text{RC}}=\text{min.}$)

I_{CC4}* : Fast Page Mode Current ($\overline{\text{RAS}}=V_{\text{IL}}$, $\overline{\text{CAS}}$, Address cycling @ $t_{\text{PC}}=\text{min.}$)

I_{CC5} : Standby Current ($\overline{\text{RAS}}=\overline{\text{CAS}}=\overline{\text{W}}=V_{\text{CC}}-0.2\text{V}$)

I_{CC6}* : CAS-Before-RAS Refresh Current ($\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ cycling @ $t_{\text{RC}}=\text{min.}$)

I_{CC7} : Battery back-up current, Average power supply current, Battery back-up mode

Input high voltage(V_{IH})= $V_{\text{CC}}-0.2\text{V}$, Input low voltage(V_{IL})= 0.2V , $\overline{\text{CAS}}=0.2\text{V}$,

DQ=Don't care, $T_{\text{RC}}=31.25\mu\text{s}$ (4K/L-ver), $62.5\mu\text{s}$ (2K/L-ver), $T_{\text{RAS}}=T_{\text{RASmin}}\sim 300\text{ns}$

I_{CCS} : Self Refresh Current

$\overline{\text{RAS}}=\overline{\text{CAS}}=0.2\text{V}$, $\overline{\text{W}}=\overline{\text{OE}}=\text{A0} \sim \text{A11}=V_{\text{CC}}-0.2\text{V}$ or 0.2V ,

DQ0 ~ DQ3= $V_{\text{CC}}-0.2\text{V}$, 0.2V or Open

***Note** : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1}, I_{CC3} and I_{CC6} address can be changed maximum once while $\overline{\text{RAS}}=V_{\text{IL}}$. In I_{CC4}, address can be changed maximum once within one fast page mode cycle time, t_{PC} .

K4P170411C, K4P160411C

CMOS DRAM

CAPACITANCE (TA=25°C, VCC=5V, f=1MHz)

Parameter	Symbol	Min	Max	Units
Input capacitance [A0 ~ A11]	CIN1	-	5	pF
Input capacitance [$\overline{\text{RAS}}$, $\overline{\text{CASx}}$, $\overline{\text{W}}$, $\overline{\text{OE}}$]	CIN2	-	7	pF
Output capacitance [DQ0 - DQ3]	CDQ	-	7	pF

AC CHARACTERISTICS (0°C≤TA≤70°C, See note 1,2)

Test condition : VCC=5.0V±10%, VIH/VIL=2.4/0.8V, VOH/VOL=2.4/0.4V

Parameter	Symbol	-50		-60		Units	Notes
		Min	Max	Min	Max		
Random read or write cycle time	t _{RC}	90		110		ns	
Read-modify-write cycle time	t _{RWC}	133		155		ns	
Access time from $\overline{\text{RAS}}$	t _{RAC}		50		60	ns	3,4,10
Access time from $\overline{\text{CAS}}$	t _{CAC}		13		15	ns	3,4,5,18
Access time from column address	t _{AA}		25		30	ns	3,10
$\overline{\text{CAS}}$ to output in Low-Z	t _{CLZ}	0		0		ns	3,18
Output buffer turn-off delay	t _{OFF}	0	13	0	15	ns	6
Transition time (rise and fall)	t _T	3	50	3	50	ns	2
$\overline{\text{RAS}}$ precharge time	t _{RP}	30		40		ns	
$\overline{\text{RAS}}$ pulse width	t _{RAS}	50	10K	60	10K	ns	
$\overline{\text{RAS}}$ hold time	t _{RSH}	13		15		ns	14
$\overline{\text{CAS}}$ hold time	t _{CSH}	50		60		ns	17
$\overline{\text{CAS}}$ pulse width	t _{CAS}	13	10K	15	10K	ns	23
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	t _{RCD}	20	37	20	45	ns	4,16
$\overline{\text{RAS}}$ to column address delay time	t _{RAD}	15	25	15	30	ns	10
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	t _{CRP}	5		5		ns	15
Row address set-up time	t _{ASR}	0		0		ns	
Row address hold time	t _{RAH}	10		10		ns	
Column address set-up time	t _{ASC}	0		0		ns	16
Column address hold time	t _{CAH}	10		10		ns	16
Column address to $\overline{\text{RAS}}$ lead time	t _{RAL}	25		30		ns	
Read command set-up time	t _{RCS}	0		0		ns	
Read command hold time referenced to	t _{RCH}	0		0		ns	8,15
Read command hold time referenced to	t _{RRH}	0		0		ns	8
Write command hold time	t _{WCH}	10		10		ns	14
Write command pulse width	t _{WP}	10		10		ns	
Write command to $\overline{\text{RAS}}$ lead time	t _{RWL}	13		15		ns	
Write command to $\overline{\text{CAS}}$ lead time	t _{CWL}	13		15		ns	17

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-50		-60		Units	Notes
		Min	Max	Min	Max		
Data set-up time	tDS	0		0		ns	9
Data hold time	tDH	10		10		ns	9
Refresh period (2K, Normal)	tREF		32		32	ms	
Refresh period (4K, Normal)	tREF		64		64	ms	
Refresh period (L-ver)	tREF		128		128	ms	
Write command set-up time	tWCS	0		0		ns	7,16
CAS to $\overline{W}$ delay time	tCWD	36		40		ns	7,14
RAS to $\overline{W}$ delay time	tRWD	73		85		ns	7
Column address to $\overline{W}$ delay time	tAWD	48		55		ns	7
CAS precharge to $\overline{W}$ delay time	tCPWD	53		60		ns	7
CAS set-up time (CAS -before-RAS refresh)	tCSR	5		5		ns	16
CAS hold time (CAS -before-RAS refresh)	tCHR	10		10		ns	15
RAS to CAS precharge time	tRPC	5		5		ns	16
Access time from CAS precharge	tCPA		30		35	ns	3,15
Fast Page mode cycle time	tPC	35		40		ns	19
Fast Page read-modify-write cycle time	tPRWC	76		85		ns	19
CAS precharge time (Fast Page cycle)	tCP	10		10		ns	20
RAS pulse width (Fast Page cycle)	tRASP	50	200K	60	200K	ns	
RAS hold time from CAS precharge	tRHCP	30		35		ns	
$\overline{OE}$ access time	tOEA		13		15	ns	21
$\overline{OE}$ to data delay	tOED	13		15		ns	22
Output buffer turn off delay time from $\overline{OE}$	tOEZ	0	13	0	15	ns	6
$\overline{OE}$ command hold time	tOEH	13		15		ns	
Write command set-up time (Test mode in)	tWTS	10		10		ns	11
Write command hold time (Test mode in)	tWTH	10		10		ns	11
$\overline{W}$ to RAS precharge time($\overline{C}$ -B- $\overline{R}$ refresh)	tWRP	10		10		ns	
$\overline{W}$ to RAS hold time($\overline{C}$ -B- $\overline{R}$ refresh)	tWRH	10		10		ns	
RAS pulse width ($\overline{C}$ -B- $\overline{R}$ self refresh)	tRASS	100		100		us	25,26,27
RAS precharge time ($\overline{C}$ -B- $\overline{R}$ self refresh)	tRPS	90		110		ns	25,26,27
CAS hold time ($\overline{C}$ -B- $\overline{R}$ self refresh)	tCHS	-50		-50		ns	25,26,27
Hold time CAS low to CAS high	tCLCH	5		5		ns	13,24

TEST MODE CYCLE

(Note 11)

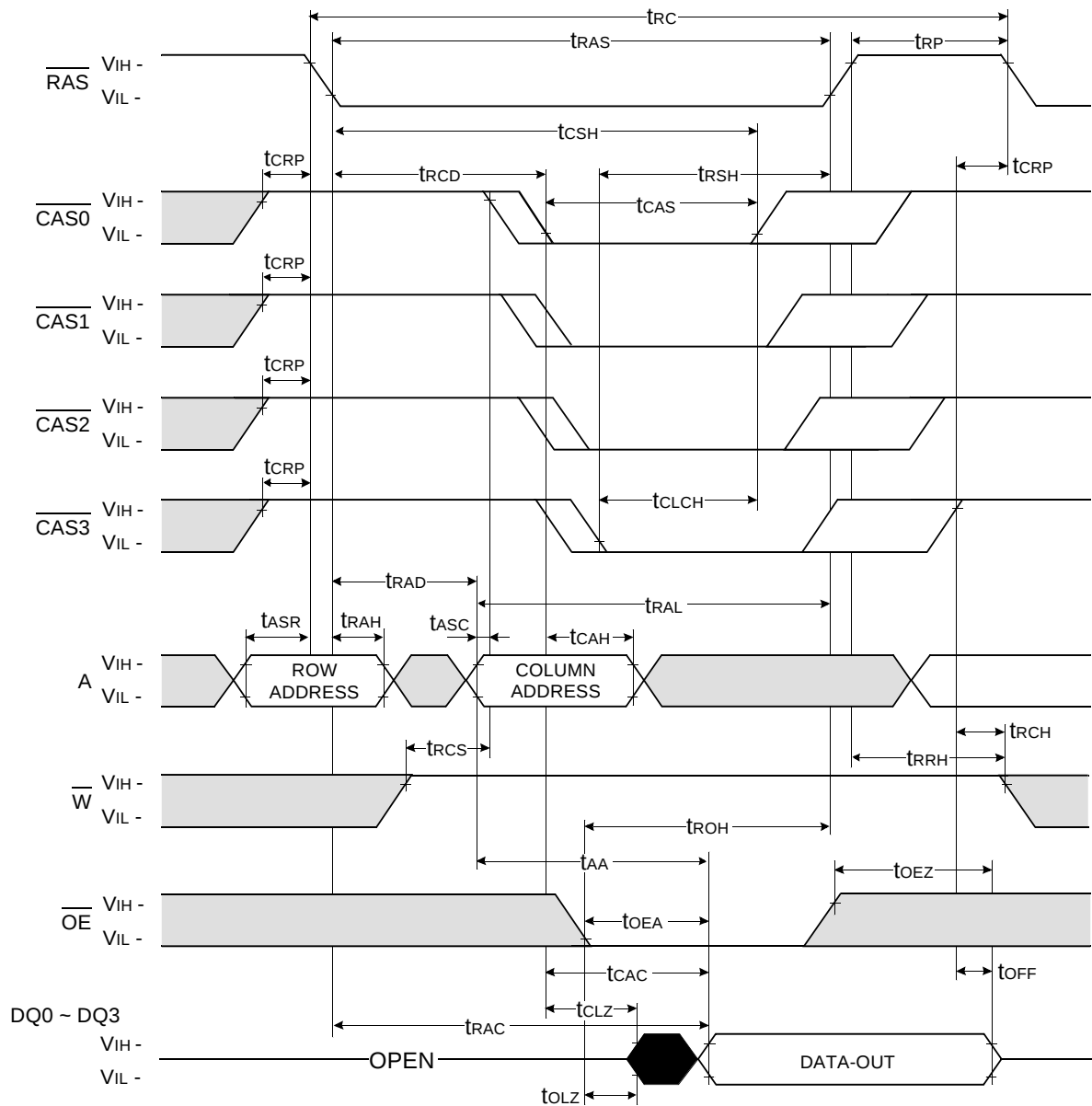
Parameter	Symbol	-50		-60		Units	Notes
		Min	Max	Min	Max		
Random read or write cycle time	t _{RC}	95		115		ns	
Read-modify-write cycle time	t _{RWC}	138		160		ns	
Access time from $\overline{\text{RAS}}$	t _{RAC}		55		65	ns	3,4,10,12
Access time from $\overline{\text{CAS}}$	t _{CAC}		18		20	ns	3,4,5,12
Access time from column address	t _{AA}		30		35	ns	3,10,12
$\overline{\text{RAS}}$ pulse width	t _{RAS}	55	10K	65	10K	ns	
$\overline{\text{CAS}}$ pulse width	t _{CAS}	18	10K	20	10K	ns	
$\overline{\text{RAS}}$ hold time	t _{RSH}	18		20		ns	
$\overline{\text{CAS}}$ hold time	t _{CSH}	55		65		ns	
Column address to $\overline{\text{RAS}}$ lead time	t _{RAL}	30		35		ns	
$\overline{\text{CAS}}$ to $\overline{\text{W}}$ delay time	t _{CWD}	41		45		ns	7
$\overline{\text{RAS}}$ to $\overline{\text{W}}$ delay time	t _{RWD}	78		90		ns	7
Column address to $\overline{\text{W}}$ delay time	t _{AWD}	53		60		ns	7
$\overline{\text{CAS}}$ precharge to $\overline{\text{W}}$ delay time	t _{CPWD}	58		65		ns	7
Fast Page mode cycle time	t _{PC}	40		45		ns	
Fast Page read-modify-write cycle time	t _{PRWC}	81		90		ns	
$\overline{\text{RAS}}$ pulse width (Fast Page cycle)	t _{RASP}	55	200K	65	200K	ns	
Access time from $\overline{\text{CAS}}$ precharge	t _{CPA}		35		40	ns	3
$\overline{\text{OE}}$ access time	t _{OEa}		18		20	ns	
$\overline{\text{OE}}$ to data delay	t _{OEaD}	18		20		ns	
$\overline{\text{OE}}$ command hold time	t _{OEh}	18		20		ns	

NOTES

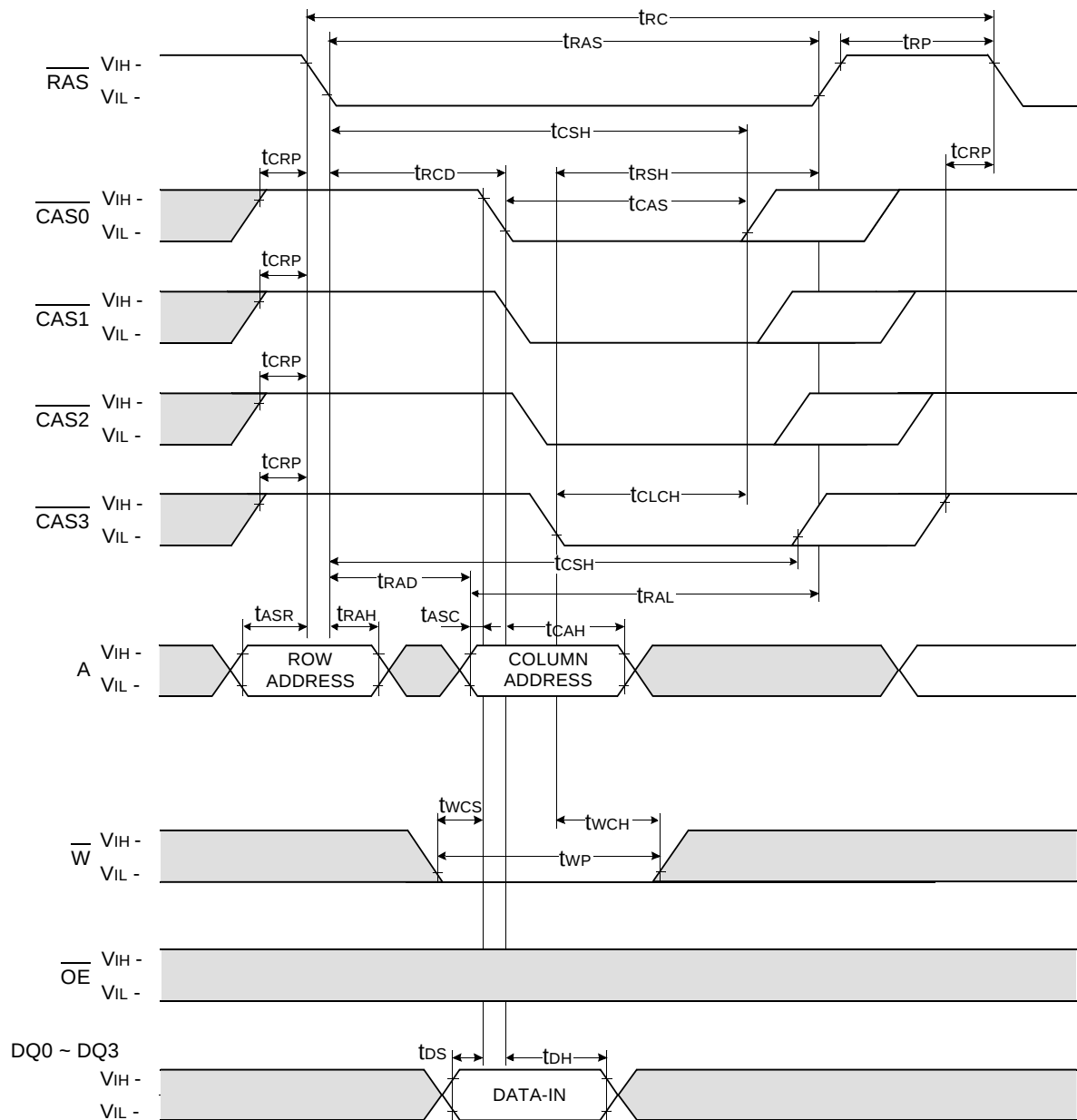
1. An initial pause of 200us is required after power-up followed by any 8 $\overline{\text{RAS}}$ -only refresh or $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycles before proper device operation is achieved.
2. $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ are reference levels for measuring timing of input signals.
Transition times are measured between $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the $t_{\text{RCD}}(\text{max})$ limit insures that $t_{\text{RAC}}(\text{max})$ can be met. $t_{\text{RCD}}(\text{max})$ is specified as a reference point only.
If t_{RCD} is greater than the specified $t_{\text{RCD}}(\text{max})$ limit, then access time is controlled exclusively by t_{CAC} .
5. Assumes that $t_{\text{RCD}} \geq t_{\text{RCD}}(\text{max})$.
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL} .
7. t_{WCS} , t_{RWD} , t_{CWD} , t_{AWD} and t_{CPWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{\text{WCS}} \geq t_{\text{WCS}}(\text{min})$, the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{\text{CWD}} \geq t_{\text{CWD}}(\text{min})$, $t_{\text{RWD}} \geq t_{\text{RWD}}(\text{min})$, $t_{\text{AWD}} \geq t_{\text{AWD}}(\text{min})$ and $t_{\text{CPWD}} \geq t_{\text{CPWD}}(\text{min})$, then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. t_{RCH} and t_{RRH} must be satisfied for a read cycle.
9. These parameters are referenced to the first $\overline{\text{CAS}}$ falling edge in early write cycles and to $\overline{\text{W}}$ falling edge in $\overline{\text{OE}}$ controlled write cycle and read-modify-write cycles.
10. Operation within the $t_{\text{RAD}}(\text{max})$ limit insures that $t_{\text{RAC}}(\text{max})$ can be met. $t_{\text{RAD}}(\text{max})$ is specified as a reference point only.
If t_{RAD} is greater than the specified $t_{\text{RAD}}(\text{max})$ limit, then access time is controlled by t_{AA} .
11. These specifications are applied in the test mode.
12. In test mode read cycle, the values of t_{RAC} , t_{AA} and t_{CAC} are delayed by 2ns to 5ns for the specified values. These parameters should be specified in test mode cycles by adding 5ns to the specified value in this data sheet.
13. In order to hold the address latched by the first $\overline{\text{CAS}}$ going low, the parameter t_{CLCH} must be met.
14. The last $\overline{\text{CASx}}$ edge to go low.
15. The last $\overline{\text{CASx}}$ edge to go high.
16. The first $\overline{\text{CASx}}$ edge to go low.
17. The first $\overline{\text{CASx}}$ edge to go high.
18. Output parameter is referenced to corresponding $\overline{\text{CASx}}$ input.
19. The last rising $\overline{\text{CASx}}$ edge to next cycle's last rising $\overline{\text{CASx}}$ edge.
20. The last rising $\overline{\text{CASx}}$ edge to first falling $\overline{\text{CASx}}$ edge.
21. The first DQx controlled by the first $\overline{\text{CASx}}$ to go low.
22. The last DQx controlled by the last $\overline{\text{CASx}}$ to go high.
23. Each $\overline{\text{CASx}}$ must meet minimum pulse width.
24. The last falling $\overline{\text{CASx}}$ edge to the first rising $\overline{\text{CASx}}$ edge.
25. If $t_{\text{RASS}} \geq 100\mu\text{s}$, then $\overline{\text{RAS}}$ precharge time must use t_{RPS} instead of t_{RP} .
26. For $\overline{\text{RAS}}$ -only refresh and burst $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh mode, 4096(4K)/2048(2K) cycles of burst refresh must be executed within 64ms/32ms before and after self refresh, in order to meet refresh specification.
27. For distributed $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ with 15.6us interval, $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh should be executed with in 15.6us immediately before and after self refresh in order to meet refresh specification.

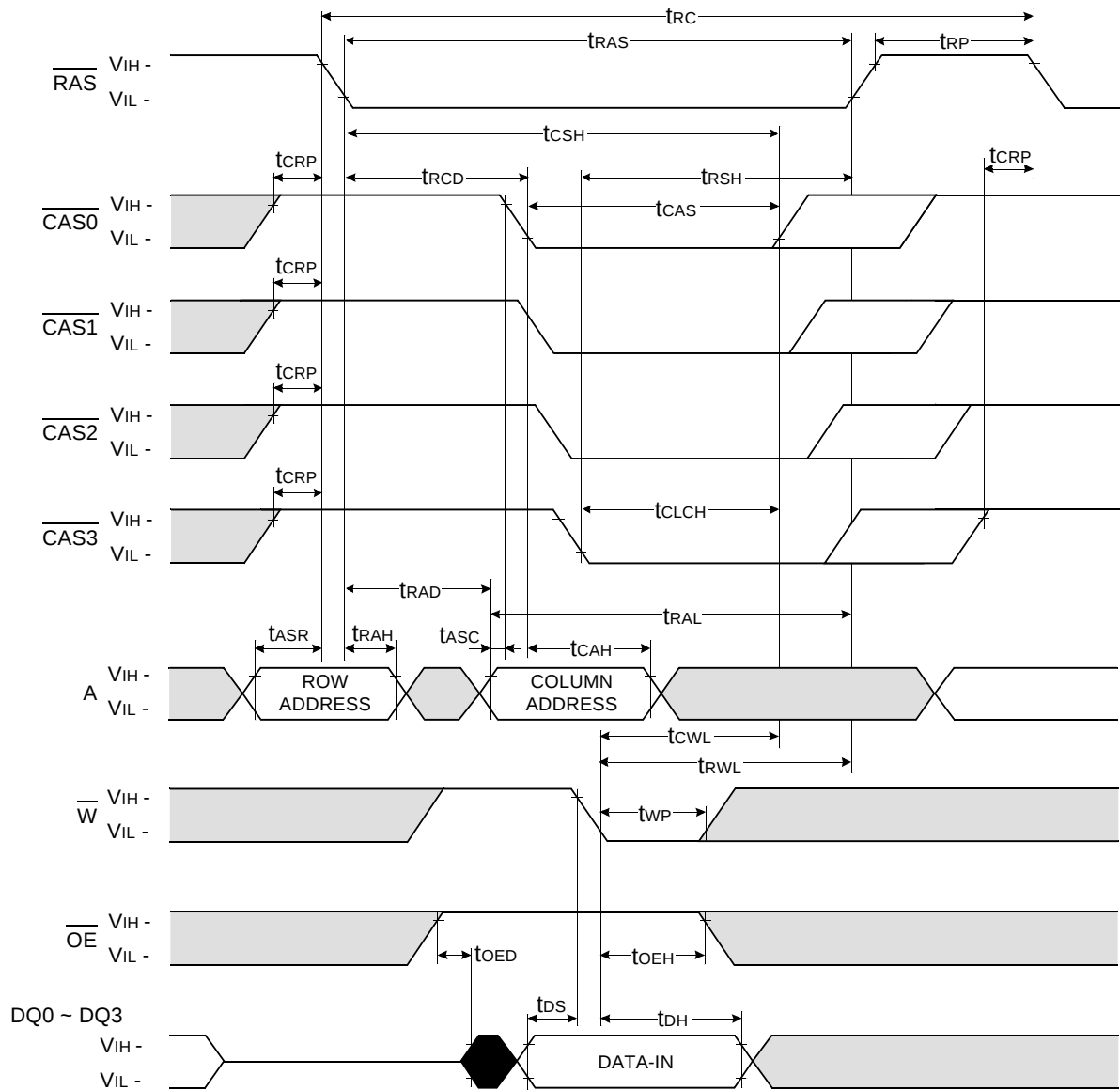
READ CYCLE

NOTE : DOUT = OPEN

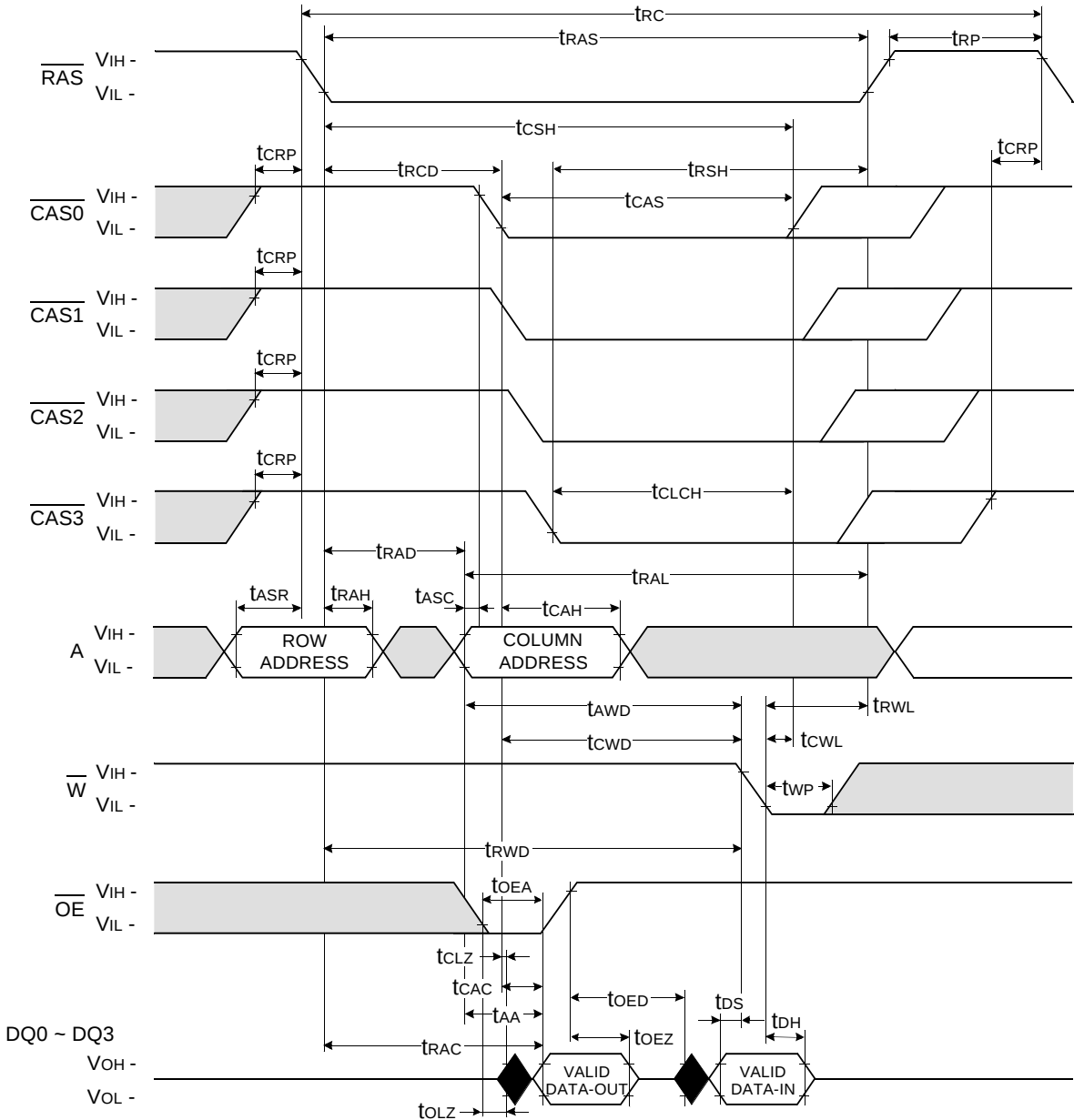


WRITE CYCLE (EARLY WRITE)



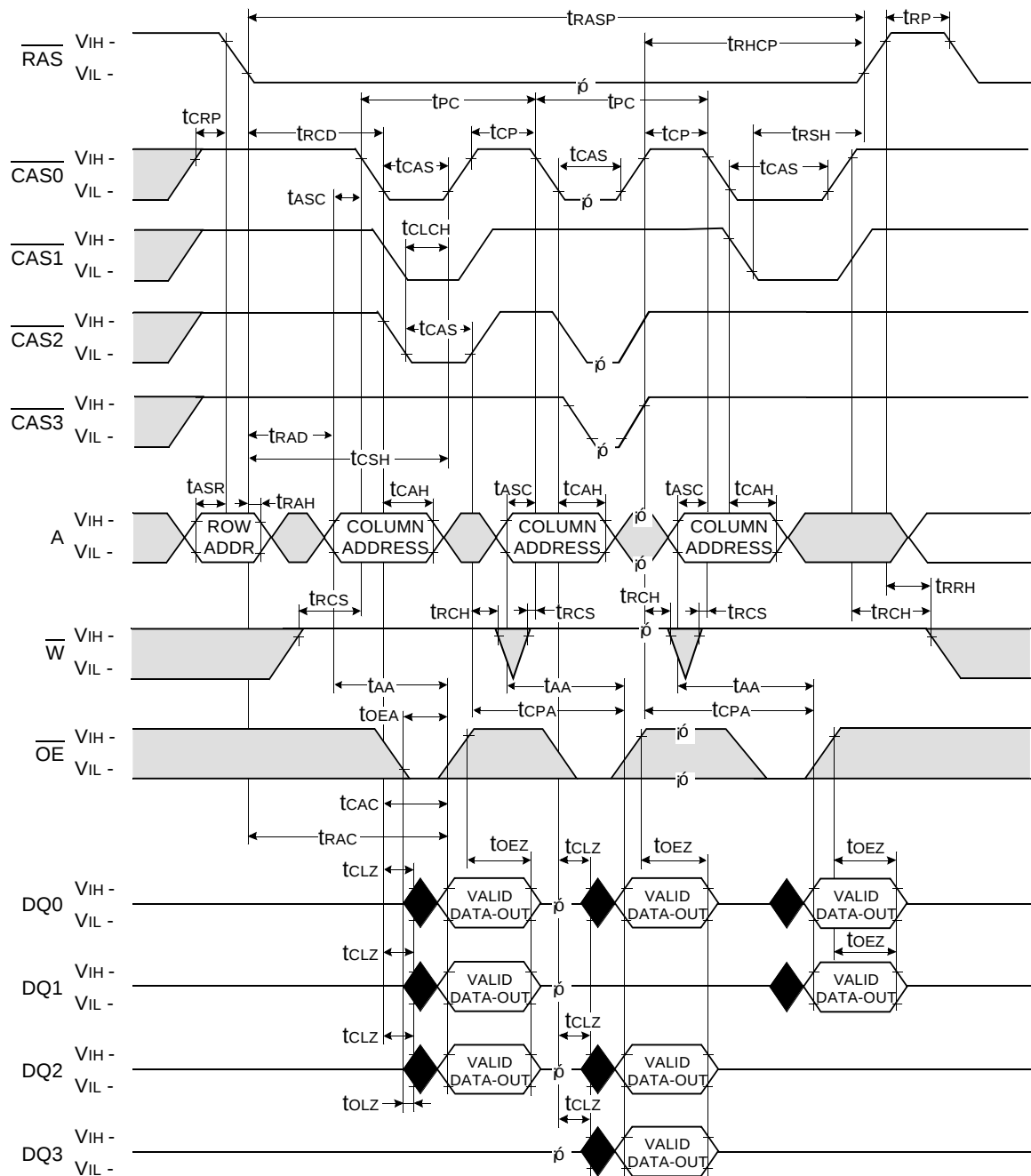
WRITE CYCLE ($\overline{\text{OE}}$ CONTROLLED WRITE)

READ - MODIFY - WRITE CYCLE

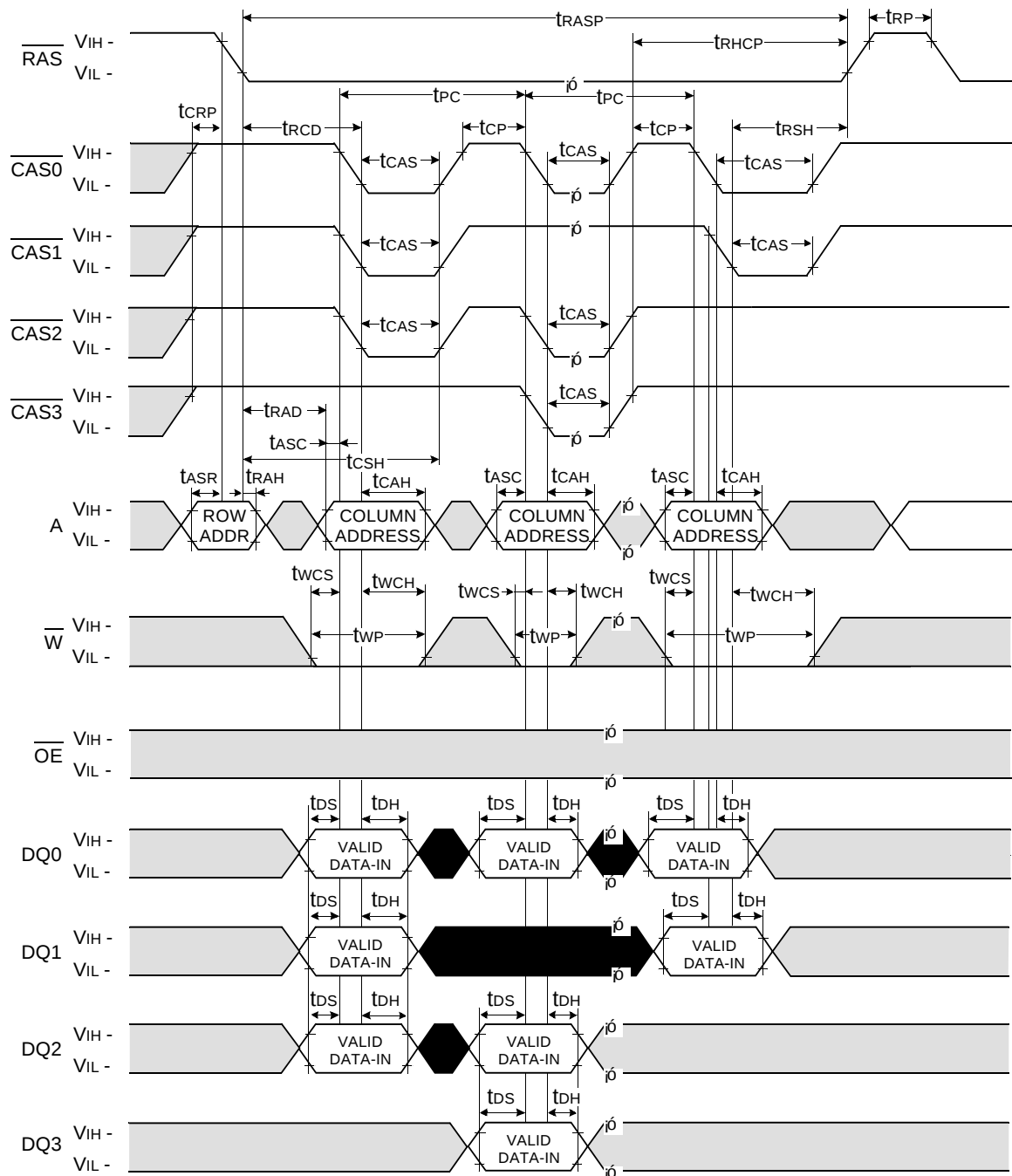


FAST PAGE READ CYCLE

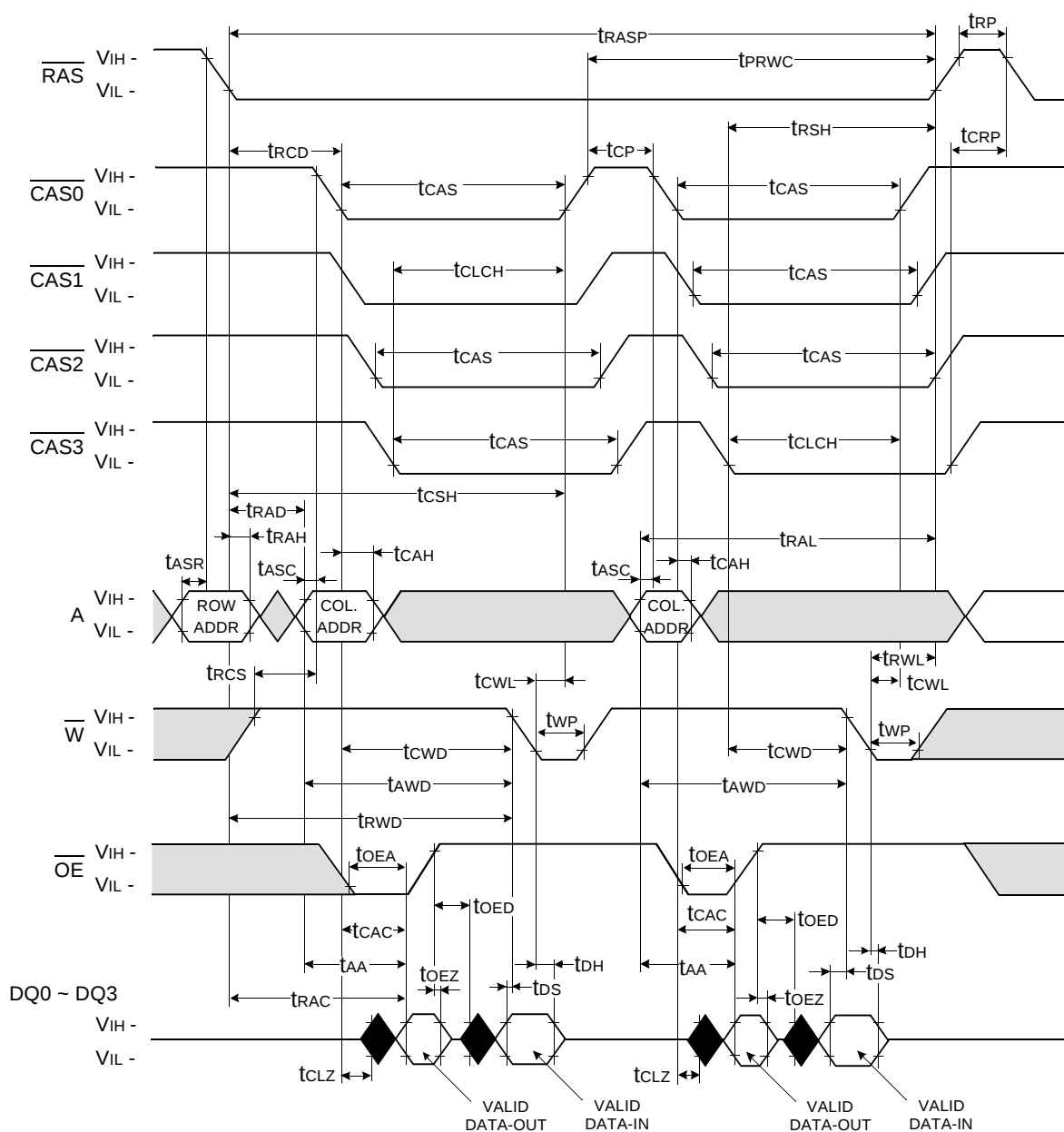
NOTE : DOUT = OPEN



FAST PAGE WRITE CYCLE (EARLY WRITE)



FAST PAGE READ - MODIFY - WRITE CYCLE



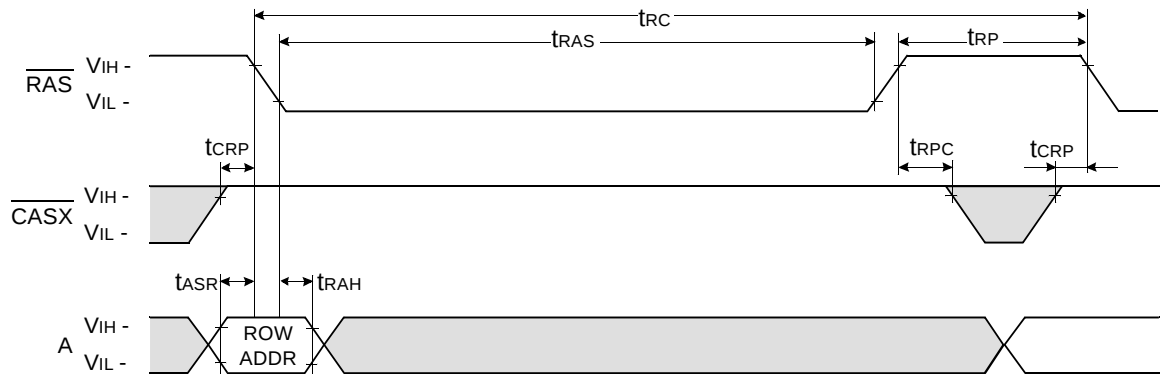
 Don't care

 Undefined

$\overline{\text{RAS}}$ - ONLY REFRESH CYCLE

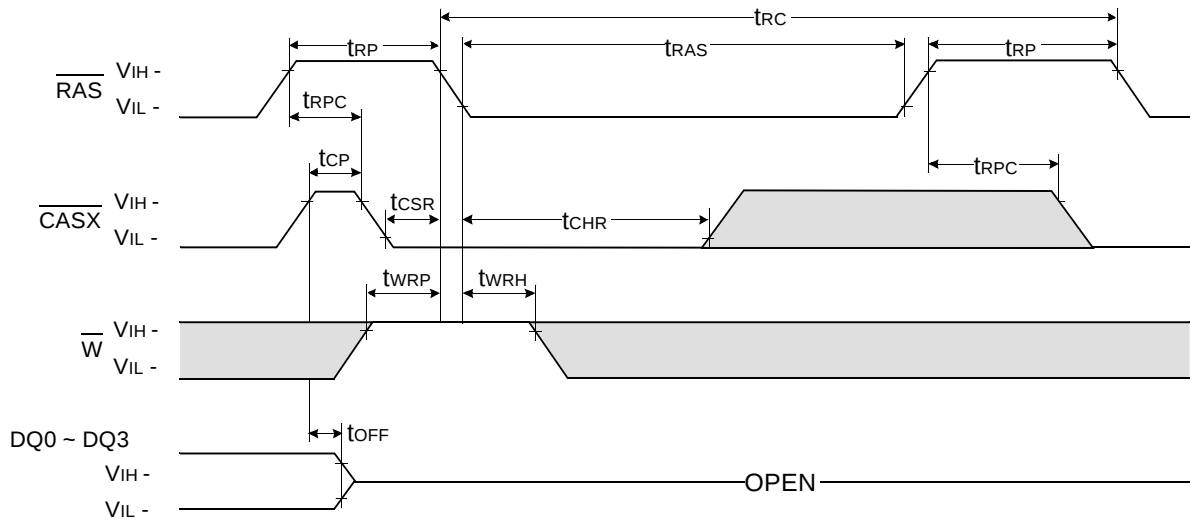
NOTE : $\overline{\text{W}}$, $\overline{\text{OE}}$, DIN = Don't care

DOUT = OPEN



$\overline{\text{CAS}}$ - BEFORE - $\overline{\text{RAS}}$ REFRESH CYCLE

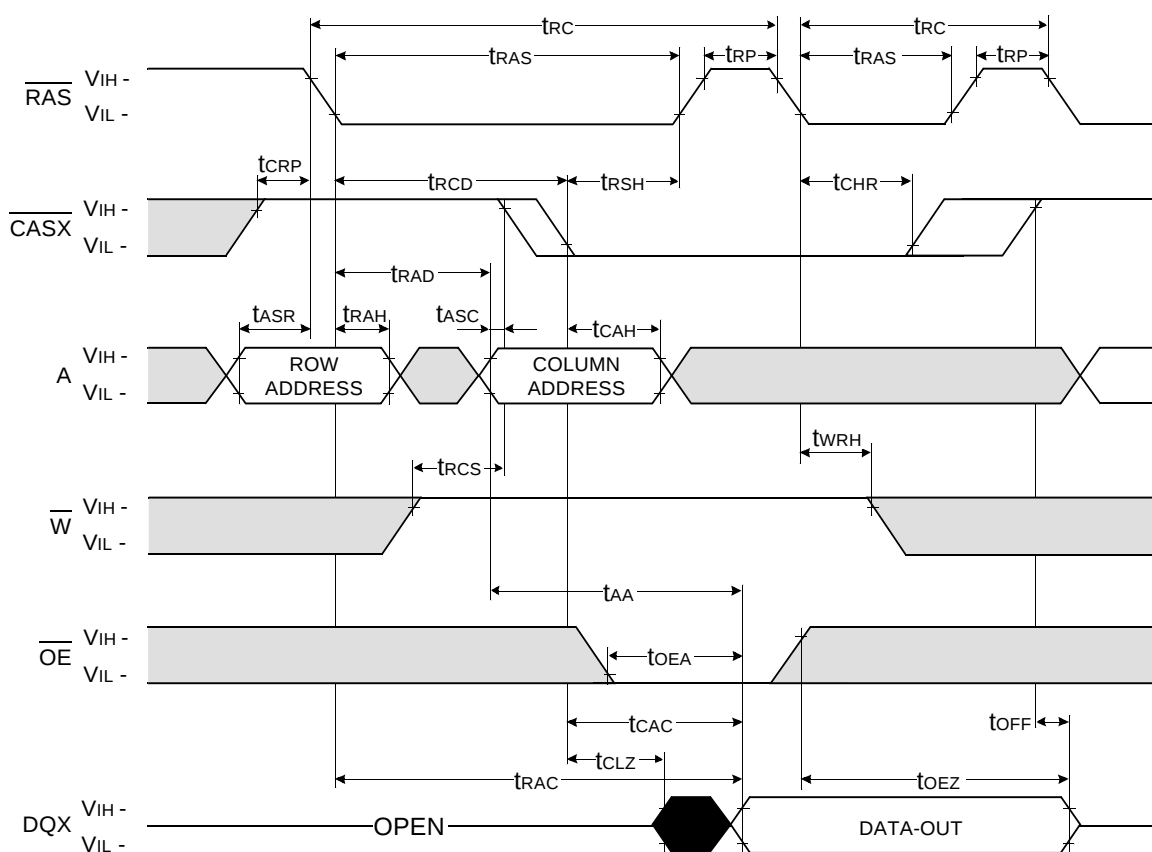
NOTE : $\overline{\text{OE}}$, A = Don't care



Don't care

Undefined

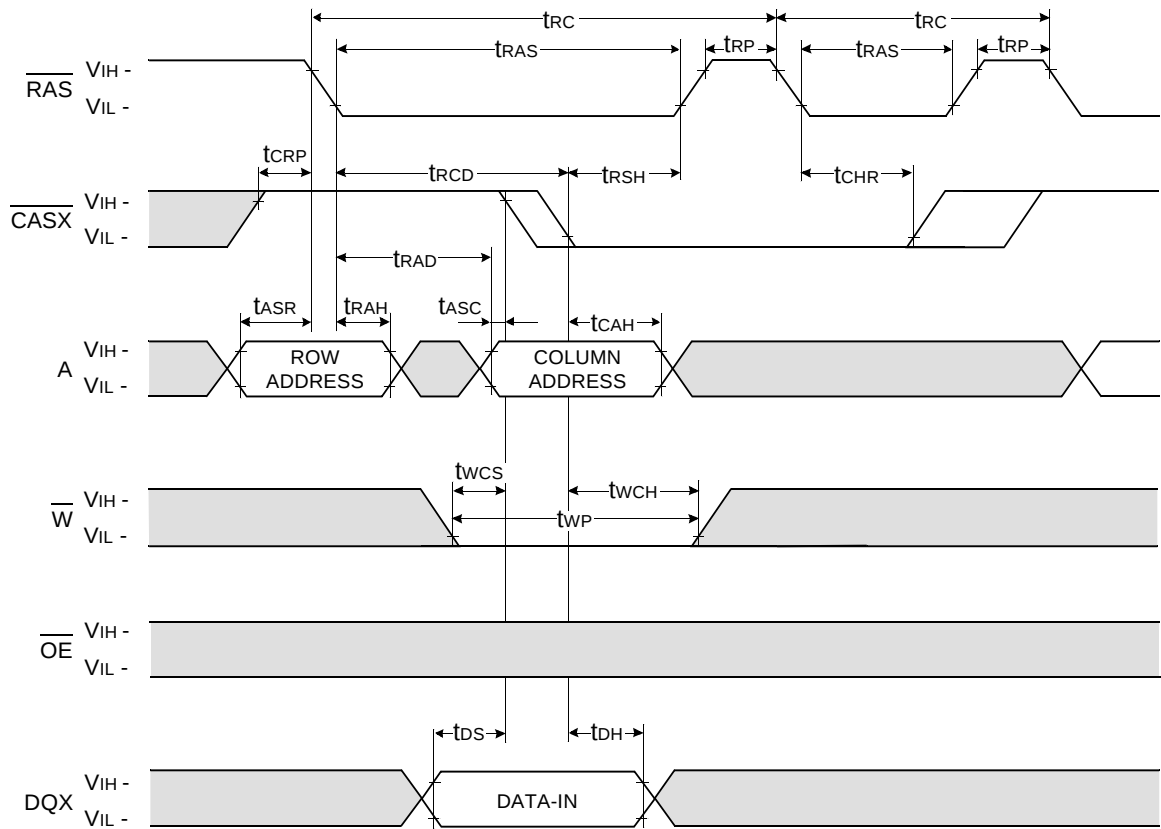
HIDDEN REFRESH CYCLE (READ)

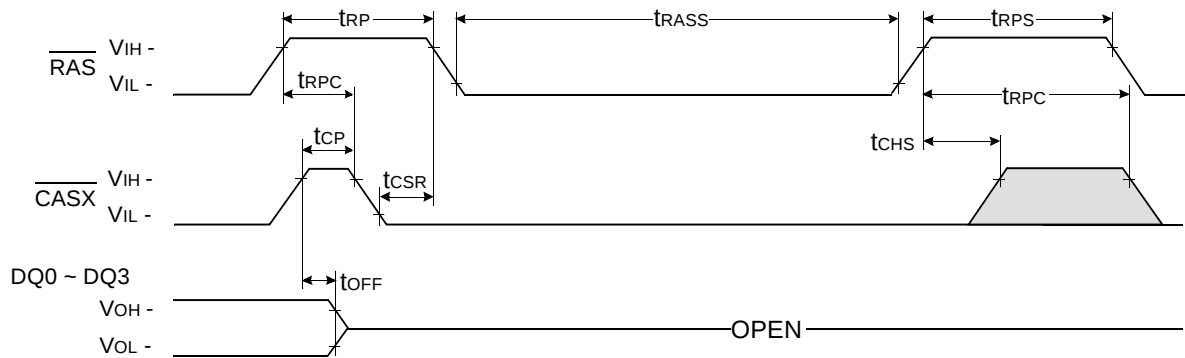
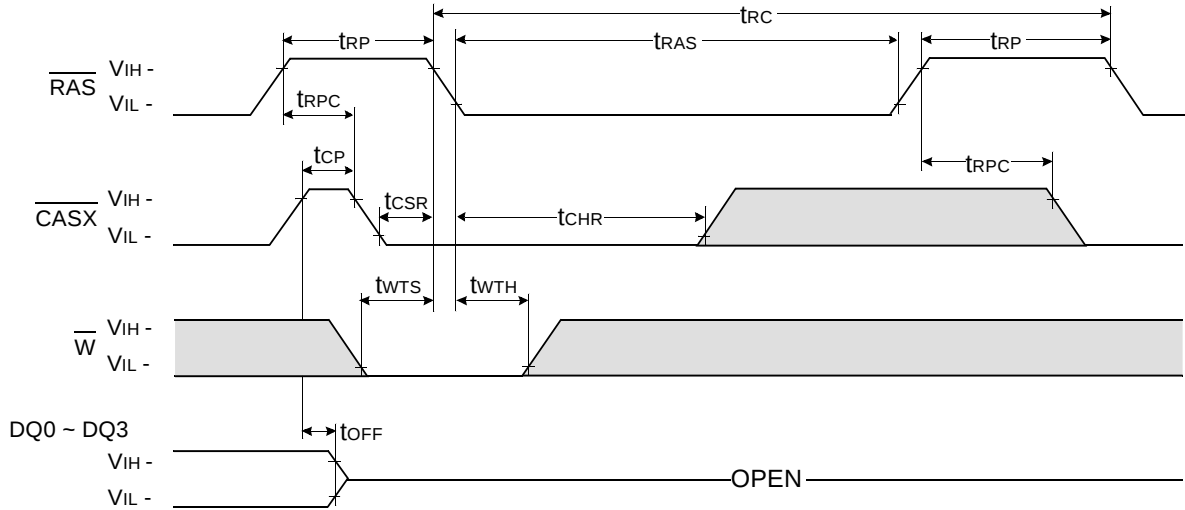


Don't care
Undefined

HIDDEN REFRESH CYCLE (WRITE)

NOTE : DOUT = OPEN



CAS - BEFORE - RAS SELF REFRESH CYCLENOTE : $\overline{\text{OE}}$, A = Don't care**TEST MODE IN CYCLE**NOTE : $\overline{\text{OE}}$, A = Don't care

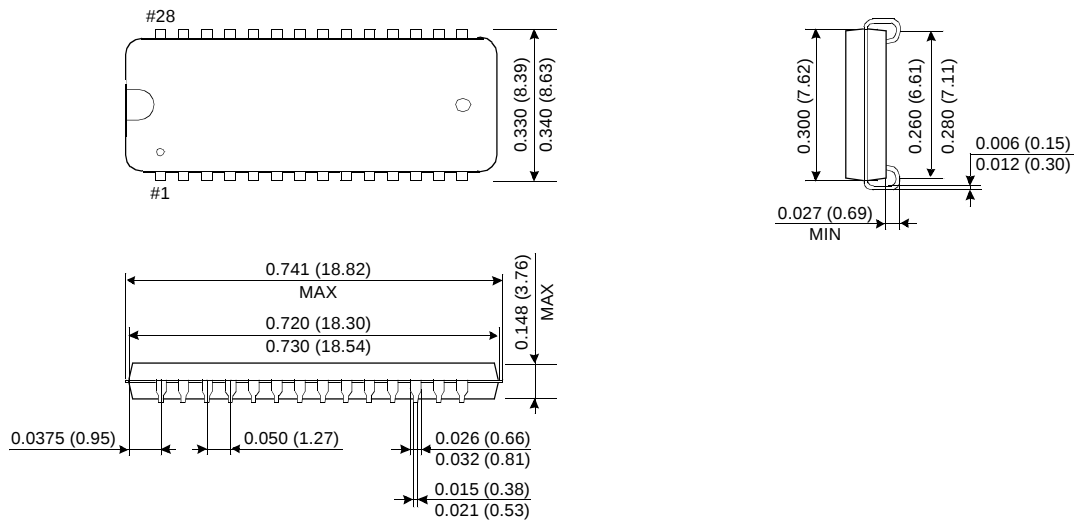
Don't care

Undefined

PACKAGE DIMENSION

28 SOJ 300mil

Units : Inches (millimeters)



28 TSOP(II) 300mil

Units : Inches (millimeters)

