512MB DDR SDRAM MODULE

(64Mx72(32Mx72*2 bank) based on 32Mx8 DDR SDRAM)

Unbuffered 184pin DIMM
72-bit ECC/Parity

Revision 0.0

Sep. 1999

Revision History

Revision 0 (Sep 1999)

1. First release for internal usage

KMM381L6423AT DDR SDRAM 184pin DIMM

64Mx72 DDR SDRAM 184pin DIMM based on 32Mx8

1. GENERAL DESCRIPTION

The Samsung KMM381L6423AT is 64M bit x 72 Double Data Rate SDRAM high density memory modules based on first gen. of 256Mb DDR SDRAM respectively. The Samsung KMM381L6423AT consists of eighteen CMOS 32M x 8 bit with 4banks Double Data Rate SDRAMs in 66pin TSOP-II(400mil) packages mounted on a 184pin glass-epoxy substrate. Four 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each DDR SDRAM. The KMM381L6423A-T is Dual In-line Memory Modules and intended for mounting into 184pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges of DQS. Range of operating frequencies, programmable latencies and burst lengths allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

2. FEATURE

- Performance range

Part No.	Max Freq.	Interface
KMM381L6423AT-G(F)Z	133MHz(7.5ns@CL=2)	SSTL_2
KMM381L6423AT-G(F)Y	133MHz(7.5ns@CL=2.5)	
KMM381L6423AT-G(F)0	100MHz(10ns@CL=2)	

- Power supply
  Vdd: 2.5V ± 0.2V
  Power: G - normal, F - Low power
- MRS cycle with address key programs
  CAS Latency (Access from column address):2,2.5
  Burst length ;2, 4, 8
  Data scramble ;Sequential & Interleave
- Serial presence detect with EEPROM
- PCB : **Height 1450 (mil)**, double sided component

3. PIN CONFIGURATIONS (Front side/back side)

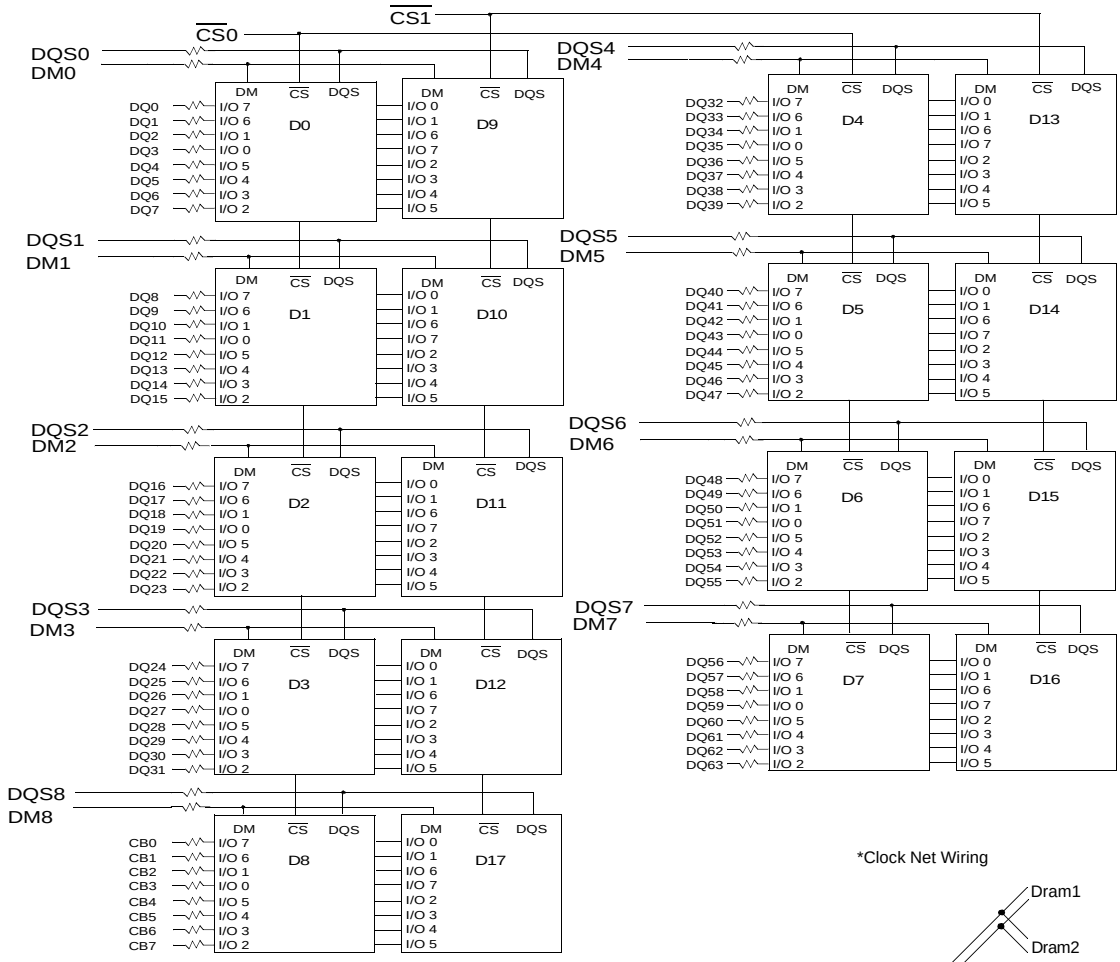
Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	VREF	32	A5	62	VDDQ	93	VSS	124	VSS	154	/RAS
2	DQ0	33	DQ24	63	/WE	94	DQ4	125	A6	155	DQ45
3	VSS	34	VSS	64	DQ41	95	DQ5	126	DQ28	156	VDDQ
4	DQ1	35	DQ25	65	/CAS	96	VDDQ	127	DQ29	157	/CS0
5	DQS0	36	DQS3	66	VSS	97	DM0	128	VDDQ	158	/CS1
6	DQ2	37	A4	67	DQS5	98	DQ6	129	DM3	159	DM5
7	VDD	38	VDD	68	DQ42	99	DQ7	130	A3	160	VSS
8	DQ3	39	DQ26	69	DQ43	100	VSS	131	DQ30	161	DQ46
9	NC	40	DQ27	70	VDD	101	NC	132	VSS	162	DQ47
10	NC	41	A2	71	NC	102	NC	133	DQ31	163	NC
11	VSS	42	VSS	72	DQ48	103	*A13	134	CB4	164	VDDQ
12	DQ8	43	A1	73	DQ49	104	VDDQ	135	CB5	165	DQ52
13	DQ9	44	CB0	74	VSS	105	DQ12	136	VDDQ	166	DQ53
14	DQS1	45	CB1	75	/CK2	106	DQ13	137	CK1	167	NC
15	VDDQ	46	VDD	76	CK2	107	DM1	138	/CK1	168	VDD
16	CK0	47	DQS8	77	VDDQ	108	VDD	139	VSS	169	DM6
17	/CK0	48	A0	78	DQS6	109	DQ14	140	DM8	170	DQ54
18	VSS	49	CB2	79	DQ50	110	DQ15	141	A10	171	DQ55
19	DQ10	50	VSS	80	DQ51	111	CKE1	142	CB6	172	VDDQ
20	DQ11	51	CB3	81	VSS	112	VDDQ	143	VDDQ	173	NC
21	CKE0	52	BA1	82	VDDID	113	*BA2	144	CB7	174	DQ60
22	VDDQ	KEY		83	DQ56	114	DQ20	KEY		175	DQ61
23	DQ16	53	DQ32	84	DQ57	115	A12	145	VSS	176	VSS
24	DQ17	54	VDDQ	85	VDD	116	VSS	146	DQ36	177	DM7
25	DQS2	55	DQ33	86	DQS7	117	DQ21	147	DQ37	178	DQ62
26	VSS	56	DQS4	87	DQ58	118	A11	148	VDD	179	DQ63
27	A9	57	DQ34	88	DQ59	119	DM2	149	DM4	180	VDDQ
28	DQ18	58	VSS	89	VSS	120	VDD	150	DQ38	181	SA0
29	A7	59	BA0	90	WP	121	DQ22	151	DQ39	182	SA1
30	VDDQ	60	DQ35	91	SDA	122	A8	152	VSS	183	SA2
31	DQ19	61	DQ40	92	SCL	123	DQ23	153	DQ44	184	V33

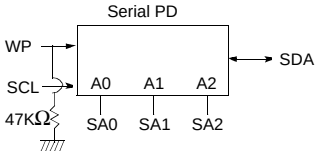
4. PIN DESCRIPTION

Pin Name	Function
A0 ~ A12	Address input (Multiplexed)
BA0 ~ BA1	Bank Select Address
DQ0 ~ DQ63	Data input/output
CB0 ~ CB7	Check bit(Data-in/data-out)
DQS0 ~ DQS8	Data Strobe input/output
CK0,$\overline{CK0}$ ~ CK2, $\overline{CK2}$	Clock input
CKE0,CKE1	Clock enable input
$\overline{CS0}$, $\overline{CS1}$	Chip select input
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
DM0 ~ DM8	Data - in mask
VDD	Power supply (2.5V)
VDDQ	Power Supply for DQs(2.5V)
VSS	Ground
VREF	Power supply for reference
V33	Serial EEPROM Power Supply (3.3V)
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
WP	Write protection
VDDID	VDD identification flag
DU	Don't use
NC	No connection

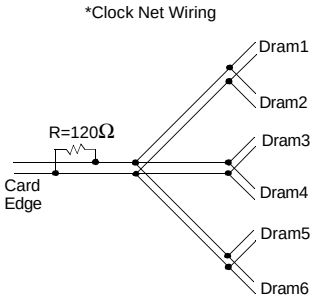
* These pins are not used in this module.

5. Functional Block Diagram

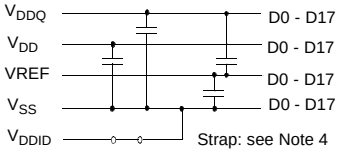




* Clock Wiring	
Clock Input	SDRAMs
CK0/CK0	6 SDRAMs
CK1/CK1	6 SDRAMs
CK2/CK2	6 SDRAMs



BA0 - BAn → BA0-BAn: SDRAMs D0 - D17
A0 - An → A0-An: SDRAMs D0 - D17



CKE1 → CKE: SDRAMs D9 - D17
RAS → RAS: SDRAMs D0 - D17
CAS → CAS: SDRAMs D0 - D17
CKE0 → CKE: SDRAMs D0 - D8
WE → WE: SDRAMs D0 - D17

Notes:
1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/DM/CKE/S relationships must be maintained as shown.
3. DQ, DQS, DM resistors: 22 Ohms.
4. VDDID strap connections
(for memory device VDD, VDDQ):
STRAP OUT (OPEN): VDD = VDDQ
STRAP IN (VSS): VDD ≠VDDQ.

6. ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-0.5 ~ 3.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}	-1.0 ~ 4.6	V
Voltage on V_{DDQ} supply relative to Vss	V_{DDQ}	-0.5 ~ 3.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	18	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

7. POWER & DC OPERATING CONDITIONS (SSTL_2 In/Out)

Recommended operating conditions(Voltage referenced to V_{SS}=0V, T_A=0 to 70°C)

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage(for device with a nominal V_{DD} of 2.5V)	V_{DD}	2.3	2.7	V	
I/O Supply voltage	V_{DDQ}	2.3	2.7	V	
I/O Reference voltage	V_{REF}	1.15	1.35	V	1
I/O Termination voltage(system)	V_{TT}	V_{REF}-0.04	V_{REF}+0.04	V	2
Input logic high voltage	V_{IH}(DC)	V_{REF}+0.18	V_{DDQ}+0.3	V	
Input logic low voltage	V_{IL}(DC)	-0.3	V_{REF}-0.18	V	
Input Voltage Level, CK and $\overline{CK}$ inputs	V_{IN}(DC)	-0.3	V_{DDQ}+0.3	V	
Input Differential Voltage, CK and $\overline{CK}$ inputs	V_{ID}(DC)	0.36	V_{DDQ}+0.6	V	
Input leakage current	I_I	-5	5	uA	3
Output leakage current	I_{OZ}	-5	5	uA	
Output High Current (V_{OUT} = 1.95V)	I_{OH}	-15.2		mA	
Output Low Current (V_{OUT} = 0.35V)	I_{OL}	15.2		mA	

Note :

1. Typically, the value of V_{REF} is expected to be about 0.5*V_{DDQ} of the transmitting device. V_{REF} is expected to track variation in V_{DDQ}.
2. Peak to peak AC noise on V_{REF} may not exceed 2% V_{REF}(DC).
3. V_{tt} of the transmitting device must track V_{REF} of the receiving device.

8. DC CHARACTERISTICS

Recommended operating conditions Unless Otherwise Noted, T_A=0 to 70°C)

Parameter	Symbol	Test Condition	$\overline{CAS}$ Latency	Version			Unit	Note
				-Z	-Y	-0		
Operating Current (One Bank Active)	I_{DD1}	Burst=2 tRC=tRC(min), CL=2.5 I_{OUT}=0mA, Active-Read-Precharge		T.B.D	T.B.D	T.B.D	mA	1
Precharge Power-down Standby Current	I_{DD2P}	CKE≤VIL(max), tCK=tCK(min), All banks idle		T.B.D			mA	
Precharge Standby Current in Non Power-down mode	I_{DD2N}	CKE≥VIH(min), $\overline{CS}$≥VIH(min), tCK=tCK(min)		T.B.D			mA	
Active Standby Current in Power-down mode	I_{DD3P}	All banks idle,CKE≤VIL(max),tCK=tCK(min)		T.B.D			mA	
Active Standby Current in Non Power-down mode	I_{DD3N}	One bank; Active-Precharge, tRC=tRAS(max), tCK=tCK(min)		T.B.D			mA	
Operating Current(Read)	I_{DD4R}	Burst=2, tCK=tCK(min), I_{OUT}=0mA	2.5	T.B.D	T.B.D	T.B.D	mA	1
			2	T.B.D	T.B.D	T.B.D		
Operating Current(Write)	I_{DD4W}	Burst=2, tCK=tCK(min)	2.5	T.B.D	T.B.D	T.B.D	mA	1
			2	T.B.D	T.B.D	T.B.D		
Auto Refresh Current	I_{DD5}	t_{RC}≥t_{RFC}(min)		T.B.D			mA	2
Self Refresh Current	I_{DD6}	CKE≤0.2V		T.B.D			mA	

Note : 1. Measured with outputs open.
2. Refresh period is 64ms

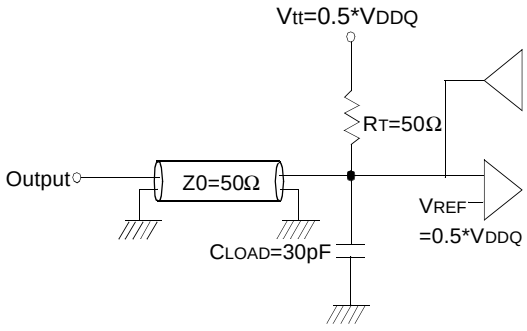
9. AC Operating Conditions

Parameter/Condition	Symbol	Min	Max	Unit	Note
Input High (Logic 1) Voltage, DQ, DQS and DM signals	VIH(AC)	VREF + 0.35		V	
Input Low (Logic 0) Voltage, DQ, DQS and DM signals.	VIL(AC)		VREF - 0.35	V	
Input Differential Voltage, CK and CK inputs	VID(AC)	0.7	VDDQ+0.6	V	1
Input Crossing Point Voltage, CK and CK inputs	VIX(AC)	0.5*VDDQ-0.2	0.5*VDDQ+0.2	V	2

Note 1. VID is the magnitude of the difference between the input level on CK and the input on $\overline{CK}$.
2. The value of V_{IX} is expected to equal 0.5*V_{DDQ} of the transmitting device and must track variations in the DC level of the same.

10. AC OPERATING TEST CONDITIONS (V_{DD}=3.3V, V_{DDQ}=2.5V, T_A= 0 to 70°C)

Parameter	Value	Unit	Note
Input reference voltage for Clock	0.5 * V_{DDQ}	V	
Input signal maximum peak swing	1.5	V	
Input signal minimum slew rate	1.0	V/ns	
Input Levels(V_{IH}/V_{IL})	V_{REF}+0.35/V_{REF}-0.35	V	
Input timing measurement reference level	V_{REF}	V	
Output timing measurement reference level	V_{tt}	V	
Output load condition	See Load Circuit		



(Fig. 1) Output Load Circuit (SSTL_2)

11. Input/Output CAPACITANCE (V_{DD}=3.3V, V_{DDQ}=2.5V, T_A= 25°C, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance(A_0 ~ A_{11}, BA_0 ~ BA_1,$\overline{RAS}$,$\overline{CAS}$, $\overline{WE}$)	C_{IN1}	-	98	pF
Input capacitance(CKE_0,CKE_1)	C_{IN2}	-	67	pF
Input capacitance($\overline{CS_0}$, $\overline{CS_1}$)	C_{IN3}	-	60	pF
Input capacitance(CLK_0, CLK_1, CLK_2)	C_{IN4}	-	38	pF
Input capacitance(DM_0~DM_8)	C_{IN5}	-	16	pF
Data & DQS input/output capacitance(DQ_0~DQ_{63})	C_{OUT1}	-	16	pF
Data input/output capacitance(CB_0~CB_7)	C_{OUT2}	-	16	pF

12. AC CHARACTERISTICS. (These AC charicteristics were tested on the Component)

Parameter		Symbol	- Z(PC266@CL=2)		- Y(PC266@CL=2.5)		- 0(PC200@CL=2)		Unit	Note
			Min	Max	Min	Max	Min	Max		
Row cycle time		tRC	65		65		70		ns	
Refresh row cycle time		tRFC	75		75		80		ns	
Row active time		tRAS	45	12K	48	12K	48	12K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD	20		20		20		ns	
Row precharge time		tRP	20		20		20		ns	
Row active to Row active delay		tRRD	15		15		15		ns	
Write recovery time		tWR	2		2		2		tCK	
Last data in to Read command		tCDLR	1		1		1		tCK	
Last data in to Write command		tCDLW	0		0		0		tCK	
Col. address to Col. address delay		tCCD	1		1		1		tCK	
Clock cycle time	CL=2.0	tCK	7.5	15	10	15	10	15	ns	
	CL=2.5		7	15	7.5	15	8	15	ns	
Clock high level width		tCH	0.45	0.55	0.45	0.55	0.45	0.55	tCK	
Clock low level width		tCL	0.45	0.55	0.45	0.55	0.45	0.55	tCK	
DQS-out access time from CK/$\overline{CK}$		tDQSCK	-0.75	+0.75	-0.75	+0.75	-0.8	+0.8	ns	
Output data access time from CK/$\overline{CK}$		tAC	-0.75	+0.75	-0.75	+0.75	-0.8	+0.8	ns	
Data strobe edge to ouput data edge		tDQSQ	-0.5	+0.5	-0.5	+0.5	-0.6	+0.6	ns	
Read Preamble		tRPRE	0.9	1.1	0.9	1.1	0.9	1.1	tCK	
Read Postamble		tRPST	0.4	0.6	0.4	0.6	0.4	0.6	tCK	
Data out high impedence time from CK/$\overline{CK}$		tHZQ	-0.75	+0.75	-0.75	+0.75	-0.8	+0.8	ns	2
CK to valid DQS-in		tDQSS	0.75	1.25	0.75	1.25	0.75	1.25	tCK	
DQS-in setup time		tWPRES	0		0		0		ns	3
DQS-in hold time		tWPREH	0.25		0.25		0.25		tCK	
DQS-in high level width		tDQSH	0.4	0.6	0.4	0.6	0.4	0.6	tCK	
DQS-in low level width		tDQSL	0.4	0.6	0.4	0.6	0.4	0.6	tCK	
DQS-in cycle time		tDSC	0.9	1.1	0.9	1.1	0.9	1.1	tCK	
Address and Control Input setup time		tIS	1.1		1.1		1.2		ns	
Address and Control Input hold time		tIH	1.1		1.1		1.2		ns	
Mode register set cycle time		tMRD	15		15		16		ns	
DQ & DM setup time to DQS		tDS	0.5		0.5		0.6		ns	
DQ & DM hold time to DQS		tDH	0.5		0.5		0.6		ns	
DQ & DM input pulse width		tDIPW	1.75		1.75		2		ns	
Power down exit time		tPDEX	10		10		10		ns	
Exit self refresh to write command		tXSW	95				116		ns	

Parameter		Symbol	PC266A		PC266B		PC200		Unit	Note
			Min	Max	Min	Max	Min	Max		
Exit self refresh to bank active command		tXSA	75		75		80		ns	
Exit self refresh to read command		tXSR	200		200		200		Cycle	
Refresh interval time	256Mb	tREF	7.8		7.8		7.8		us	1
Output DQS valid window		tDV	0.35		0.35		0.35		tCK	
DQS write postamble time		tWPST	0.25		0.25		0.25		tCK	4
Auto precharge write recovery + Precharge time		tDAL	35		35		35		ns	

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1. Maximum burst refresh of 8
2. tHZQ transitions occurs in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level, but specify when the device output is no longer driving.
3. The specific requirement is that DQS be valid(High or Low) on or before this CK edge. The case shown(DQS going from High_Z to logic Low) applies when no writes were previously in progress on the bus. If a previous write was in progress, DQS could be High at this time, depending on tDQSS.
4. The maximum limit for this parameter is not a device limit. The device will operate with a great value for this parameter, but system performance (bus turnaround) will degrade accordingly.

13. SIMPLIFIED TRUTH TABLE

COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DM	$BA_{0,1}$	A_{10}/AP	A_{11},A_{12} A_9 ~ A_0	Note
Register	Extended MRS		H	X	L	L	L	L	X	OP CODE			1, 2
Register	Mode Register Set		H	X	L	L	L	L	X	OP CODE			1, 2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank Active & Row Addr.			H	X	L	L	H	H	X	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address (A_0~A_7)	4
	Auto Precharge Enable										H		4
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address (A_0~A_7)	4
	Auto Precharge Enable										H		4, 6
Burst Stop			H	X	L	H	H	L	X	X			7
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	All Banks									X	H		5
Active Power Down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DM			H	X					V	X			8
No Operation Command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

Note : 1. OP Code : Operand Code. A_0 ~ A_{12} & BA_0 ~ BA_1 : Program keys. (@EMRS/MRS)

2.EMRS/ MRS can be issued only at all banks precharge state.
A new command can be issued 2 clock cycles after EMRS or MRS.

3. Auto refresh functions are same as the CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.

4. BA_0 ~ BA_1 : Bank select addresses.
If both BA_0 and BA_1 are "Low" at read, write, row active and precharge, bank A is selected.
If both BA_0 is "High" and BA_1 is "Low" at read, write, row active and precharge, bank B is selected.
If both BA_0 is "Low" and BA_1 is "High" at read, write, row active and precharge, bank C is selected.
If both BA_0 and BA_1 are "High" at read, write, row active and precharge, bank D is selected.

5. If A_{10}/AP is "High" at row precharge, BA_0 and BA_1 are ignored and all banks are selected.

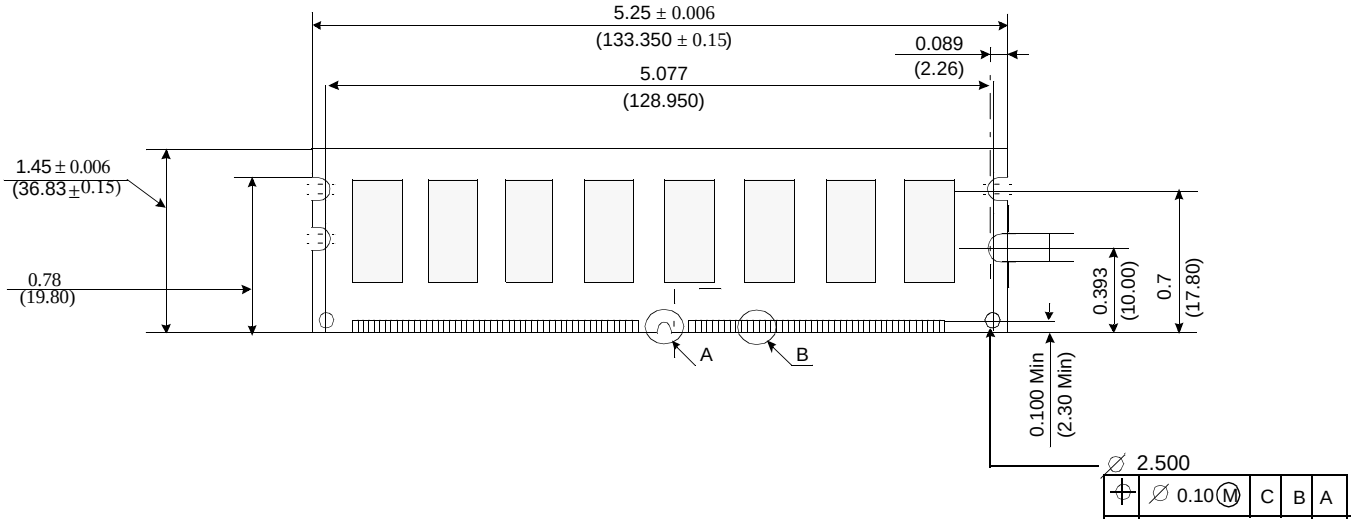
6. During burst write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at t_{RP} after the end of burst.

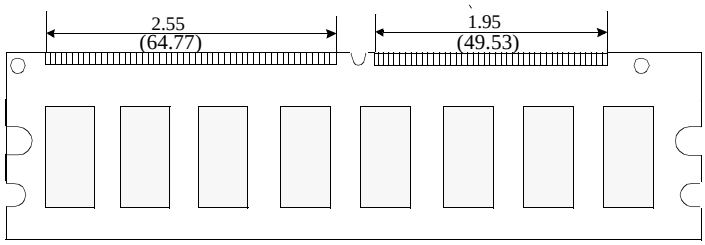
7. Burst stop command is valid at every burst length.

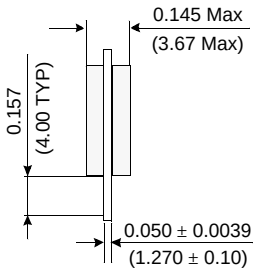
8. DM sampled at the rising and falling edges of the DQS and Data-in are masked at the both edges (Write DM latency is 0).

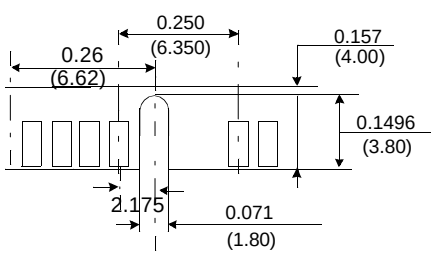
14. PACKAGE DIMENSIONS

Units : Inches (Millimeters)

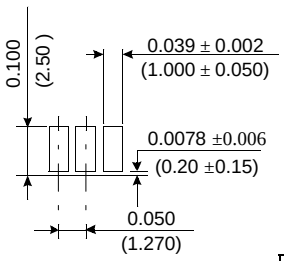




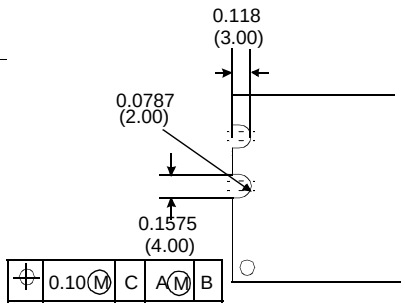




Detail A



Detail B



Tolerances : ± 0.005(.13) unless otherwise specified.
The used device is 32Mx8 SDRAM, TSOP.
SDRAM Part NO : KM48L32331AT