KMM379S823CT, Burst Mode

8Mx72 SDRAM DIMM with PLL & Register based on 8Mx8, 4Banks, 4K Ref. 3.3V Synch. DRAMs

GENERAL DESCRIPTION

The Samsung KMM379S823CT is a 8M bit x 72 Synchronous Dynamic RAM high density memory module. The Samsung KMM379S823CT consists of nine CMOS 8M x 8 bit Synchronous DRAMs in TSOP-II 400mil packages, one 20 bits Drive ICs for input control signal and one PLL in 52-pin TQFP package mounted on a 200-pin glass-epoxy substrate. Two 0.1uF decopling capacitors are mounted on the printed circuit board for each SDRAM. The KMM379S823CT is a Dual In-line Memory Module and is intended for mounting into 200-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
KMM379S823CT-GL	100MHz (10ns @ CL=3)

- Burst Mode Operation
- Auto & Self Refresh Capability (4096 cycles / 64ms)
- LVTTL compatible inputs and outputs
- Single **3.3V±0.3V** power supply
- MRS cycle with address key programs
  Latency (Access from column address)
  Burst Length (1, 2, 4, 8 & Full page)
  Data Scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- PCB : **Height(1,500mil max)**, double sided component

PIN CONFIGURATIONS (Front Side / Back Side)

Pin	Front	Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back	Pin	Back
1	V_{DD}	26	$V_{DD(Q)}$	51	$\overline{V_{SS}}$	76	DQ16	101	*VTT	126	DQ53	151	CLK0	176	$V_{DD(Q)}$
2	*VTT	27	DQ51	52	RAS	77	V_{SS}	102	*VTT	127	DQ52	152	$\overline{V_{DD}}$	177	*CLK2
3	*VTT	28	DQ50	53	V_{SS}	78	*VRef	103	V_{SS}	128	$V_{DD(Q)}$	153	$\overline{CS1}$	178	V_{SS}
4	*IN	29	V_{SS}	54	*A14	79	*VTT	104	*REGE	129	DQ47	154	$\overline{CS0}$	179	V_{SS}
5	*OUT	30	DQ49	55	A13	80	$V_{DD(Q)}$	105	NC	130	DQ46	155	V_{SS}	180	*DQMB1
6	ID1	31	DQ48	56	V_{DD}	81	DQ15	106	NC	131	V_{SS}	156	BA1(A12)	181	*DQMB2
7	ID2	32	$V_{DD(Q)}$	57	A0	82	DQ14	107	ID3	132	DQ45	157	A10(AP)	182	V_{DDQ}
8	V_{SS}	33	DQ43	58	A1	83	V_{SS}	108	DQ71	133	DQ44	158	V_{DD}	183	DQ11
9	DQ67	34	DQ42	59	V_{SS}	84	DQ13	109	DQ70	134	$V_{DD(Q)}$	159	A2	184	DQ10
10	DQ66	35	V_{SS}	60	DQ35	85	DQ12	110	V_{SS}	135	DQ39	160	A3	185	V_{SS}
11	$V_{DD(Q)}$	36	DQ41	61	DQ34	86	$V_{DD(Q)}$	111	DQ69	136	DQ38	161	V_{SS}	186	DQ9
12	DQ65	37	DQ40	62	$V_{DD(Q)}$	87	DQ7	112	DQ68	137	V_{SS}	162	DQ31	187	DQ8
13	DQ64	38	$V_{DD(Q)}$	63	DQ33	88	DQ6	113	$V_{DD(Q)}$	138	DQ37	163	DQ30	188	V_{DDQ}
14	V_{SS}	39	A4	64	DQ32	89	V_{SS}	114	*CLK3	139	DQ36	164	$V_{DD(Q)}$	189	DQ3
15	DQ63	40	A5	65	V_{SS}	90	DQ5	115	V_{SS}	140	V_{DD}	165	DQ29	190	DQ2
16	DQ62	41	V_{SS}	66	DQ27	91	DQ4	116	*VRef	141	A6	166	DQ28	191	V_{SS}
17	*VTT	42	A8	67	DQ26	92	$\overline{V_{DDQ()}}$	117	DQ59	142	A7	167	V_{SS}	192	DQ1
18	DQ61	43	A9	68	$V_{DD(Q)}$	93	*PDE	118	DQ58	143	V_{SS}	168	DQ23	193	DQ0
19	DQ60	44	V_{DD}	69	DQ25	94	PD1	119	V_{SS}	144	BA0(A11)	169	DQ22	194	PD5
20	$V_{DD(Q)}$	45	CKE1	70	DQ24	95	PD2	120	DQ57	145	*A15	170	$V_{DD(Q)}$	195	PD6
21	*DQMB7	46	CKE0	71	V_{SS}	96	PD3	121	DQ56	146	V_{DD}	171	DQ21	196	PD7
22	*DQMB6	47	$\overline{V_{SS}}$	72	DQ19	97	PD4	122	$V_{DD(Q)}$	147	$\overline{DQM}$	172	DQ20	197	PD8
23	V_{SS}	48	CAS	73	DQ18	98	*VTT	123	DQ55	148	WE	173	V_{SS}	198	V_{DD}
24	*DQMB5	49	*VTT	74	$V_{DD(Q)}$	99	*VTT	124	DQ54	149	V_{SS}	174	*DQMB3	199	*VTT
25	*DQMB4	50	V_{DD}	75	DQ17	100	V_{SS}	125	V_{SS}	150	*CLK1	175	*DQMB2	200	*VTT

Note :1. "*" ; These pins are tied together
2. In LVTTL interface, V_{DDQ}=V_{DD} and VSSQ=VSS

PIN NAMES

Pin Name	Function	
A0 ~ A11	Address Input (multiplexed)	Row & column address are multiplexed on the same pins. Row address:RA0~RA11, Column address:CA0~CA8
BA0, BA1	Select Bank	Select bank to be activated during row address latch time and select bank for read/wirte during column address latch time.
DQ0 ~ DQ71	Data Input / Output	Data inputs/outputs are multiplexed on the same pins.
CLK1 ~ CLK3	Clock Input	Clock Input
CKE	Clock Enable Input	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disables input buffers for power down standby.
$\overline{CS}$0	Chip Select Input	Disables or enables device operation by masking or enabling all
$\overline{RAS}$	Row Address Storbe	Latches row address on the positive edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	Colume Address Strobe	Latches column address on the positive edge of the CLK with $\overline{RAS}$ low. Enables column access.
$\overline{WE}$	Write Enable	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$,$\overline{WE}$ active.
DQM	Data Mask	Makes data output Hi-Z, tSHZ after the clock and masks the output. Blocks data intput when DQM
$\overline{PDE}$	Presence Detect Buffer Enable	Presence Detect Buffer Enable
PD1 ~ PD8	Buffered Logical Presence Detect Output	Buffered Logical Presence Detect Output
ID1 ~ ID3	ID Output	ID Output
*IN, *OUT	Unbuffered Physical Detect Input/Output	Unbuffered Physical Detect Input/Output
V_{DD}	Power Supply	Power Supply
$V_{DD(Q)}$	Power Supply for data Input/Output	Power Supply for data Input/Output
V_{Ref}	Power Supply for Reference	
V_{TT}	Termination Power Supply	Power Supply
V_{SS}	Ground	
NC	No Connection	

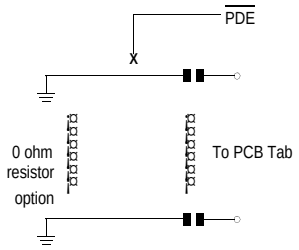
* These pins are tied together

PD & ID Table

Pin	10ns
PD1	1
PD2	1
PD3	0
PD4	1
PD5	1
PD6	0
PD7	1
PD8	1

ID3	Power	KMM379S823CT
1	Low-Power (Battery):Self Ref. with Low Power	X
0		O
ID2	**Precharge**	
1	Early RAS	X
0	No Early RAS	O
ID1	**Command Interval (tCCD)**	
1	1 Clock	O
0	2 Clock	X

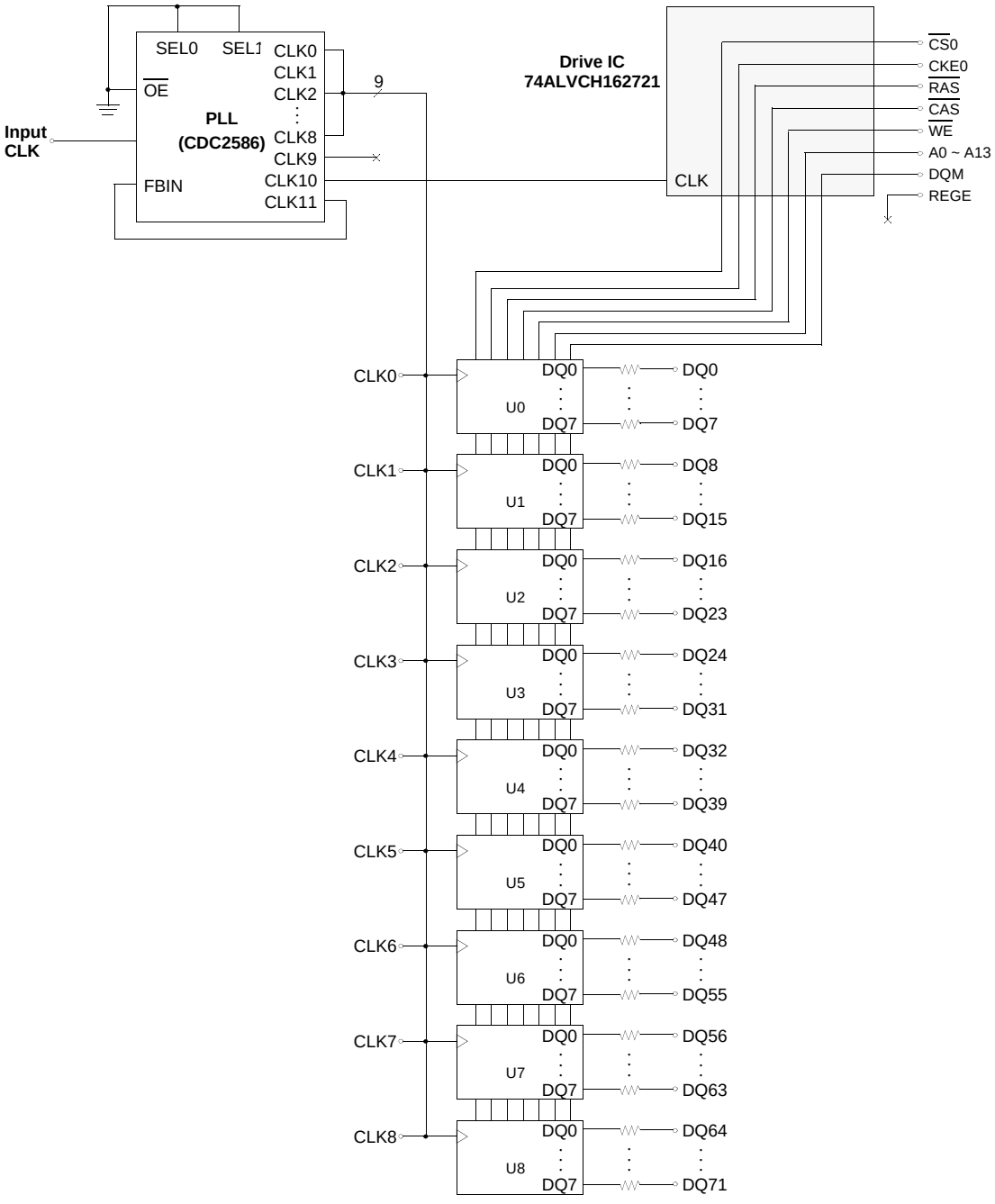
$\overline{PDE}$ & PD pin Scheme



Note : 1. Presence detect pins PD0 ~ PD7 are buffered and enabled by $\overline{PDE}$.

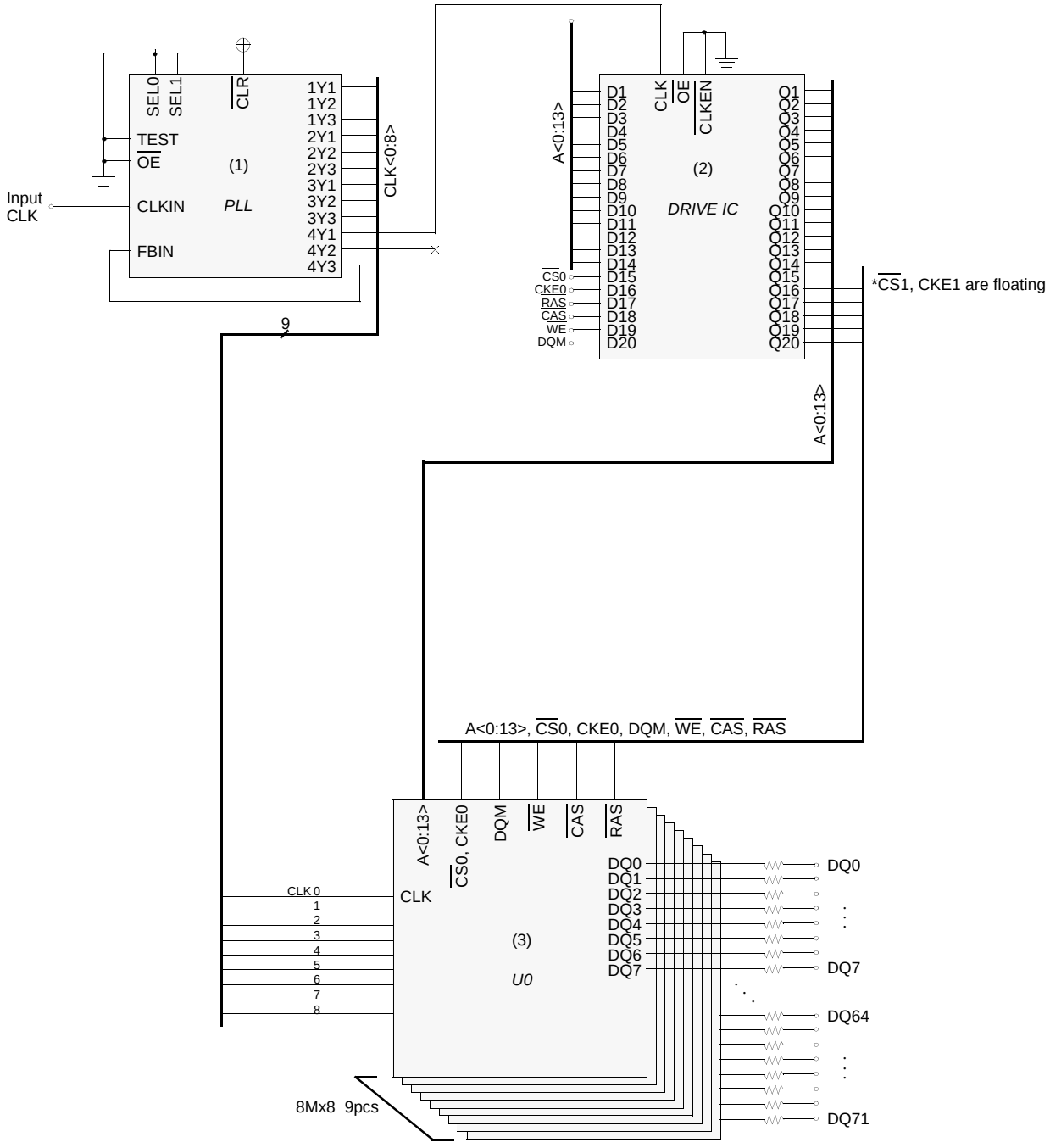
2. For the ID0 ... ID2 pins, a "0" is a strap to Vss, and a "1" is NC (No Connection).

FUNCTIONAL BLOCK DIAGRAM

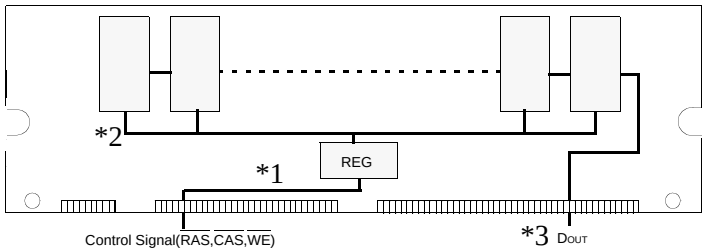


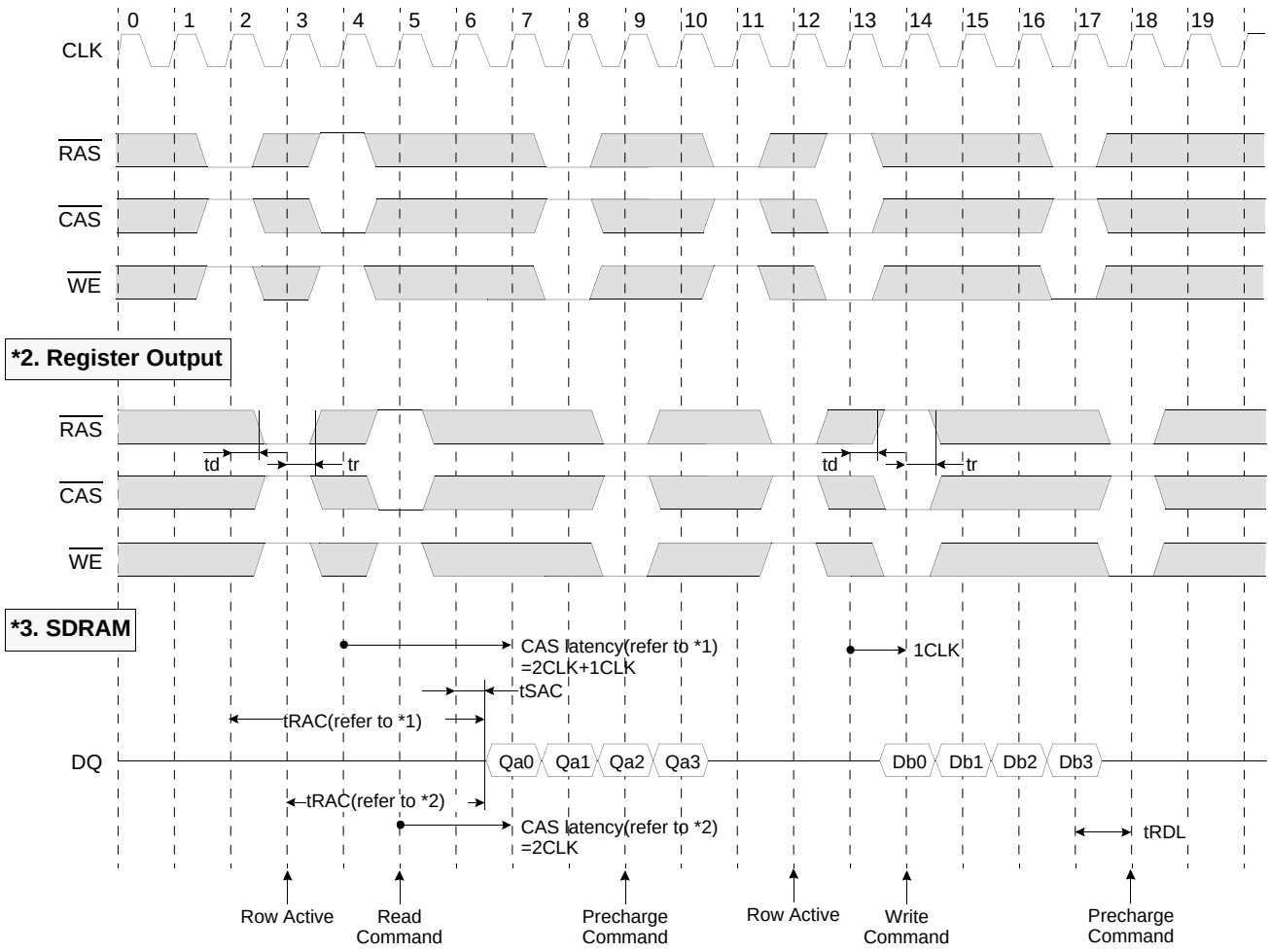
Note : 1. A 10 ohm +/-20% register shall be wired in series with DQ ... DQ71 near PCB tab edge connector.
2. All clock line outputs from the PLL CLOCK BUFFER should be equal length.

Standard Timing Diagram with PLL & Register



STANDARD TIMING DIAGRAM WITH PLL & REGISTER (CL=2, BL=4)





td, tr = Delay of register (74ALVC162835)

Notes : 1. In case of module timing, command cycles delayed 1CLK with respect to external input timing at the address and input signal because of the buffering in register (74ALVC162835). Therefore, Input/Output signals of read/write function should be issued 1CLK earlier as compared to Unbuffered DIMMs.

2. DIN is to be issued 1clock after write command in external timing because DIN is issued directly to module.

: Don't care

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	9	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high votlage	V_{IH}	2.0	3.0	V_{DD} +0.3	V	1
Input low voltage	V_{IL}	-0.3	0	0.8	V	2
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	**I_{IL}**	**-1**	-	**1**	**uA**	3
Output leakage current	I_{OL}	-1.5	-	1.5	uA	4

Note :
1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
   Input leakage currents include HI-Z output leakage for all bi-directional buffers with Tri-State outputs.
4. Dout is disabled, 0V ≤ V_{OUT} ≤ V_{DDQ}.

CAPACITANCE (T_A = 25°C, f = 1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A_0 ~ A_{13})	C_{IN1}	-	18	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, CKE0)	C_{IN2}	-	18	pF
Input capacitance (CLK0)	C_{IN3}	-	18	pF
Input capacitance ($\overline{CS0}$)	C_{IN4}	-	19	pF
Input capacitance (DQM)	C_{IN5}	-	20	pF
Data input/output capacitance (DQ_0 ~ DQ_{71})	C_{OUT}	-	20	pF

DC CHARACTERISTICS

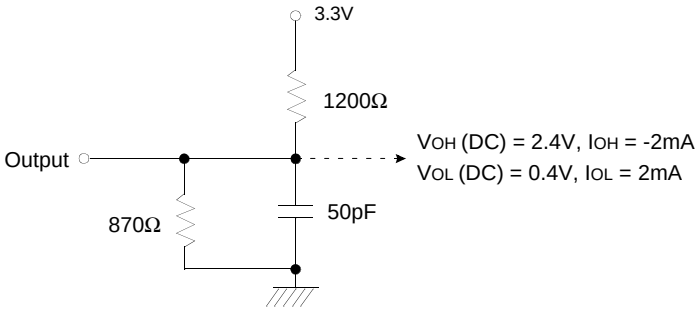
(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

Parameter	Symbol	Test Condition	CAS Latency	Version -L	Unit	Note
Operating Current (One Bank Active)	I_{CC1}	Burst Length =1 $t_{RC} \geq t_{RC}$(min) I_{OL} = 0 mA		630	mA	1
Precharge Standby Current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC} = 15ns		9	mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		9		
Precharge Standby Current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 15ns Input signals are changed one time during 30ns		108	mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		54		
Active Standby Current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CC} = 15ns		18	mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		18		
Active Standby Current in non power-down mode	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 15ns Input signals are changed one time during 30ns		180	mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		90		
Operating Current (Burst Mode)	I_{CC4}	I_{OL} = 0 mA Page Burst t_{CCD} = 2CLKs	3	675	mA	1
			2	630		
Refresh Current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		1,025	mA	2
Self Refresh Current	I_{CC6}	CKE ≤ 0.2V		9	mA	3

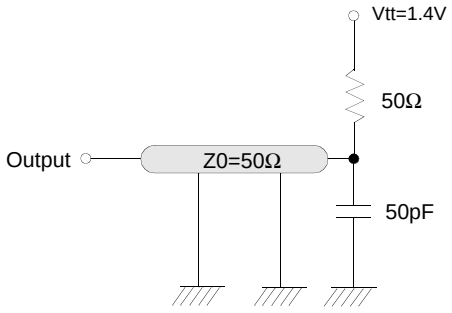
Note : 1. Measured with outputs open.
2. Refresh period is 64ms.
3. Measured with 1 PLL & 1 Drive IC.

AC OPERATING TEST CONDITIONS (V_{DD} = 3.45V±0.15V, T_A = 0 to 70°C)

Parameter	Value	Unit
Input levels (Vih/Vil)	2.4 / 0.4	V
Input timing measurement reference level	1.4	V
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC Output Load Circuit



(Fig. 2) AC Output Load Circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version	Unit	Note
			-L		
Row active to row active delay		$t_{RRD(min)}$	20	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		$t_{RCD(min)}$	20	ns	1
Row precharge time		$t_{RP(min)}$	20	ns	1
Row active time		$t_{RAS(min)}$	50	ns	1
		$t_{RAS(max)}$	100	us	
Row cycle time		$t_{RC(min)}$	70	ns	1
Last data in to row precharge		$t_{RDL(min)}$	10	ns	2
Last data in to new col. address delay		$t_{CDL(min)}$	1	CLK	2
Last data in to burst stop		$t_{BDL(min)}$	1	CLK	2
Col. address to col. address delay		$t_{CCD(min)}$	1	CLK	3
Number of valid output data	CAS latency=3		2	ea	4
	CAS latency=2		1		

Note : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time, and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Parameter		Symbol	- L		Unit	Note
			Min	Max		
CLK cycle time	CAS latency=3	tCC	10	1000	ns	1
	CAS latency=2		12			
CLK to valid output delay	CAS latency=3	tSAC		6	ns	1, 2
	CAS latency=2			7		
Output data hold time	CAS latency=3	tOH	3		ns	2
	CAS latency=2		3			
CLK high pulse width		tCH	3		ns	3
CLK low pulse width		tCL	3		ns	3
Data input setup time		tDSU	2		ns	3
Data input hold time		tDSH	1		ns	3
CLK to output in Low-Z		tSLZ	1		ns	
CLK to output in Hi-Z	CAS latency=3	tSHZ		6	ns	
	CAS latency=2			7		

*All AC parameters are measured from half to half.

Note : 1. Parameters depend on programmed CAS latency.
2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
3. Assumed input rise and fall time (tr & tf)=1ns.
If tr & tf is longer than 1ns, transient time compensation should be considered,
i.e., [(tr + tf)/2-1]ns should be added to the parameter.

FREQUENCY vs. AC PARAMETER RELATIONSHIP TABLE

KMM379S823CT - GL

(Unit : number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		70ns	50ns	20ns	20ns	20ns	10ns	10ns	10ns
100MHz (10.0ns)	3	7	5	2	2	2	1	1	1
83MHz (12.0ns)	2	6	5	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	5	4	2	2	2	1	1	1
60MHz (16.7ns)	2	5	3	2	2	2	1	1	1

SIMPLIFIED TRUTH TABLE

COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	$BA_{0,1}$	A_{10}/AP	A_{11}, A_9 ~ A_0	Note
Register	Mode Register Set		H	X	L	L	L	L	X	OP CODE			1, 2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank Active & Row Addr.			H	X	L	L	H	H	X	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address (A_0~A_8)	4
	Auto Precharge Enable										H		4, 5
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address (A_0~A_8)	4
	Auto Precharge Enable										H		4, 5
Burst Stop			H	X	L	H	H	L	X	X			6
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	Both Banks									X	H		
Clock Suspend or Active Power Down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No Operation Command			H	X	H	X	X	X	X	X			
					L	H	H	H					

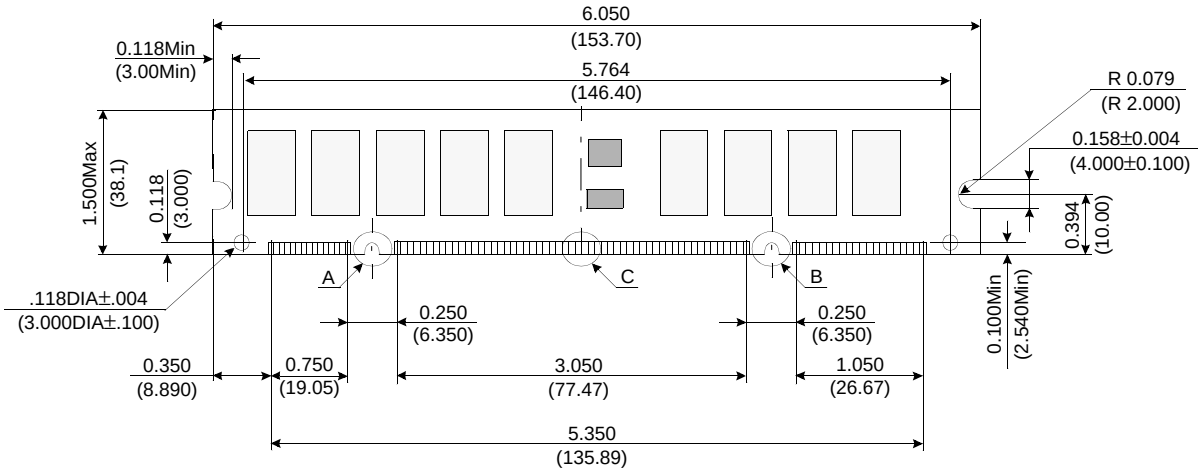
(V=Valid, X=Dont Care, H=Logic High, L=Logic Low)

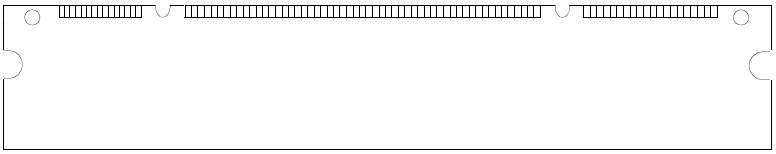
Note :

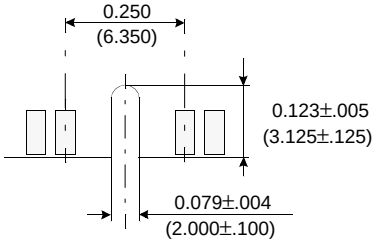
1. OP Code : Operand code
   A_0 ~ A_{11} & BA_0 ~ BA_1 : Program keys. (@ MRS)
2. MRS can be issued only at all banks precharge state.
   A new command can be issued after 2 clock cycles of MRS.
3. Auto refresh functions are as same as CBR refresh of DRAM.
   The automatical precharge without row precharge command is meant by "Auto".
   Auto/self refresh can be issued only at all banks precharge state.
4. BA_0 ~ BA_1 : Bank select addresses.
   If both BA_0 and BA_1 are "Low" at read, write, row active and precharge, bank A is selected.
   If both BA_0 is "Low" and BA_1 is "High" at read, write, row active and precharge, bank B is selected.
   If both BA_0 is "High" and BA_1 is "Low" at read, write, row active and precharge, bank C is selected.
   If both BA_0 and BA_1 are "High" at read, write, row active and precharge, bank D is selected.
   If A_{10}/AP is "High" at row precharge, BA_0 and BA_1 is ignored and all banks are selected.
5. During burst read or write with auto precharge, new read/write command can not be issued.
   Another bank read/write command can be issued after the end of burst.
   New row active of the associated bank can be issued at t_{RP} after the end of burst.
6. Burst stop command is valid at every burst length.
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

PACKAGE DIMENSIONS

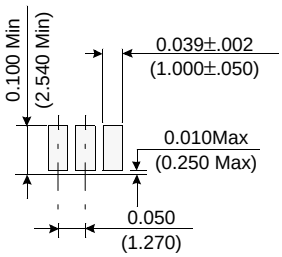
Units : Inches (millimeters)



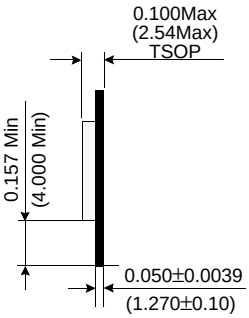




Detail A & B



Detail C



Tolerances :± 0.005(.13) unless otherwise specified

The used device is 8Mx8 SDRAM, TSOPII (Forward)
SDRAM Part No. : KM48S8030CT-GL
PLL Part No. : CDC2586
Drive IC : SN74ALVCH162721