SPECIFICATION

Character Type Dot Matrix LCD Module

JCM121A

SHENZHEN JINGHUA DISPLAYS CO.,LTD.

● GENERAL SPECIFICATION

12 characters X 1line display

LCD driver: KS0066

Interface with Z80, 8088, 8051 MPU

Display Specification

Display Mode: Positive mode

Display type: TN or STN

Polarizer mode: Transflective

Viewing angle: 6:00

Display duty: 1/16

Driving bias: 1/5

Mechanical characteristics (Unit:mm)

Extenal dimension: 59.0X16.0X11.0

View area: 49.0X9.0

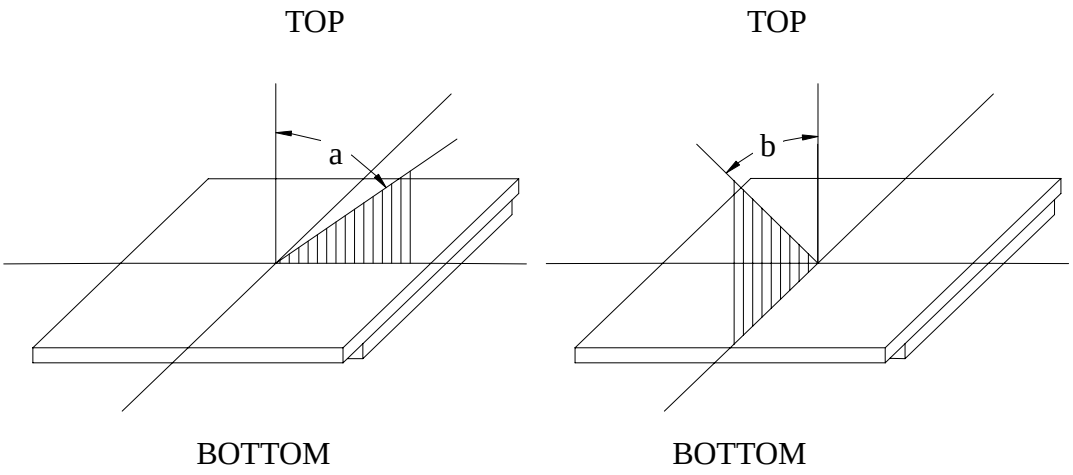
Dot size: 0.6X0.68

Dot pitch: 0.67X0.75

POWER: +5V power

● Optical Characteristics

(1) Definition of viewing Angle



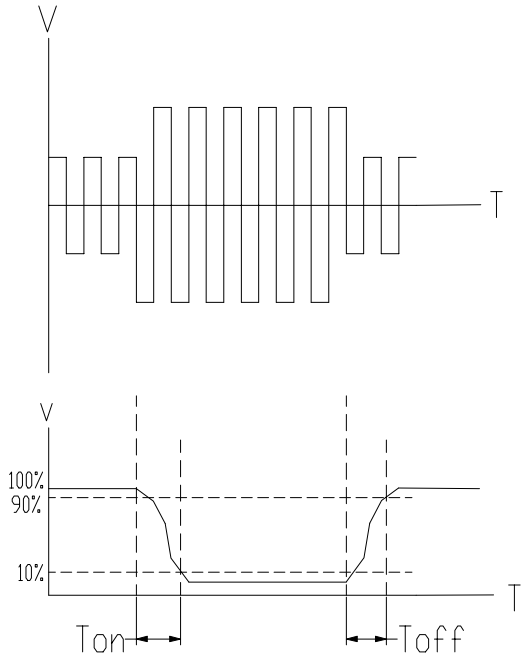
(2) Definition of Contrast Ratio:

$$\text{Contrast Ratio} = \frac{\text{Reflectance value of non-selected state brightness}}{\text{Reflectance value of selected state brightness}}$$

Test condition : standard A light source

(3) Response Time

Response time is measured as the shortest period of time possible between the change in state of an LCD segment as demonstrated below



● Absolute Maximum Ratings

Item	Symbol	Condition	Standard Value		Unit
			min	max	
Supply Voltage for logic	Vdd-Vss	Ta=25℃	-0.3	7.0	V
Supply Voltage for LCD	Vdd-Vee		-	7.0	V
Input Voltage	V1		-0.3	Vdd+0.3	V
Operating Temperature	Top	-	-10	50	℃
Storage Temperature	Tstg	-	-20	70	℃

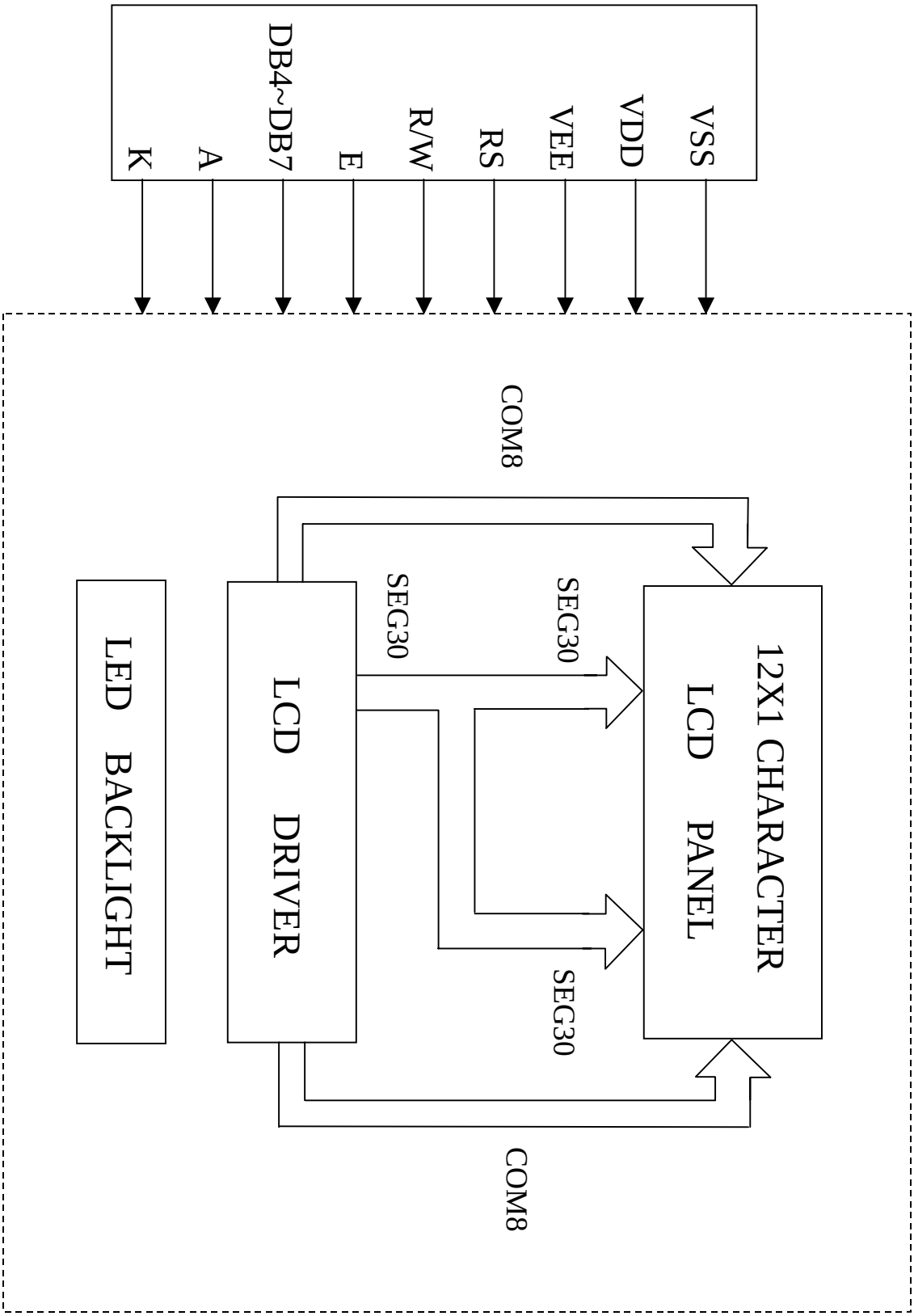
● Electrical Characteristics (Ta=25℃, Vdd= 5.0V)

Item	Symbol	Condition	Standard Value			Unit
			min	Type	max	
Supply Voltage for logic	Vdd-Vss	-	4.75	5.0	5.25	V
Supply Current for logic	Idd	Vdd=5.0	-	1.0	-	mA
Driving Current for LCD	Iee	Vee=-8.5	-	0.43	-	mA
Driving Voltage for LCD	Vdd-Vee	25℃	-	4.8	-	V
Input Voltage “H” level	V_{IH}	H	0.7Vdd	-	Vdd	V
Input Voltage “L” level	V_{IL}	L	Vss	-	0.3Vdd	V

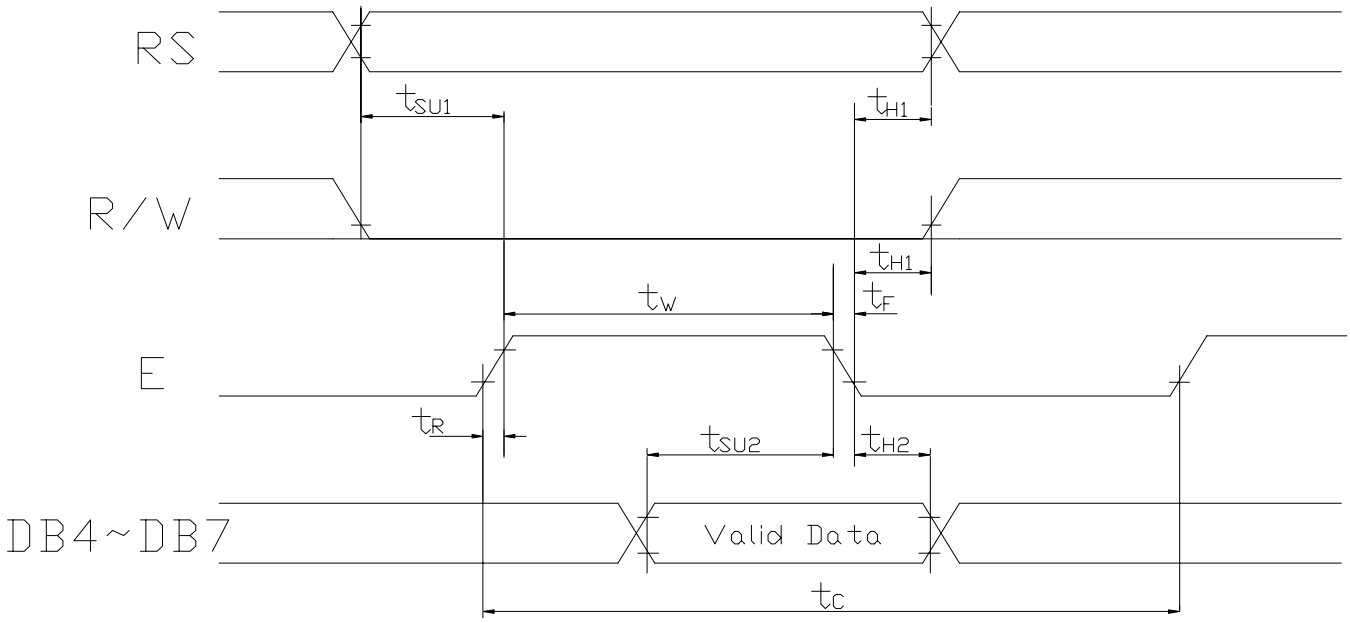
● Absolute Maximum Ratings For LED Backlight

Parameter	Symbol	Test condition	Min	Type	Max	Unit
LED Forward Consumption Current	I_f	Ta=25℃ Vf=4.1V	-	40	80	mA
LED Allowable Dissipation	P_d		-	160	320	mW

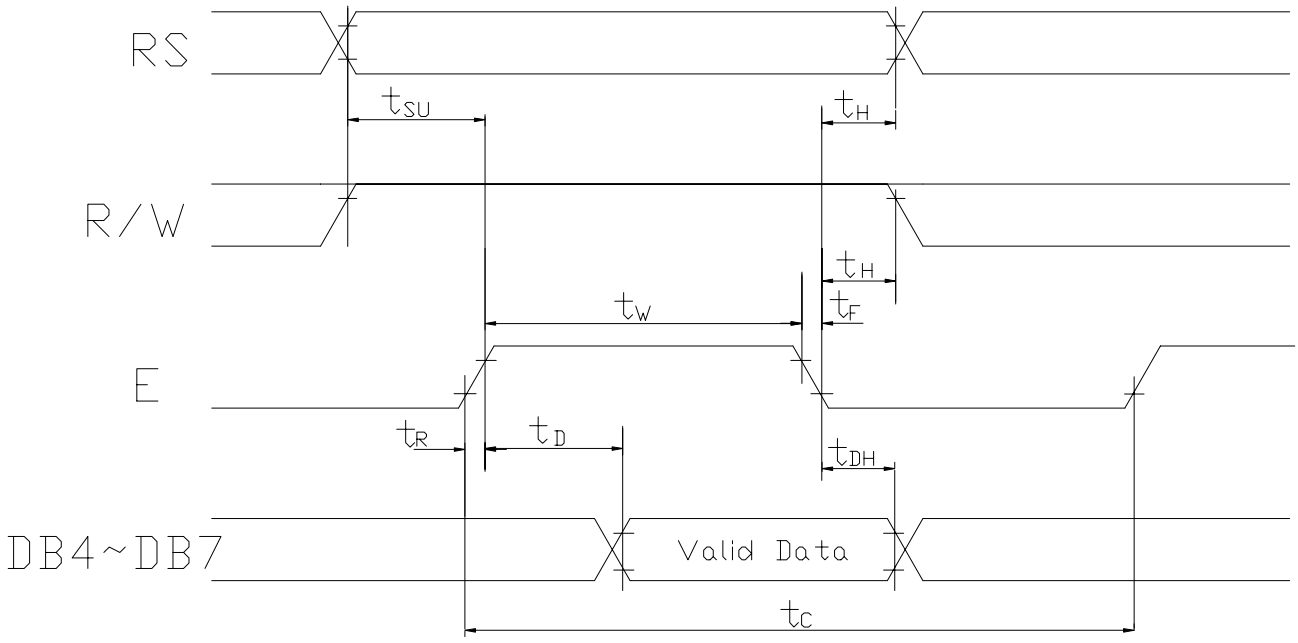
- **Block Diagram**



- **Bus Timing**



Write Mode Timing Diagram



Read Mode Timing Diagram

● AC Characteristics (Vdd=2.7V~4.5V,Ta=-30~+85℃)

Mode	Characteristic	Symbol	Min.	Typ.	Max.	Unit
Write Mode	E Cycle Time	t_C	1000	-	-	ns
	E Rise/Fall Time	t_R,t_F	-	-	25	
	E Pulse Width (High,Low)	t_W	450	-	-	
	R/W and RS Setup Time	t_{SU1}	60	-	-	
	R/W and RS Hold Time	t_{H1}	20	-	-	
	Data Setup Time	t_{SU2}	195	-	-	
	Data Hold Time	t_{H2}	10	-	-	
Read Mode	E Cycle Time	t_C	1000	-	-	ns
	E Rise/Fall Time	t_R,t_F	-	-	25	
	E Pulse Width (High,Low)	t_W	450	-	-	
	R/W and RS Setup Time	t_{SU}	60	-	-	
	R/W and RS Hold Time	t_H	20	-	-	
	Data Output Delay Time	t_D	-	-	360	
	Data Hold Time	t_{DH}	5	-	-	

● Pin assignment

Pin NO.	Symbol	Function		Remark
1	Vss	Power Supply	0V	
2	Vdd		+5V	
3	Vo		For LCD	Variable
4	RS	H:Data register L:Instruction register		
5	R/W	H:Read L:Write		
6	E	Read/Write enable signal		
7	DB4	Data Bit 4		
8	DB5	Data Bit 5		
9	DB6	Data Bit 6		
10	DB7	Data Bit 7		
11	A	LED+		
12	K	LED-		

● Instruction Table

Instruction	Instruction Code										Description	Execution Time(fosc= 270kHz)
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Clear Display	0	0	0	0	0	0	0	0	0	1	Write"20H" to DDRAM set DDRAM address to "00H" from AC	1.53ms
Return Home	0	0	0	0	0	0	0	0	1	-	Set DDRAM address to "00H" from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed	1.53ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	SH	Assign cursor moving direction and enable the shift of entire display	39 μ s
Display ON/OFF Control	0	0	0	0	0	0	1	D	C	B	Set display(D) cursor(C) and blinking of cursor(B) on/off	39 μ s
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	-	-	Set cursor moving and display shift control bit,and the direction, without changing DDRAM data	39 μ s
Function Set	0	0	0	0	1	DL	N	F	-	-	Set interface data length(DL:8bit/4bit), number of display line (N:2line/1line) and,display font type F:5X11dots / 5X8dots	39 μ s
Set CGRAM Address	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address counter	39 μ s
Set DDRAM Address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address counter	39 μ s
Read Busy Flag and Address	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Whether during internal operation or not can be known by reading BF The contents of address counter can also be read	0 μ s
Write Data to RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM (DDRAM/CGRAM)	43 μ s
Read data from RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM/CGRAM)	43 μ s

● Instruction Description

A. Clear Display

RS	R/W	DB7	DB6	DB5	DB4
0	0	0	0	0	0
RS	R/W	DB7	DB6	DB5	DB4
0	0	0	0	0	1

Clear all the display data by writing “20H”(space code) to all DDRAM address,and set DDRAM address to “00H” into AC(address counter).
Return cursor to the original status,namely,bring the cursor to the left edge on the first line of the display.
Make the entry mode increment(I/D=”High”).

B. Return Home

RS	R/W	DB7	DB6	DB5	DB4
0	0	0	0	0	0
RS	R/W	DB7	DB6	DB5	DB4
0	0	0	0	1	-

Set DDRAM address to “00H” into the address counter.
Return cursor to its original site and return display to its original status,if shifted.
Contents of DDRAM does not change.

C. Entry Mode Set

RS	R/W	DB7	DB6	DB5	DB4
0	0	0	0	0	0
RS	R/W	DB7	DB6	DB5	DB4
0	0	0	1	I/D	SH

Set the moving direction of cursor and display.

I/D:Increment /decrement of DDRAM address(cursor or blink)

I/D=High,cursor/blink moves to right and DDRAM address is increased by 1.

I/D=low,cursor/blink moves to left and DDRAM address is decreased by 1.

*CGRAM operates the same way as DDRAM, when reading from or writing to CGRAM.

SH:Shift of entire display

When DDRAM read (CGRAM read/write) operation or SH=Low,shifting of entire display is not performed.if SH=High, and DDRAM write operation,shift of entire display is performed according to I/D value(I/D=High,shift left,I/D=Low, shift right).

D. Display ON/OFF Control

RS	R/W	DB7	DB6	DB5	DB4
0	0	0	0	0	0
RS	R/W	DB7	DB6	DB5	DB4
0	0	1	D	C	B

D:Display ON/OFF control bit

When D=High, entire display is turned on.

When D=Low, display is turned off,but display data remains in DDRAM.

C:Cursor ON/OFF control bit

When C=High, cursor is turned on.

When C=Low, cursor is disappeared in current display ,but I/D register preserves its data.

B:Cursor Blink ON/OFF control bit

When B=High, cursor blink is on, which performs alternately between all the “High” data and display characters at the cursor position.

When B=Low ,blink is off.

E. Cursor or Display Shift

RS	R/W	DB7	DB6	DB5	DB4
0	0	0	0	0	1
RS	R/W	DB7	DB6	DB5	DB4
0	0	S/C	R/L	-	-

Shifting of right/left cursor position or display without writing or reading of display data.

This instruction is used to correct or search display data.

During 2-line mode display,cursor moves to the 2^{nd} line after the 40^{th} digit of the 1^{st} line.

Note that display shift is performed simultaneously in all the lines.

When displayed data is shifted repeatedly,each line is shifted individually.

When display shift is performed,the contents of the address counter are not changed.

S/C	R/L	Operation
0	0	Shift cursor to the left, AC is decreased by1
0	1	Shift cursor to the right, AC is increased by1
1	0	Shift all the display to the left,cursor moves according to the display
1	1	Shift all the display to the right,cursor moves according to the display

F. Function set

RS	R/W	DB7	DB6	DB5	DB4
0	0	0	0	1	DL
RS	R/W	DB7	DB6	DB5	DB4
0	0	N	F	-	-

DL:Interface data length control bit
When DL=High, it means 8-bit bus mode with MPU.
When DL=Low, it means 4-bit bus mode with MPU.
When 4-bit bus mode, it needs to transfer 4-bit data twice.
N:Display line number control bit
When N=Low, 1-line display mode is set.
When N=High, 2-line display mode is set.
F:Display font type control bit
When F=Low, 5x8 dots format display mode is set.
When F=High, 5x11 dots format display mode.

G. Set CGRAM Address

RS	R/W	DB7	DB6	DB5	DB4
0	0	0	1	AC5	AC4
RS	R/W	DB7	DB6	DB5	DB4
0	0	AC3	AC2	AC1	AC0

Set CGRAM address to AC.
This instruction makes CGRAM data available from MPU.

H. Set DDRAM Address

RS	R/W	DB7	DB6	DB5	DB4
0	0	1	AC6	AC5	AC4
RS	R/W	DB7	DB6	DB5	DB4
0	0	AC3	AC2	AC1	AC0

Set DDRAM address to AC.
This instruction makes DDRAM data available from MPU.
When 1-line display mode(N=Low),DDRAM address is from “00H” to “4FH”.
In 2-line display mode(N=High),DDRAM address in the 1st line is from “00H” to “27H”,and DDRAM address in the 2nd line is from “40H” to “67H”.

I. Read Busy Flag & Address

RS	R/W	DB7	DB6	DB5	DB4
0	1	BF	AC6	AC5	AC4
RS	R/W	DB7	DB6	DB5	DB4
0	1	AC3	AC2	AC1	AC0

This instruction shows whether IC is in internal operation or not .
If BF is “High”,internal operation is in progress and should wait until BF is to be Low,which by then the next instruction can be performed. In this instruction you can also read the value of the address counter.

J. Write data to RAM

RS	R/W	DB7	DB6	DB5	DB4
1	0	D7	D6	D5	D4
RS	R/W	DB7	DB6	DB5	DB4
1	0	D3	D2	D1	D0

Write binary 8-bit data to DDRAM/CGRAM.
The selection of RAM from DDRAM,and CGRAM,is set by the previous address set instruction(DDRAM address set,CGRAM address set).
RAM set instruction can also determine the AC direction to RAM.
After write operation, the address is automatically increased /decreased by 1,according the entry mode.

K. Read data from RAM

RS	R/W	DB7	DB6	DB5	DB4
1	1	D7	D6	D5	D4
RS	R/W	DB7	DB6	DB5	DB4
1	1	D3	D2	D1	D0

Read binary 8-bit data from DDRAM/CGRAM.
The selection of RAM is set by the previous address set instruction.If the address set instruction of RAM is not performed before this instruction, the data that has been read first is invalid, as the direction of AC is not yet determined. If RAM data is read several times without RAM address instructions set before read operation,the correct RAM data can be obtained from the second. But the first data would be incorrect,as there is no time margin to transfer RAM data.
In case of DDRAM read operation,cursor shift instruction plays the same role as DDRAM

address set instruction,it also transfers RAM data to output data register.

After read operation,address counter is automatically increased/decreased by 1 according to the entry mode.

After CGRAM read operation,display shift may not be executed correctly.

Note:In case of RAM write operation,AC is increased/decreased by 1 as in read operation. At this time,AC indicates the next address position, but only the previous data can be read by the read instruction.

● Relationship between Character Code and CGRAM

Character code								CGRAM Address						CGRAM Data								Pattern number
D7	D6	D5	D4	D3	D2	D1	D0	A5	A4	A3	A2	A1	A0	P7	P6	P5	P4	P3	P2	P1	P0	
0	0	0	0	x	0	0	0	0	0	0	0	0	0	x	x	x	0	1	1	1	0	pattern 1
											0	0	1	x	x	x	1	0	0	0	1	
											0	1	0	x	x	x	1	0	0	0	1	
											0	1	1	x	x	x	1	1	1	1	1	
											1	0	0	x	x	x	1	0	0	0	1	
											1	0	1	x	x	x	1	0	0	0	1	
											1	1	0	x	x	x	1	0	0	0	1	
											1	1	1	x	x	x	0	0	0	0	0	
0	0	0	0	x	1	1	1	0	0	0	0	0	0	x	x	x	1	0	0	0	1	pattern8
											0	0	1	x	x	x	1	0	0	0	1	
											0	1	0	x	x	x	1	0	0	0	1	
											0	1	1	x	x	x	1	1	1	1	1	
											1	0	0	x	x	x	1	0	0	0	1	
											1	0	1	x	x	x	1	0	0	0	1	
											1	1	0	x	x	x	1	0	0	0	1	
											1	1	1	x	x	x	0	0	0	0	0	

● Display Data RAM(DDRAM)

DDRAM stores display data of maximum 80x8 bits(80 characters).

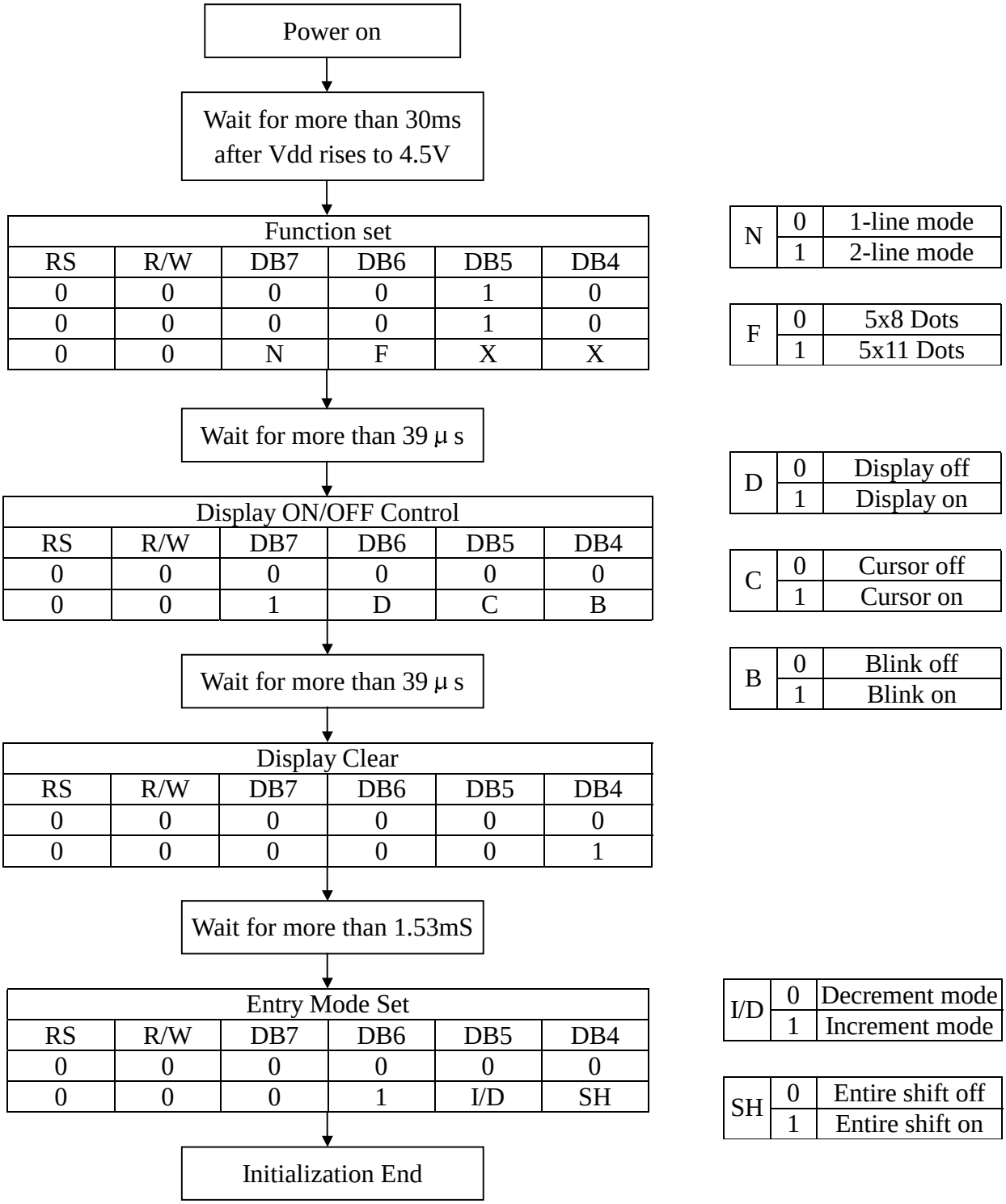
DDRAM address is set in the address counter(AC) as a hexadecimal number

MSB						LSB
AC6	AC5	AC4	AC3	AC2	AC1	AC0

● Reflector of Screen and DDRAM Address

Disp position	1	2	3	4	5	6						
DDRAM addr	00	01	02	03	04	05	06	---	1F	---	26	27
Disp position	7	8	9	10	11	12						
DDRAM addr	40	41	42	43	44	45	46	---	5F	---	66	67

● Initializing Flowchart(Condition:fosc=270KHZ)



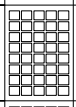
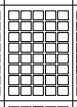
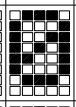
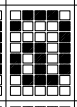
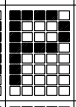
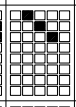
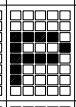
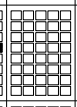
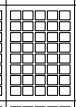
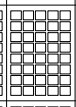
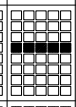
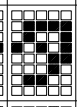
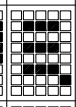
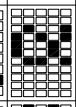
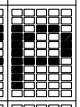
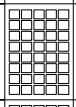
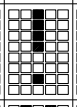
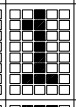
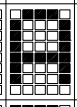
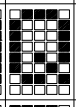
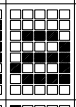
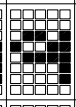
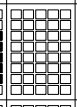
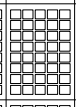
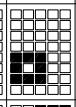
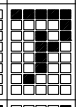
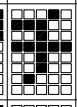
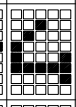
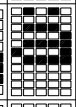
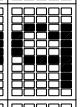
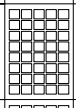
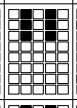
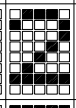
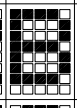
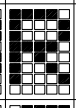
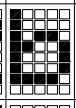
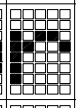
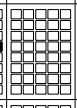
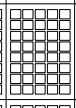
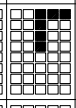
● Programm Example

```
INIT:
        LCALL T3        ;DELAY 30mS
        CLR RS
        CLR R/W
        MOV A,#20H
        MOV P1,A
        SETB E
        LCALL T1
        CLR E
        MOV   R0,#28H   ;SET 2LINE MODE,5X8DOTS
        LCALL WRITE
        LCALL T2        ;DELAY 39 μ s
        MOV R0,#0CH     ;DISPLAY ON
        LCALL WRITE
        LCALL T2        ;DELAY 39 μ s
        MOV R0,#01H     ;DISPLAY CLEAR
        LCALL WRITE
        LCALL T4        ;DELAY 1.53ms
        MOV R0,#06H     ;SET INCREMENT MODE
        LCALL WRITE
        LCALL T2        ;DELAY 39 μ s
        MOV R0,#03H     ;RETURN HOME
        LCALL WRITE
        LCALL T2        ;DELAY 39 μ s
MAIN:
        MOV DPTR,#TAB1
        MOV R0,#80H     ;SET DDRAM ADDRESS TO “00H”
        LCALL WRITE
        SETB RS
        MOV R3,#06H     ;WRITE TAB1 TO DDRAM FROM “00H” TO “05H”
WD1:CLR A
        MOVC A,@A+DPTR
        MOV R0,A
        LCALL WRITE
        INC DPTR
        DJNZ R3,WD1
        MOV DPTR,#TAB1
        MOV R0,#0C0H    ;SET DDRAM ADDRESS TO “40H”
        LCALL WRITE
```

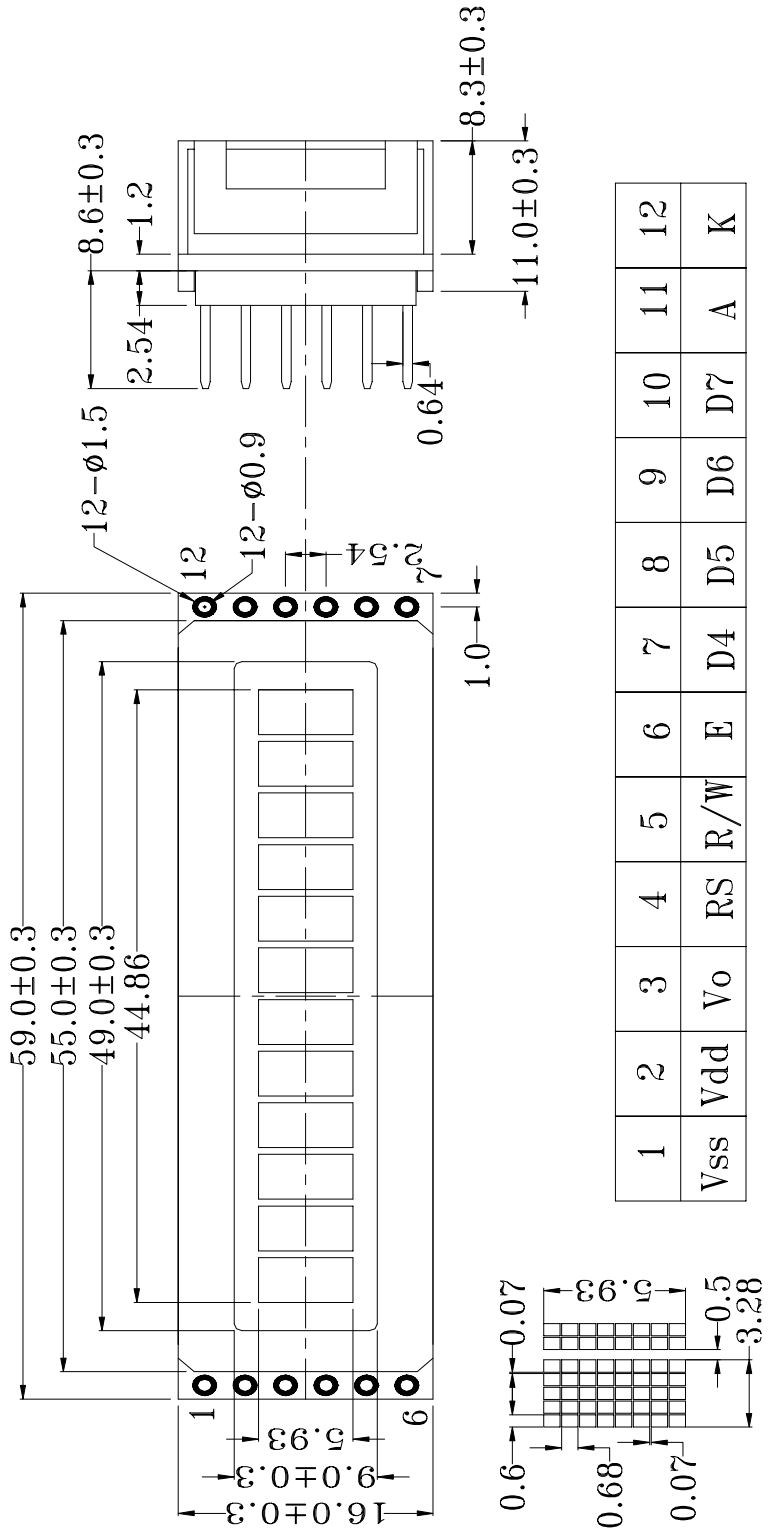
```
        SETB RS
        MOV R3,#06H       ;WRITE TAB1 TO DDRAM FROM “40H” TO “45H”
WD2:CLR A
        MOVC A,@A+DPTR
        MOV R0,A
        LCALL WRITE
        INC DPTR
        DJNZ R3,WD2

WRITE:
        MOV A,R0
        MOV P1,A
        SETB E
        LCALL T1
        CLR E
        LCALL T5
        MOV A,R0
        SWAP A
        MOV P1,A
        SETB E
        LCALL T1
        CLR E
        LCALL T5
        RET
        END
```

● Character Generator ROM

Upper 4bit / Lower 4bit	LLLL	LLLH	LLHL	LLHH	LHLL	LHLH	LHHL	LHHH	HLLL	HLLH	HLHL	HLHH	HHLL	HHLH	HHHL	HHHH
LLLL	CG RAM (1)															
LLLH	(2)															
LLHL	(3)															
LLHH	(4)															
LHLL	(5)															
LHLH	(6)															
LHHL	(7)															
LHHH	(8)															
HLLL	(1)															
HLLH	(2)															
HLHL	(3)															
HLHH	(4)															
HHLL	(5)															
HHLH	(6)															
HHHL	(7)															
HHHH	(8)															

- **Extenal Dimension**



1	2	3	4	5	6	7	8	9	10	11	12
Vss	Vdd	Vo	RS	R/W	E	D4	D5	D6	D7	A	K