National Semiconductor

MICROCIRCUIT DATA SHEET

MJLF198-X REV 2B0

Original Creation Date: 07/20/95
Last Update Date: 11/02/00
Last Major Revision Date: 08/02/00

SAMPLE AND HOLD CIRCUIT, 10K OHM LOAD

General Description

The LF198 is a monolithic sample-and-hold circuit which utilize BI-FET technology to obtain ultra-high dc accuracy with fast acquisition of signal and low droop rate. Operating as a unity gain follower, dc gain accuracy is 0.002% typical and acquisition time is as low as 6 us to 0.01%. A bipolar input stage is used to achieve low offset voltage and wide bandwidth. Input offset adjust is accomplished with a single pin, and does not degrade input offset drift. The wide bandwidth allows the LF198 to be included inside the feedback loop of 1 MHz op amps without having stability problems. Input impedance of 10(10) ohms allows high source impedances to be used without degrading accuracy.

P-channel junction FETs are combined with bipolar devices in the output amplifier to give droop rates as low as 5 mV/min with a 1uF hold capacitor. The JFETs have much lower noise than MOS devices used in previous designs and do not exhibit high temperature instabilities. The overall design guarantees no feed-through from input to output in the hold mode, even for input signals equal to the supply voltages.

Logic inputs on the LF198 are fully differential with low input current, allowing direct connection to TTL, PMOS, and CMOS. Differential theshold is 1.4V. The LF198 will operate from $\pm$5V to $\pm$18V supplies.

Industry Part Number

LF198

NS Part Numbers

JL198BGA
JL198SGA

Prime Die

LF198

Controlling Document

38510/12501

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (^{O}C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- Operates from ±5V to ±18V supplies
- Less than 10uS acquisition time
- TTL, PMOS, CMOS compatible logic input
- 0.5mV typical hold step at Cn = 0.01uF
- Low input offset
- 0.002% gain accuracy
- Low output noise in hold mode
- Input characteristics do not change during hold mode
- High supply rejection ratio in sample or hold
- Wide bandwidth
- Space qualified

(Absolute Maximum Ratings)

(Note 1)

Supply Voltage	±18V
Power Dissipation (Note 2) (Package Limitation)	500mW
Operating Ambient Temperature Range	-55 C ≤ Ta ≤ +125 C
Storage Temperature Range	-65 C to +150 C
Input Voltage	Equal To Supply Vol.
Logic to Logic Ref. Diff. Voltage (Note 3)	+7V, -30V
Output Short Circuit Duration	Indefinite
Hold Capacitor Short Circuit Duration	10 seconds
Lead Temperature (Soldering, 10 seconds)	300 C
Thermal Resistance	
ThetaJA	
Metal Can	
Still Air @ 0.5W	160 C/W
500LF/Min Air flow @ 0.5W	84 C/W
ThetaJC	
Metal Can	48 C/W
ESD Tolerance (Note 4)	500V

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by Tjmax (maximum junction temperature), ThetaJA (package junction to ambient thermal resistance), and TA (ambient temperature). The maximum allowable power dissipation at any tempeature is Pdmax - (Tjmax - TA)/ThetaJA or the number given in the Absolute Maximum Ratings, whichever is lower.

Note 3: Although the differential voltage may not exceed the limits given, the common-mode voltage on the logic pins may be equal to the supply voltages without causing damage to the circuit. For proper logic operation, however, one of the logic pins must always be at least 2V below the positive supply and 3V above the negative supply.

Note 4: Human body model, 100pF discharged through 1.5k Ohms.

Electrical Characteristics

DC PARAMETERS

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Vio	Input Offset Voltage	+Vcc = 3.5V, -Vcc = -26.5V, Vcm = 11.5V			-3	3	mV	1
					-5	5	mV	2, 3
		+Vcc = 26.5V, -Vcc = -3.5V, Vcm = -11.5V			-3	3	mV	1
					-5	5	mV	2, 3
		+Vcc = 15V, -Vcc = -15V, Vcm = 0V			-3	3	mV	1
					-5	5	mV	2, 3
		+Vcc = 7V, -Vcc = -3V, Vcm = 2V			-3	3	mV	1
					-5	5	mV	2, 3
		+Vcc = 3V, -Vcc = -7V, Vcm = -2V			-3	3	mV	1
					-5	5	mV	2, 3
Iib	Input Bias Current	+Vcc = 3.5V, -Vcc = -26.5V, Vcm = 11.5V			-1	25	nA	1
					-25	75	nA	2, 3
		+Vcc = 26.5V, -Vcc = -3.5V, Vcm = -11.5V			-1	25	nA	1
					-25	75	nA	2, 3
		+Vcc = 15V, -Vcc = -15V, Vcm = 0V			-1	25	nA	1
					-25	75	nA	2, 3
		+Vcc = 7V, -Vcc = -3V, Vcm = 2V			-1	25	nA	1
					-25	75	nA	2, 3
		+Vcc = 3V, -Vcc = -7V, Vcm = -2V			-1	25	nA	1
					-25	75	nA	2, 3
Zi	Input Impedance	+Vcc = 3.5V to 26.6V, -Vcc = -26.5V to -3.5V, Vcm = 11.5V to -11.5V			2		GOhms	1
					1		GOhms	2, 3
Vio adj+	Input Offset Voltage Adjustment	+Vcc = 15V, -Vcc = -15V, Vcm = 0V			6		mV	1, 2, 3
Vio adj-	Input Offset Voltage Adjustment	+Vcc = 15V, -Vcc = -15V, Vcm = 0V				-6	mV	1, 2, 3
PSRR+	Power Supply Rejection Ratio	-Vcc = -18V, +Vcc = 18V to 12V			80		dB	1, 2, 3
PSRR-	Power Supply Rejection Ratio	+Vcc = 18V, -Vcc = -12V to -18V			80		dB	1, 2, 3
Icc	Supply Current	+Vcc = 15V, -Vcc = -15V, Vcm = 0V			1	5.5	mA	1, 2
					1	6.5	mA	3

Electrical Characteristics

DC PARAMETERS(Continued)

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Ae	Gain Error	+Vcc = 3.5V to 26.5V, -Vcc = -26.5V to -3.5V, Vcm = -11.5V to 11.5V			-0.005	0.005	%	1
					-0.02	0.02	%	2, 3
		+Vcc = 3V to 7V, -Vcc = -7V to -3V, Vcm = -2V to 2V			-0.02	0.02	%	1
					-0.04	0.04	%	2, 3
Rsc	Series Charge Resistance	+Vcc = 15V, -Vcc = -15V, Vcm = 0V			75	400	Ohms	1, 2, 3
Iih (a)	Logical 1 Input Current	+Vcc = 8.5V, -Vcc = -21.5V			0	10	uA	1, 2, 3
Iih (b)	Logical 1 Input Current	+Vcc = 8.5V, -Vcc = -21.5V			0	10	uA	1, 2, 3
Iil (a)	Logical 0 Input Current	+Vcc = 21.5V, -Vcc = -8.5V			-1	1	uA	1, 2, 3
Iil (b)	Logical 0 Input Current	+Vcc = 21.5V, -Vcc = -8.5V			-1	1	uA	1, 2, 3
Ios+	Output Short Circuit Current	+Vcc = 15V, -Vcc = -15V, Vcm = 0V			-25		mA	1, 2, 3
Ios-	Output Short Circuit Current	+Vcc = 15V, -Vcc = -15V, Vcm = 0V				25	mA	1, 2, 3
Ich+	Hold Capacitor Charge Current	+Vcc = 15V, -Vcc = -15V, Vcm = 0V				-3	mA	1
						-2	mA	2, 3
Ich-	Hold Capacitor Charge Current	+Vcc = 15V, -Vcc = -15V, Vcm = 0V			3		mA	1
					2		mA	2, 3
Vth(H)	Differential Logic Threshold	+Vcc = 15V, -Vcc = -15V, Vcm = 0V Logic = 2.0V, Logic Ref = 2.0V			1		mA	1, 2, 3
Vth(L)	Differential Logic Threshold	+Vcc = 15V, -Vcc = -15V, Vcm = 0V Logic = 0.8V, Logic Ref = 2.0V			-10	10	uA	1, 2, 3
Ihl+	Hold Mode Leakage Current	+Vcc = 3.5V, -Vcc = -26.5V, Vcm = -11.5V			-0.100	0.100	nA	1
					-50	50	nA	2
Ihl-	Hold Mode Leakage Current	+Vcc = 26.5V, -Vcc = -3.5V, Vcm = 11.5V			-0.100	0.100	nA	1
					-50	50	nA	2
Zo	Output Impedance	+Vcc = 15V, -Vcc = -15V, Vcm = 0V				2	Ohms	1, 2, 3
Vhs	(HOLD) Step Voltage	+Vcc = 3.5V, -Vcc = -26.5V, Vcm = 11.5V			-2	2	mV	1
					-5	5	mV	2, 3
		+Vcc = 26.5V, -Vcc = -3.5V, Vcm = -11.5V			-2	2	mV	1
					-5	5	mV	2, 3

Electrical Characteristics

DC PARAMETERS(Continued)

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Frr	Feedthrough Rejection Ratio	+Vcc = 15V, -Vcc = -15V, Vcm = 0V, Vin = 0V to 11.5V			86		dB	1
					80		dB	2, 3
		+Vcc = 15V, -Vcc = -15V, Vcm = 0V, Vin = 11.5V to 0V			86		dB	1
					80		dB	2, 3
		+Vcc = 15V, -Vcc = -15V, Vcm = 0V, Vin = 0V to -11.5V			86		dB	1
					80		dB	2, 3
		+Vcc = 15V, -Vcc = -15V, Vcm = 0V, Vin = -11.5V to 0V			86		dB	1
					80		dB	2, 3

AC/DC PARAMETERS

Delta Vio/Delta T	Input Offset Voltage Temp Sensitivity		1		-20	20	uV/ C	8A, 8B
taq	Aquisition Time	+Vcc = 15V, -Vcc = -15V	2			25	uS	7
tap	Aperture Time	+Vcc = 15V, -Vcc = -15V	2			300	nS	7
ts	Settling Time	+Vcc = 15V, -Vcc = -15V	2			1.5	uS	7
Frr AC	Feedthrough Rejection Ratio	+Vcc = 15V, -Vcc = -15V, Vin = 20Vpp	2		86		dB	7
TR(ts)	Transient Response (settling time)	+Vcc = 3.5V, -Vcc = -26.5V, Vin = 100mV pulse	2			2.5	uS	7
		+Vcc = 26.5V, -Vcc = -3.5V, Vin = 100mV pulse	2			2.5	uS	7
TR(os)	Transient Response (Overshoot)	+Vcc = 3.5V, -Vcc = -26.5V, Vin = 100mV pulse	2			40	%	7
		+Vcc = 26.5V, -Vcc = -3.5V, Vin = 100mV pulse	2			40	%	7
en (H)	Noise	+Vcc = 15V, -Vcc = -15V	2			10	mVRMS	7
en (S)	Noise	+Vcc = 15V, -Vcc = -15V	2			10	mVRMS	7

DC PARAMETERS: DRIFT VALUES

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: "Delta calculations performed on JAN S and QMLV devices at group B, subgroup 5 only".

Vio	Input Offset Voltage	+Vcc = 15V, -Vcc = -15V, Vcm = 0V			-0.5	0.5	mV	1
Iib	Input Bias Current	+Vcc = 15V, -Vcc = -15V, Vcm = 0V			-2.5	2.5	nA	1

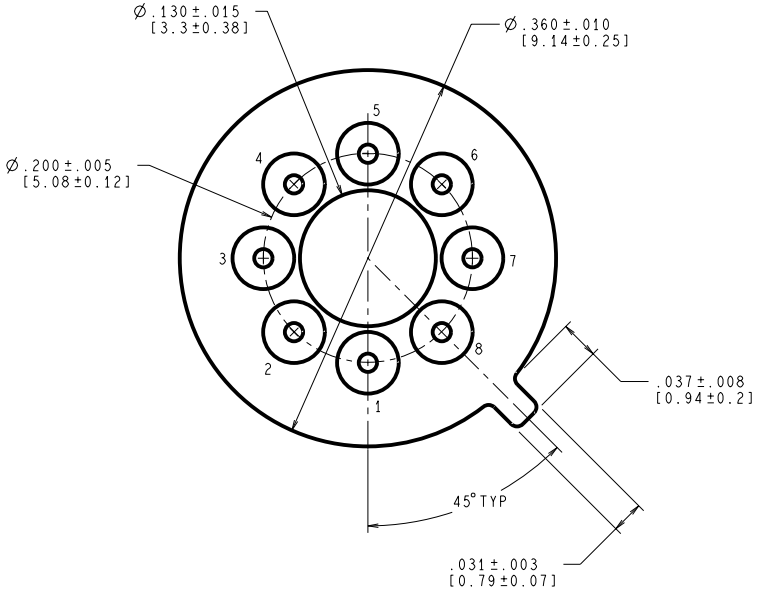
Note 1: Calculated parameters.
Note 2: Bench test.

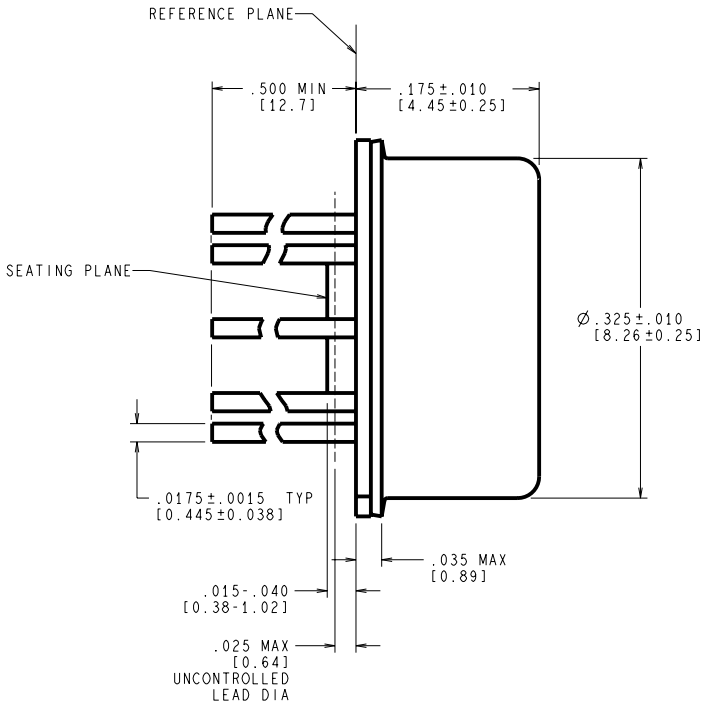
Graphics and Diagrams

GRAPHICS#	DESCRIPTION
05022HRC1	METAL CAN (H), TO-99, 8LD .200 DIA P.C. (B/I CKT)
06068HRA2	METAL CAN (H), TO-99, 8LD .200 DIA P.C. (B/I CKT)
06069HRA2	METAL CAN (H), TO-99, 8LD .200 DIA P.C. (B/I CKT)
H08CRF	METAL CAN (H), TO-99, 8LD, .200 DIA P.C. (P/P DWG)
P000194A	METAL CAN (H), TO-99, 8LD, .200 DIA P.C. (PINOUT)

See attached graphics following this page.

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
F	REVISE & REDRAW PER CURRENT STANDARD; UPDATE MIL/AERO STAMP & TITLE.	11002	06/22/95	MS/





CONTROLLING DIMENSION IS INCH
VALUES IN [] ARE MILLIMETERS

MIL-I-38535
CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEADS TO BE LOCATED WITHIN .007 IN/ 0.18 mm OF THEIR TRUE POSITIONS RELATIVE TO A MAXIMUM WIDTH TAB.
2. STANDARD METAL CAN TYPE: SOLID BASE WITH CERAMIC STANDOFF.
3. APPLIES TO MIL-AERO AND LINEAR PRODUCTS.
4. REFERENCE JEDEC REGISTRATION TO-99, JEDEC PUBLICATION No.95.

APPROVALS	DATE
DRAWN: MARTA SUCHY	06/22/95
DFTG. CHK.	
ENGR. CHK.	

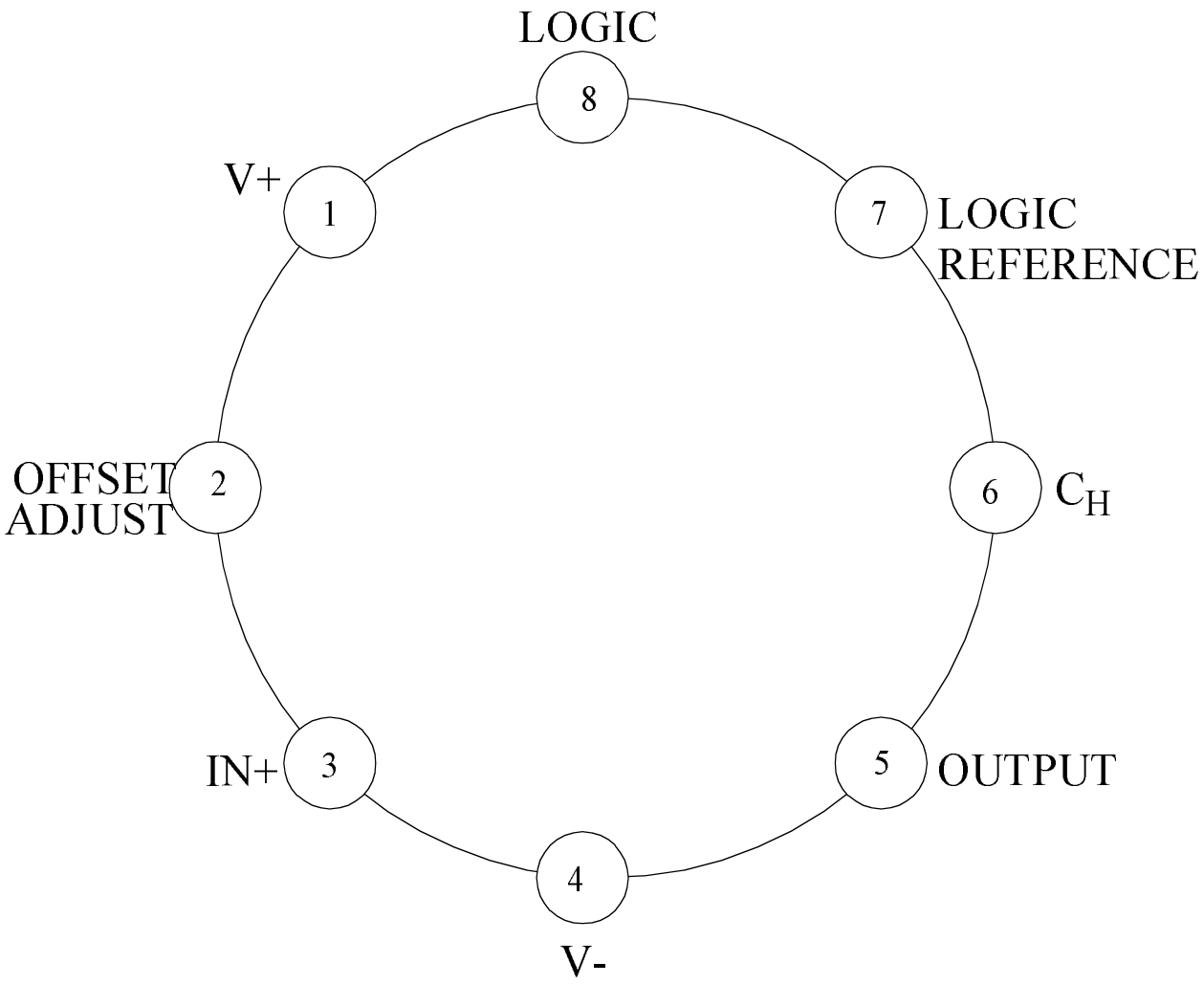
National Semiconductor
2900 Semiconductor dr, Santa Clara, CA 95052-8090

METAL CAN, TO-99, 8 LEAD, .200 DIA P.C.

PROJECTION — INCH [MM]

SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	MKT-H08C	F

DO NOT SCALE DRAWING — SHEET 1 of 1



LF198H
8 - PIN METAL CAN
CONNECTION DIAGRAM
TOP VIEW
P000194A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050

Revision History

Rev	ECN #	Rel Date	Originator	Changes
1A0	M0003625	08/04/00	Rose Malone	Update MDS - MJLF198-X, Rev. 0CL to MJLF198-X, Rev. 1A0 Fully Released MDS Data Sheet. Parameter PSRR-Condition changed from +Vcc = 18V, -Vcc = -12V. Is Now , +Vcc = 18V, -Vcc = -12V to -18V. Changed parameter to agree with test program.
2A0	M0003738	11/02/00	Rose Malone	Update MDS: MJLF198-X, Rev. 1A0 to MJLF198-X, Rev. 2A0. Addition in Electrical Section, Conditions for Vth(H) and Vth(L). For Clarification.
2B0	M0003766	11/02/00	Rose Malone	Update MDS: MJLF198-X, Rev. 2A0 to MJLF198-X, Rev. 2B0. Added ESD parameter. This is a resend previous ECN notification had a TYPO error in the ECN Change Section.