National Semiconductor

MICROCIRCUIT DATA SHEET

MJCD4020A-X REV 1A0

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14-STAGE RIPPLE CARRY BINARY COUNTERS

General Description

The counter is advanced one count on the negative transition of each clock pulse. The counter is reset to the zero state by a logical "1" at the reset input independent of clock.

Industry Part Number

CD4020A

NS Part Numbers

JM4020ABEA

Prime Die

CD4020A

Controlling Document

38510/05603, amend. #1

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

(Absolute Maximum Ratings)
(Note 1, 2)

Voltage at Any Pin	-0.5V to Vdd +0.5V
Power Dissipation (Pd)	200mW
Vdd Range	-0.5V to +15.5V
Storage Temperature (Ts)	-65C to +150C
Lead Temperature (Soldering, 10 seconds)	300C
Input Current (each input)	± 10mA
Thermal Resistance, junction to case	See MIL-STD-1835
Maximum Junction Temperature (Tj max)	175C

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.
Note 2: All voltages measured with respect to Vss unless otherwise specified.

Recommended Operating Conditions

Supply Voltage (VDD)	4.5V to 12.5V
Operating Temperature Range	-55C to +125C
Input Low Voltage Range (VIL)	
VDD=5.0V	0V to 0.85V
VDD=10.0V	0V to 2.0V
VDD=12.5V	0V to 2.1V
Input High Voltage Range (VIH)	
VDD=5.0V	3.95V to 5.0V
VDD=10.0V	8.0V to 10.0V
VDD=12.5V	10.0V to 12.5V

Electrical Characteristics

DC PARAMETERS

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Vic+	Input Clamping Voltage (positive)	VDD=0.0V, VSS=Open, IIN = 1mA	5, 6	INPUTS		1.5	V	1
Vic-	Input Clamping Voltage (negative)	VDD=Open, VSS=Gnd, IIN= -1mA	5, 6	INPUTS		-6.0	V	1
IIH	Input High Current	VDD=15.0V (each input measured separately)	3, 4	INPUTS		100.0	nA	1, 2
IIL	Input Low Current	VDD=15.0V (each input measured separately)	3, 4	INPUTS		-100.0	nA	1, 2
ISS	Power Supply Current	VDD=15.0V, VIH=15.0V, VIL=0.0V, VSS=Gnd, VM=0.0V	3, 4	VSS		-1.0	uA	1
			3, 4	VSS		-10.0	uA	2
VOH1	Output High Voltage	VDD=5.0V, VIL=1.1V, IOH= -90.0uA	1, 2	OUTPUTS	4.5		V	1
		VDD=5.0V, VIL=0.85V, IOH= -65.0uA	1, 2	OUTPUTS	4.5		V	2
		VDD=5.0V, VIL=1.35V, IOH= -110.0uA	1, 2	OUTPUTS	4.5		V	3
VOH2	Output High Voltage	VDD=12.5V, VIL=2.8V, IOH=-0.0mA	1, 2	OUTPUTS	11.25		V	1
		VDD=12.5V, VIL=2.55V, IOH=-0.0mA	1, 2	OUTPUTS	11.25		V	2
		VDD=12.5V, VIL=3.05V, IOH=-0.0mA	1, 2	OUTPUTS	11.25		V	3
VOL1	Output Low Voltage	VDD=5.0V, VIH=3.8V, IOL=100uA	1, 2	OUTPUTS		0.5	V	1
		VDD=5.0V, VIH=3.60V, IOL=90.0uA	1, 2	OUTPUTS		0.5	V	2
		VDD=5.0V, VIH=3.95V, IOL=125.0uA	1, 2	OUTPUTS		0.5	V	3
VOL2	Output Low Voltage	VDD=12.5V, VIH=9.5V, IOL=0.0mA	1, 2	OUTPUTS		1.25	V	1
		VDD=12.5V, VIH=9.25V, IOL=0.0mA	1, 2	OUTPUTS		1.25	V	2
		VDD=12.5V, VIH=9.75V, IOL=0.0mA	1, 2	OUTPUTS		1.25	V	3
VIH	Input High Voltage	VDD=5.0V	1, 2, 9	INPUTS		3.8	V	1
			1, 2, 9	INPUTS		3.6	V	2
			1, 2, 9	INPUTS		3.95	V	3
VIL	Input Low Voltage	VDD=5.0V	1, 2, 9	INPUTS	1.1		V	1
			1, 2, 9	INPUTS	0.85		V	2
			1, 2, 9	INPUTS	1.35		V	3

Electrical Characteristics

FUNCTIONAL PARAMETERS

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
FUNCTION	Functional Test	VDD=5.0V, VIL=0.55V, VIH=4.56V	13, 14	OUTPUTS	L	H		7
		VDD=15.0V, VIL=1.68V, VIH=13.68V	13, 14	OUTPUTS	L	H		7

AC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: VDD=5.0V, CL=50pF, RL=200K Ohms to ground, Tr/Tf=15nS on Clock Pin, tR/tF=30nS on the Reset Pin

tpHL1	Propagation Delay Time		7, 8	Clock to Q1	0.031	0.89	uS	9, 11
			7, 8	Clock to Q1	0.031	1.34	uS	10
			7, 8	Clock to Q4	0.31	3.50	uS	9, 11
			7, 8	Clock to Q4	0.31	5.25	uS	10
			7, 8	Clock to Q5	0.31	4.45	uS	9, 11
			7, 8	Clock to Q5	0.31	6.68	uS	10
			7, 8	Clock to Q6	0.31	5.35	uS	9, 11
			7, 8	Clock to Q6	0.31	8.03	uS	10
			7, 8	Clock to Q7	0.31	6.20	uS	9, 11
			7, 8	Clock to Q7	0.31	9.30	uS	10
			7, 8	Clock to Q8	0.31	7.10	uS	9, 11
			7, 8	Clock to Q8	0.31	10.65	uS	10
			7, 8	Clock to Q9	0.31	8.10	uS	9, 11
			7, 8	Clock to Q9	0.31	12.15	uS	10
			7, 8	Clock to Q10	0.31	8.90	uS	9, 11
			7, 8	Clock to Q10	0.31	13.35	uS	10
			7, 8	Clock to Q11	0.31	9.90	uS	9, 11
			7, 8	Clock to Q11	0.31	14.85	uS	10

Electrical Characteristics

AC PARAMETERS(Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: VDD=5.0V, CL=50pF, RL=200K Ohms to ground, Tr/Tf=15nS on Clock Pin, tR/tF=30nS on the Reset Pin

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
tpHL1	Propagation Delay Time		7, 8	Clock to Q12	0.31	10.70	uS	9, 11
			7, 8	Clock to Q12	0.30	16.05	uS	10
			7, 8	Clock to Q13	0.31	11.60	uS	9, 11
			7, 8	Clock to Q13	0.30	17.40	uS	10
			7, 8	Clock to Q14	0.31	12.50	uS	9, 11
			7, 8	Clock to Q14	0.30	18.75	uS	10
tpLH1	Propagation Delay Time		7, 8	Clock to Q1	0.031	0.89	uS	9, 11
			7, 8	Clock to Q1	0.031	1.34	uS	10
			7, 8	Clock to Q4	0.06	3.50	uS	9, 11
			7, 8	Clock to Q4	0.08	5.25	uS	10
			7, 8	Clock to Q5	0.31	4.45	uS	9, 11
			7, 8	Clock to Q5	0.31	6.68	uS	10
			7, 8	Clock to Q6	0.31	5.35	uS	9, 11
			7, 8	Clock to Q6	0.31	8.03	uS	10
			7, 8	Clock to Q7	0.31	6.20	uS	9, 11
			7, 8	Clock to Q7	0.31	9.30	uS	10
			7, 8	Clock to Q8	0.31	7.10	uS	9, 11
			7, 8	Clock to Q8	0.31	10.65	uS	10
			7, 8	Clock to Q9	0.31	8.10	uS	9, 11
			7, 8	Clock to Q9	0.31	12.15	uS	10
			7, 8	Clock to Q10	0.31	8.90	uS	9, 11
			7, 8	Clock to Q10	0.31	13.35	uS	10

Electrical Characteristics

AC PARAMETERS(Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: VDD=5.0V, CL=50pF, RL=200K Ohms to ground, Tr/Tf=15nS on Clock Pin, tR/tF=30nS on the Reset Pin

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
tpLH1	Propagation Delay Time		7, 8	Clock to Q11	0.31	9.90	uS	9, 11
			7, 8	Clock to Q11	0.31	14.85	uS	10
			7, 8	Clock to Q12	0.31	10.70	uS	9, 11
			7, 8	Clock to Q12	0.30	16.05	uS	10
			7, 8	Clock to Q13	0.31	11.60	uS	9, 11
			7, 8	Clock to Q13	0.30	17.40	uS	10
			7, 8	Clock to Q14	0.31	12.50	uS	9, 11
			7, 8	Clock to Q14	0.30	18.70	uS	10
tpHL2	Propagation Delay Time		7, 8	Reset to Q	0.03	3.30	uS	9, 11
			7, 8	Reset to Q	0.03	4.95	uS	10
tTHL/LH	Transition Time		7, 8	Qn	0.01	1.15	uS	9, 11
			7, 8	Qn	0.02	1.73	uS	10
Cin	Input Capacitance	VDD=Gnd, f=1MHz	10	INPUTS		12	pF	4

DC PARAMETERS: DRIFT VALUES

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Delta calculations performed at production burn-in and Group C (operational life test).

ISS	Power Supply Current	VDD=15.0V, VIH=15.0V, VIL=0.0V, VM=0.0V, VSS=Gnd	12	VSS	-0.25	0.25	uA	1
VOL1	Output Low Voltage	VDD=5.0V, VIH=3.8V, IOL=100uA	12	OUTPUTS	-0.04	0.04	V	1
VOH1	Output High Voltage	VDD=5.0V, VIL=1.1V, IOH= -90.0uA	12	OUTPUTS	-0.08	0.08	V	1

Note 1: Screen tested 100% on each device at +25C, +125C and -55C temperature, subgroups A1, 2 and 3.
Note 2: Sample tested (Method 5005, Table 1) on each MFG. lot at +25C, +125C and -55C temperature, subgroups A1, 2 and 3.
Note 3: Screen tested 100% on each device at +25C and +125C temperature only, subgroup A1 and 2.
Note 4: Sample tested (Method 5005, Table 1) on each MFG. lot at +25C and +125C temperature only, subgroup A1 and 2.
Note 5: Screen tested 100% on each device at +25C temperature only, subgroup A1.

(Continued)

Note 6: Sample tested (Method 5005, Table 1) on each MFG. lot at +25C temperature only, subgroup A1.
Note 7: Screen tested 100% on each device at +25C temperature only, subgroup A9.
Note 8: Sample tested (Method 5005, Table 1) on each MFG. lot at +25C, +125C and -55C temperature, subgroups A9, 10 and 11.
Note 9: VIL, VIH, IOL and IOH are guaranteed by applying specified conditions and testing VOL and VOH.
Note 10: Guaranteed parameter. This test is only performed during initial qualification or after changes to either design or process which may impact capacitance.
Note 11: Guaranteed parameter, not tested.
Note 12: Drift values need not be calculated if post burn-in electrical test is performed within 24 hours after burn-in.
Note 13: Screen tested 100% on each device at +25C temperature only, subgroup 7. "L" is defined as VSS + 0.5V and "H" is defined as VDD - 0.5V.
Note 14: Sample tested (Method 5005, Table 1) on each MFG. lot at +25C temperature only, subgroup 7. "L" is defined as VSS + 0.5V and "H" is defined as VDD - 0.5V.

Revision History

Rev	ECN #	Rel Date	Originator	Changes
1A0	M0003486	03/10/00	Donald B. Miller	1) Archive JRETS4020MX, Rev 4A. Release to MDS, MJCD4020A-X, Rev 1A0. 2) Change IIH from 1nA and 45nA at +25C and +125C respectively to 100nA for both temperatures. 3) Change IIL from -1nA and -45nA at +25C and +125C respectively to -100nA for both temperatures. 4) Added Function symbol.