INTEGRATED FREQUENCY SYNTHESIZERS

Click on package to view outline drawing


124SL


197

HIGH FREQUENCY

FREQUENCY RANGE (MHz)	STEP SIZE (KHz)	DC BIAS REQUIREMENTS Vcc1 & 2 (Volts)	DC BIAS REQUIREMENTS CURRENT Max. (mA)	OUTPUT POWER dBm	OUTPUT POWER Tolerance (dB)	SETTLING TIME (mSec)	TYPICAL PHASE NOISE dBc/Hz Offset at 10 KHz/100 KHz	TYPICAL HARMONIC SUPPRESSION 2nd (dBc)	TYPICAL HARMONIC SUPPRESSION 3rd (dBc)	TYPICAL SPURIOUS REFERENCE SIDEBAND SUPPRESSION (dBc)	PACKAGE	MODEL
1000 - 1800	20	+5/+15	50	+5	+2	<15	-90/-115	15	15	60	197	**SPLH1000SA** Φ
1000 - 2000	1000	+5/+15	35	+5	+2	<15	-92/-120	10	15	60	124SL	**SPLH1000SB** Φ
1000 - 2000	100	+5/+18	40	+5	+2	<20	-92/-120	10	15	50	197	**SPLH1000SD** Φ
1290 - 2000	100	+5/+15	45	+5	+2	<15	-95/-120	10	15	60	124SL	**SPLH1290SA** Φ
1400 - 1600	100	+5/+15	45	+5	+2	<15	-95/-120	20	15	60	124SL	**SPLH1400SA** Φ
1470 - 2070	25	+5/+15	45	+5	+3	<15	-90/-110	10	15	60	124SL	**SPLH1470SA** Φ
1485 - 1635	250	+5/+10.5	45	+5	+3	<20	-95/-120	10	15	60	197	**SPLH1485SA** Φ
1500 - 2050	1500	+5/+15	45	+5	+2	<15	-95/-120	10	15	60	124SL	**SPLH1500SA** Φ
1525 - 1560	10	+5/+5	45	0	+3	<15	-100/-125	20	15	60	124SL	**SPLH1525SA** ¥
1685 - 1780	50	+5/+5	35	0	+3	<20	-90/-115	10	15	60	124SL	**SPLH1685SA** Φ
1750 - 2250	1500	+5/+15	45	+5	+3	<20	-86/-106	10	15	60	124SL	**SPLH1750SA** Φ
1880 - 1940	50	+5/+5	45	0	+3	<15	-95/-120	10	15	60	124SL	**SPLH1880SA** Φ
1885 - 1975	50	+5/+5	35	0	+3	<20	-90/-115	10	15	60	124SL	**SPLH1885SA** Φ
1900 - 2400	1000	+5/+15	35	+5	+2	<15	-90/-110	10	15	60	124SL	**SPLH1900SB** Φ
1900 - 2400	100	+5/+15	35	+5	+2	<15	-90/-110	10	15	60	124SL	**SPLH1900SA** Φ
2000 - 2060	50	+5/+5	45	0	+3	<15	-95/-120	10	15	60	124SL	**SPLH2000SA** Φ
2050 - 2600	1500	+5/+15	45	+5	+3	<15	-87/-106	10	15	60	124SL	**SPLH2050SA** Φ
2115 - 2230	250	+5/+10.5	45	+5	+3	<20	-95/-120	10	15	60	197	**SPLH2115SA** Φ
2330 - 2540	1000	+5/+12	45	0	+2	<10	-90/-115	10	15	60	124SL	**SPLH2330SA** Φ
2420 - 2480	1000	+5/+5	45	0	+2	<10	-90/-110	10	15	60	124SL	**SPLH2400SA** Φ
5100 - 5220	300	+5/+5	45	-3	+3	<10	-80/-100	10****	15	60	197	**SPLH5100SA** ***
5650 - 5791	300	+5/+5	45	-3	+3	<10	-80/-100	10****	15	60	197	**SPLH5650SA** ***

New! HIGH FREQUENCY FRACTIONAL SYNTHESIZERS

1470 - 2070	25	+5/+18	60	9	+3	<15	-85/-110	10	15	55	197	**FSPLH1470SA**Ξ**
1710 - 1880	50	+5/+12	50	3	+3	<15	-92/-110	10	15	60	197	**FSPLH1710SA**Ξ**
1850 - 1990	50	+5/+12	50	3	+3	<15	-92/-110	10	15	60	197	**FSPLH1850SA**Ξ**
2040 - 2540	100	+5/+12	50	7	+3	<15	-85/-105	10	15	60	197	**FSPLH2040SA**Ξ**

COMMON SPECIFICATIONS

Output Impedance: 50 ohms
Reference Input Voltage: >0.5 V p-p

***Reference Input Frequency : 5 to 40 MHz**
Contact the factory for more stringent operating temperature range

Operating Temperature: -20°C to +70°C

*** - Must be a multiple of the step size** **** Reference frequency must be multiple of (16 x step size)**
***** - Programming Type -** Same programming as National Semiconductor LMX2326 chip
**** - Also applies to sub-harmonic rejection
¥ - Programming Type - Same programming as National Semiconductor LMX2320 chip
Φ - Programming Type - Same programming as National Semiconductor LMX2325 chip
Ξ - Programming Type - Same programming as National Semiconductor LMX2350 fractional chip. **

PIN-OUT TABLE

RF Out	Vcc1	Vcc2	Clock In	Latch Enable Input	Data In	F_{ref} In	Lock Detect Output	Ground	Package Style
13	12	16	1	4	5	8	9	2,3,14,15	124SL
5	16	18	11	12	9	14	7	All Others	197

For pin location and package outline drawings, see back pages.

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INTEGRATED FREQUENCY SYNTHESIZERS

HIGH FREQUENCY

192

FREQUENCY RANGE (MHz)	STEP SIZE (KHz)	DC BIAS REQUIREMENTS Vcc1 & 2 (Volts)	DC BIAS REQUIREMENTS CURRENT Max. (mA)	OUTPUT POWER dBm	OUTPUT POWER Tolerance (dB)	SETTLING TIME (mSec)	TYPICAL PHASE NOISE dBc/Hz Offset at 10 KHz/100 KHz	TYPICAL HARMONIC SUPPRESSION 2nd (dBc)	TYPICAL HARMONIC SUPPRESSION 3rd (dBc)	TYPICAL SPURIOUS REFERENCE SIDEBAND SUPPRESSION (dBc)	PACKAGE	MODEL
1512 - 1585	200	+5/+5	35	2	+2	<15	-75/-100	20	20	60	192	**JPLH1512SA** **
1652 - 1710	200	+5/+5	35	2	+2	<15	-75/-100	20	20	60	192	**JPLH1652SA** **
1705 - 1780	50	+5/+5	45	0	+3	<15	-90/-115	10	15	60	192	**JPLH1705SA** ¥
1710 - 1770	30	+5/+5	45	0	+3	<15	-90/-115	10	15	60	192	**JPLH1710SA** ¥
1760 - 1830	50	+5/+5	45	0	+3	<15	-90-115	10	15	60	192	**JPLH1760SA** ¥
1775 - 1885	625	+5/+5	40	0	+3	<15	-95/-120	10	15	60	192	**JPLH1775SA** Φ
1790 - 1850	30	+5/+5	45	0	+3	<15	-90/-115	10	15	60	192	**JPLH1790SA** ¥
1850 - 1910	50	+5/+5	45	0	+3	<15	-90/-115	10	15	60	192	**JPLH1850SA** ¥
1880 - 1960	625	+5/+5	40	0	+3	<15	-95/-120	10	15	60	192	**JPLH1880SA** Φ
2060 - 2140	50	+5/+5	45	0	+3	<15	-90/-115	10	15	60	192	**JPLH2060SA** Φ
2320 - 2400	625	+5/+5	40	0	+3	<15	-95/-120	10	15	60	192	**JPLH2320SA** Φ
2440 - 2470	1000	+5/+5	40	0	+2	<15	-90/-115	15	15	60	192	**JPLH2440SA** Φ

COMMON SPECIFICATIONS

Output Impedance: 50 ohms
Reference Input Voltage: >0.5 V p-p

***Reference Input Frequency : 5 to 40 MHz**
Contact the factory for more stringent operating temperature range

Operating Temperature: -20°C to +70°C

*** - Must be a multiple of the step size**
**** - Programming Type -** Same programming as National Semiconductor LMX2326 chip
¥ - Programming Type - Same programming as National Semiconductor LMX2320 chip
Φ **- Programming Type -** Same programming as National Semiconductor LMX2325 chip

PIN-OUT TABLE

RF Out	Vcc1	Vcc2	Clock In	Latch Enable Input	Data In	F_{ref} In	Lock Detect Output	Ground	Package Style
7	5	1	10	12	11	3	9	2,4,6,8	192

For pin location and package outline drawings, see back pages.