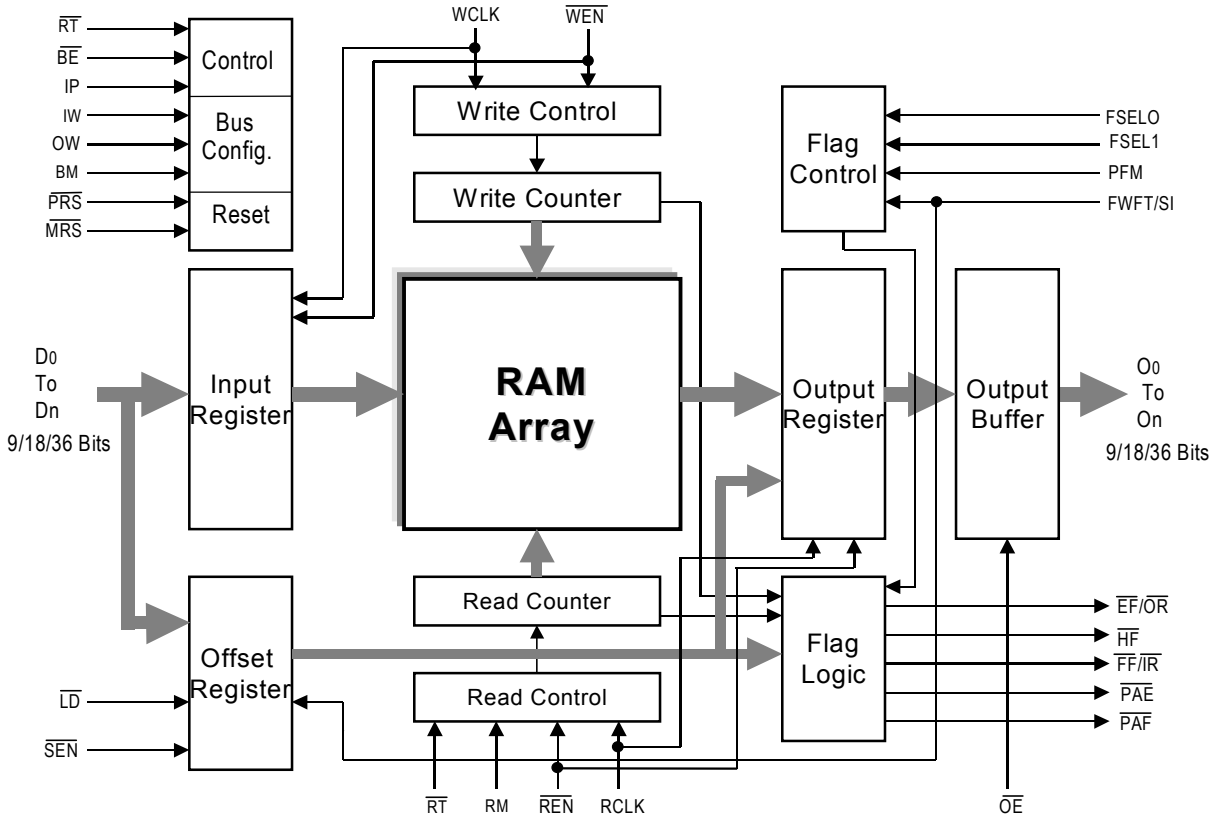
J72V3630 512 x 36 Bits J72V3640 1,024 x 36 Bits J72V3650 2,048 x 36 Bits J72V3660 4,096 x 36 Bits
J72V3670 8,192 x 36 Bits J72V3680 16,384 x 36 Bits J72V3690 32,768 x 36 Bits

VeloSync+$_{TM}$ High Performance 36 Bit Wide 3.3V Synchronous FIFO

Features:

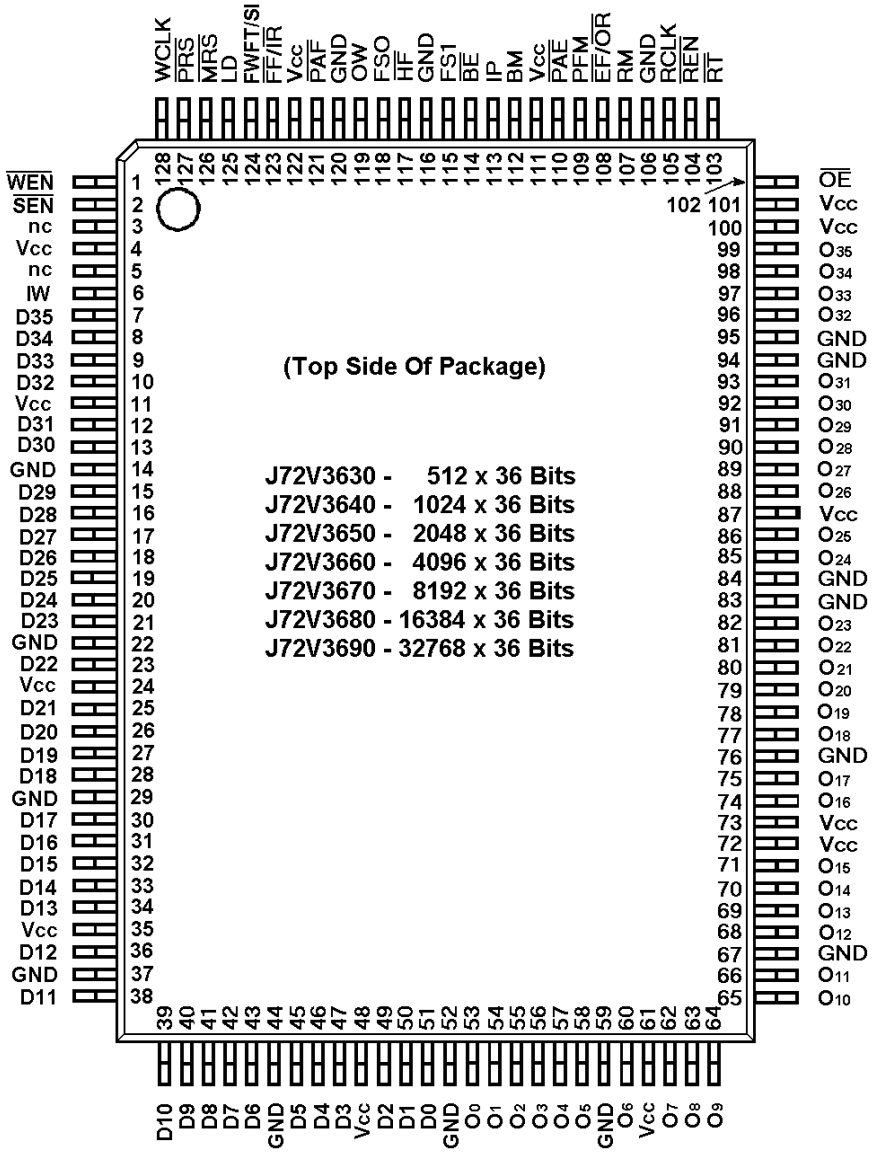
- **Very High Performance – 133 MHz Max Clock Rate**
- **Low Power Requirements**
- **5 ns Data Access Time**
- **7.5 ns Read/Write Cycle Times**
- **Separate and Independent Read / Write Clocking**
- **Bus Configuration Select Pins For x9, x18, and x36 Input and Output Widths**
- **FIFO Empty, FIFO Half Full and FIFO Full Status Flags**
- **Choice of Partial Clear or Master Clear**
- **3.3 V Operation, 5V Tolerant Device Inputs**
- **Cascade Capability to Expand Width and Depth**
- **Designed For Zero Fall-Through Timing**
- **Retransmit Feature With Zero Latency**
- **Almost Empty and Almost Full Flags Are Programmable With Default To One Of Eight Pre-selected Offsets**
- **Fixed, Low First Word Latency**
- **Programmable Endian Byte Views**
- **Programmable Flags Can Be Set Up in Parallel or Serial Fashion**
- **Programmable Flags Can Be Set Up for Asynchronous or Synchronous Operation**
- **Output Enable for 3-State Mode Control of Data Bus**
- **Offered in 128-Pin Plastic Thin Quad Flat Pack (TQFP)**
- **Commercial (0°C to +70°C) and Industrial (-40° C to +85° C.) Temperatures Available**
- **High Performance, Lower-Power Replacement For Industry Standard FIFOs (See Page 31)**



Device Description:

These very high-performance, low-power synchronous First-In/First-Out (FIFO) buffer memories are directly pin and function compatible with currently available industry standard FIFOs. They offer independently clocked read and write controls, provide maximum operational flexibility, and utilize synchronous read and write clocking for easy system design. An Input Bus Configuration of x36 may have either a x9, x18, or x36 Output Bus Configuration. An Output Bus Configuration of x36 may have either a x9, x18, or x36 Input Bus Configuration. Bus Configurations are programmed by the $\overline{IW}$, $\overline{OW}$, and BM input pins during Master Clear. These FIFOs offer high performance, while providing lower power than similar devices when utilized at comparable clock rates. They are offered in 1,024, 2048, 4096, 8,192, 16,384, 32,768, 65,536, and 131,072 x36 bit wide organizations with cascading capability in both width and depth to match a variety of data buffering requirements. These FIFOs are a cost effective solution to provide elastic data buffering for data communications, multi-processing, networking, video, and graphics applications. The data input port is controlled by WCLK, a free-running clock, and $\overline{WEN}$, a Write Enable pin. Each rising edge of the clock writes data into the FIFO when the write enable pin is active. RCLK and the Read Enable pin $\overline{REN}$, control reading the FIFO in the same manner. Both the Read Clock and the Write Clock can be tied together for single clock operation or each clock can be utilized asynchronously for dual, separate clock operation. $\overline{OE}$ provides control of the read output 3-state buffer for use in direct bus applications.

For maximum flexibility and ease of use, these FIFOs offer two programmable flags to indicate Almost Full and Almost Empty as well as the standard Full ($\overline{FF}$), Half Full (HF), and Empty ($\overline{EF}$) flags. The programmable flag offsets are set to default values during Master Clear ($\overline{MRS}$) by one of the eight states of the LD, FSEL0, and FSEL1 input pins. Parallel and Serial loading of these offsets to any value is also available. Parallel loading occurs via the Data Inputs on the rising edge of the Write Clock (WCLK) when Write Enable (WEN) and Load ($\overline{LD}$) inputs are low. Serial loading of these offsets via the Serial Input (SI of the FWFT/SI pin) occurs on each rising edge of the Write Clock (WCLK) when the Serial Load (SL) and Load ($\overline{LD}$) inputs are low. Master Clear ($\overline{MRS}$) and Partial Clear ($\overline{PRS}$) are asynchronous low signals that reset the output register, the output register, the write pointer and the read pointer to zero. During Master Clear ($\overline{MRS}$), the state of the FWFT/SI input pin selects either the Normal Mode or the Fall Through Mode of FIFO operation. If this input pin is high during Master Clear, the Fall Through Mode is selected, and the Input Ready ($\overline{IR}$) and Output Ready ($\overline{OR}$) functions are active. After 3 transitions of the Read Clock (RCLK), the first word input to an empty FIFO is available on the data outputs regardless of the state of Read Enable ($\overline{REN}$) input pin. Additional words input to the FIFO do require a low state of REN in order to be read. Chaining the Data Outputs of one FIFO to the Data Inputs of a second FIFO accomplishes depth expansion when the Fall Through Mode (FWFT) is selected without requiring any other logic. A low on the FWFT/SI pin during Master Clear ($\overline{MRS}$) selects Normal Mode of FIFO operation, and the Full Flag ($\overline{FF}$) an Empty Flag ($\overline{EF}$) functions are active. The first word input to an empty FIFO is available at the data outputs on the first enabled ($\overline{REN}$) rising edge of the Read Clock (RCLK). The functions of the Programmable Almost Full, Almost Empty and Half Full Flags are not affected by the mode selected.



The output format of x9, x18, and x36 data input widths is also selected during Master Clear by the state of the Big Endian/Little Endian (BE) input pin. If high, Little Endian is selected and if low, Big Endian is selected. Refer to Table 6 for Endian Byte programming.

Maximum Ratings:

Symbol	Rating	Unit	Range
I_{out}	Output Current (DC)	mA	-50 to +50
V_{input}	Terminal Voltage vs. GND	V	-0.5 to +4.5
T_{store}	Storage Temperature	°C	-55 to +125

Note:
Exceeding maximum stress ratings may possibly cause permanent damage to the device. The device is designed to operate only within the conditions specified for normal operation, and should never be operated beyond those normal operating limits. Reliability may be compromised if the device is exposed to absolute maximum rating conditions for extended periods of time.

Recommended Operating Conditions:

Symbol	Parameter	Unit	Min.	Max.
Vil	Input Low Voltage	V	--	0.8
Vih	Input High Voltage	V	2.0	5.5
To	Operating Temperature	°C	0	+70
Vcc	Supply Voltage	V	3.15	3.45
GND	Ground Reference Voltage	V	0	0

DC Electrical Characteristics:

Commercial Temperature Range (0°C to + 70°C) with Vcc of +3.15V to +3.45V. RCLK and WCLK may either be static or running.

Parameter	Symbol	Unit	Min	Max
Output Leakage Current (All Outputs)	I_{out}	µA	-10	10
Input Leakage Current (All Inputs)	I_{in} (1)	µA	-1	1
Power Supply Current (Active with x9 Input and Output Widths)	I_{cc} (2,3)	mA	-	30
Power Supply Current (Active with x18 Input and Output Widths)	I_{cc} (2,3)	mA	-	35
Stand-By Current	I_{ccx}	mA	-	15
Voh (Output Voltage High) Ioh=-2mA	V_{oh}	V	2.4	-
Vol (Output Voltage Low) Iol=8mA	V_{ol}	V	-	0.4

NOTES:

1. Measured with a voltage input range of +0.4V to Vcc.
2. Data inputs are switched at 10 MHz with WCLK and RCLK running at 20 MHz.
3. Outputs are disabled during test.
4. All Inputs = GND + 0.2V or Vcc – 0.2V . WCLK and RCLK, are running at 20 MHz.

Input/Output Capacitance: (Clock Frequency = 2.0 MHz, Ambient Temperature = +25°C)

Symbol	Parameter	Unit	Conditions	Max.
C_i[2]	Input Capacitance	pF	Vin = 0V	10
C_o[1,2]	Output Capacitance	pF	Vout = 0V	10

NOTES:

1. With output set to 3-state high impedance ($\overline{OE} \geq Vih$).
2. Not currently tested specifications (characterized only).

AC Test Conditions:

Input Levels	GND to +3.0V
Input Rise/Fall Time	1 ns
Input Reference Levels	1.5 V
Output Reference Levels	1.5 V
Output Load	See figure 2.

Typical Derating For Total Capacitive Load:

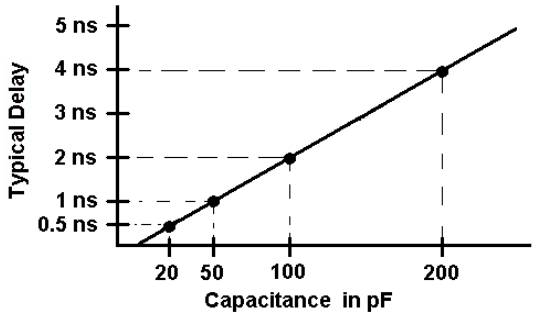
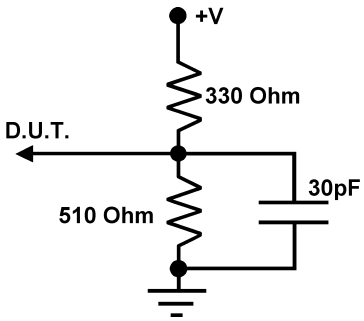


Figure 1. Capacitive Loading

Equivalent Test Load Circuits

Up To 100 MHz



133 MHz

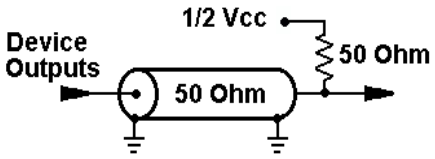


Figure 2. Test Load Circuits

Pin Functions and Description:

Pin	Pin #	Symbol	I/O	Description
Power	4, 11, 24, 35, 48, 61, 72, 87, 100, 101, 111, 122	Vcc	N/A	12 Positive power supply pins (+3.3 Volts)
Ground	14,22, 29, 37,44, 52, 59, 67, 76, 83, 84, 94 ,95, 106, 116, 120	GND	N/A	16 Ground pins (Zero Volts)
Master Clear	126	$\overline{MRS}$	Input	Master Clear is an asynchronous low signal, which resets the output register, the write pointer, and the read pointer to zeros. Most programmable mode functions and offsets are also configured during Master Clear.
Partial Clear	127	$\overline{PRS}$	Input	Partial Clear is an asynchronous low signal, which resets the output register, the write pointer, and the read pointer to zeros.
Interspersed Parity Mode(1)	113	IP(1)	Input	Interspersed Parity will be programmed if this pin is high during Master Clear. Non-Interspersed Parity will be programmed if this pin is low during Master Clear.
Retransmit Timing Mode(1)	107	RM(1)	Input	Normal Latency Timing will be programmed if this pin is high during Master Clear. Zero Latency Timing will be programmed if this pin is low during Master Clear.
Input Width(1)	6	IW(1)	Input	Input Width is programmed during Master Clear. Please see Table 1 for usage.
Bus Matching(1)	6	BM1)	Input	Bus Matching is programmed during Master Clear. Please see Table 6 for usage.
Input Data	7-10, 12, 13, 15-21, 23, 25-28, 30-36, 38-43, 45-47, & 49-51	D35 - D0	Input	Input Data (36 bits wide) When set to less than 36 Bit Input, the unused pins are in a " don't care" state. Note: It is recommended that any unused input pins be tied to ground or held at Vil (Input Low Voltage).
Write Enable	1	$\overline{WEN}$	Input	When $\overline{WEN}$ is low, the Write Clock (WCLK) is Enabled
Write Clock	128	WCLK	Input	Low to high transitions of WCLK, when enabled by Write Enable ($\overline{WEN}$), writes data into the FIFO, and if parallel programming has been selected, into the programmable registers. Low to high transitions of WCLK, when enabled by Serial Loading ($\overline{SEN}$), and serial programming of the Programmable Offset Registers has been selected, writes one bit of data into the registers.
Normal Mode ,Fall Through Mode, Serial Input	124	FWFT/SI	Input	If this input pin is low during Master Clear, the Normal Mode of FIFO operation is selected. If this input pin is high during Master Clear, the Fall Through Mode of FIFO operation is selected. This pin is then used for serial loading of the programmable offsets, if enabled by Serial Loading ($\overline{SEN}$).
Serial Load	2	$\overline{SEN}$	Input	When this input pin is low, serial loading of the programmable offsets is enabled.
Output Width(1)	119	OW(1)	Input	This pin along with IW and BM programs the Output Width during Master Clear.
Big Endian/ Little Endian(1)	114	$\overline{BE}$	Input	Little Endian output read will be programmed if this pin is high during Master Clear. Big Endian output read will be programmed if this pin is low during Master Clear
Output Data	31-32, 34-35, 37-38, 40-43, 45, 47, 49-50, 52-53, 56-57	$O_{35} - O_0$	Output	Output Data -36 bits wide (Various output widths can be programmed during Master Reset.) NOTE: Unused outputs should be left open.
Read Enable	104	$\overline{REN}$	Input	When $\overline{REN}$ is low, the Read Clock (RCLK) is Enabled
Read Clock	105	RCLK	Input	When $\overline{REN}$ is low, the rising edge of this clock causes data to be read from the FIFO and Programmable Offset Registers.
Output Enable	102	$\overline{OE}$	Input	The data output bus is active whenever OE is Low. The output data bus is in a high-impedance state whenever $\overline{OE}$ is high.
Flag Select O(1)	118	FS0(1)	Input	Bit 0 utilized to program the flag offset values during Master Clear.
Flag Select 1(1)	115	FS1(1)	Input	Bit 1 utilized to program the flag offset values during Master Clear.
Load	125	$\overline{LD}$	Input	Bit 2 utilized to program the flag offset values during Master Clear. After Master Clear this pin, when in the low state, enables serial reading and writing of the offset numbers.

Pin Functions and Description (Continued):

Pin	Pin #	Symbol	I/O	Description
Retransmit	103	$\overline{RT}$	Input	When this signal is low during the rising edge of an enabled read clock (RCLK) the empty flag ($\overline{EF}$)is set to low (Normal Mode) or output ready ($\overline{OR}$) is set to high in FWFT (Fall Through Mode) and sets the Read Pointer to zero enabling a Reread of data from the first location in the FIFO.
Empty Flag Output Ready	108	$\overline{EF}/\overline{OR}$	Output	When this pin goes low in the Normal Mode, there is no data in the FIFO ($\overline{EF}$ = Empty). When this pin goes low in the Fall Through Mode, there is data available from the Data Outputs ($\overline{OR}$ = Data Available).
Programmable Flag Mode(1)	109	PFM(1)	Input	Synchronous flag timing will occur if this pin is high during Master Clear. Asynchronous flag timing will occur if this pin is low during Master Clear.
Programmable Almost-Empty Flag	110	$\overline{PAE}$	Output	This signal indicates the almost empty state of the FIFO based upon the offset number previously loaded into the FIFO. When $\overline{PAE}$ is low, it indicates that the FIFO is Almost-Empty with fewer words than the offset number. When $\overline{PAE}$ is high, it indicates that the FIFO contains a number of words equal to, or greater than the offset number.
Half-Full Flag	117	$\overline{HF}$	Output	When this signal goes low, it indicates that the FIFO is at least Half Full.
Programmable Almost-Full Flag	121	$\overline{PAF}$	Output	This signal indicates the almost full state of the FIFO based upon the offset number previously loaded into the FIFO. When $\overline{PAF}$ is low, it indicates that the FIFO is Almost-Full with empty word locations equal to or less than the offset number. When $\overline{PAF}$ is high, it indicates that the FIFO contains more empty word locations than the offset number.
Full Flag Input Ready	123	$\overline{FF}/\overline{IR}$	Output	When this pin goes low in the Normal Mode, the FIFO is full ($\overline{FF}$ = Full). When this pin goes low in the Fall Through Mode, the FIFO is available to receive Data. ($\overline{IR}$ = Input Ready).
Do Not Connect	3 & 5	NC	N/A	Unused - Do not connect

NOTES:

1. These Input Signals are to remain stable during and after Master Clear

Input/Output Bus Width/ Bus Matching Programming:

Table 1 illustrates the selectable Input and Output Bus Configurations/Bus Matching versus the **States of BM, IW and OW,** indicating the polarity of the pins during Master Clear.

BM	IW	OW	Output Data Width	Input Data Width
H	**H**	**H**	**x36**	**x9**
H	**H**	**L**	**x36**	**x18**
H	**L**	**H**	**x9**	**x36**
H	**L**	**L**	**x18**	**x36**
L	**L**	**L**	**x36**	**x36**

Table 1. Input/Output Width Programming

AC Electrical Characteristics: (VCC = +3.15V to +3.45V, Temperature = 0°C to + 70°C)

Symbol	Parameter	J72VxxxxL7.5		J72VxxxxL10		J72VxxxxL15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
fcy	Clock Cycle Frequency	--	133	--	100	--	66	MHz
tacc	Data Access Time	--	5	2	6.5	2	10	ns
tclk	Read/Write Clock Cycle Time	7.5	--	10	--	15	--	ns
tclkl	Read/Write Clock Low Time	3.5	--	4.5	--	6	--	ns
tclkh	Read/Write Clock High Time	3.5	--	4.5	--	6	--	ns
tis	Data Set-up Time for Input	2.5	--	3.5	--	4	--	ns
tih	Data Hold Time for Input	0.5	--	0.5	--	1	--	ns
tes	Set-up Time for Enable	2.5	--	3.5	--	4	--	ns
teh	Hold Time for Enable	0.5	--	0.5	--	1	--	ns
tls	Set-up Time for Load	3.5	--	3.5	--	4	--	ns
tlh	Hold Time for Load	0.5	--	0.5	--	1	--	ns
trpw	Pulse Width of RST(1)	10	--	10	--	15	--	ns
trsts	Set-up Time for RST	15	--	15	--	15	--	ns
trstr	Recovery Time from RST	10	--	10	--	15	--	ns
trfo	Time from Reset to Flag and Outputs	--	15	--	15	--	15	ns
trrs	Set-up Time for Reread	3.5	--	3.5	--	4	--	ns
toel	Output Enable to Output in Low-Z(2)	0	--	0	--	0	--	ns
tov	Output Enable to Output Valid	2	6	2	6	3	8	ns
toeh	Output Enable to Output High-Z(2)	2	6	2	6	3	8	ns
twf	Write Clock to Full Flag/Input Ready delay	--	5	--	6.5	--	10	ns
tfe	Read Clock to Empty Flag/Output Ready delay	--	5	--	6.5	--	10	ns
taffs	Write Clock to Synchronous Almost-Full Flag delay	--	12.5	--	16	--	20	ns
taffa	Write Clock to Asynchronous Amost-Full Flag delay	--	5	--	6.5	--	10	ns
taefs	Read Clock to Synchronous Almost Empty Flag delay	--	4.0	--	4.4	--	6.5	ns
taefa	Read Clock to Asynchronous Almost Empty Flag delay	--	12.5	--	16	--	20	ns
thff	Clock to Half Full Flag delay	--	12.5	--	16	--	20	ns
t_{SKEW1}	Read Clock & Write Clock skew time for Empty Flag & Full Flag	5	--	7		9	--	ns
t_{SKEW2}	Read Clock & Write Clock skew time for Almost-Empty Flag & Almost – Full Flag	7	--	10	--	14	--	ns

NOTES:
1. Minimum pulse widths must not be violated.
2. These values are not specifically tested, but are guaranteed by design.

Offset Registers Default and Programmable Bit Assignments

The following charts indicate the bit assignments for these FIFO's. Each FIFO utilizes a different number of bits for programming the offsets depending on the FIFO size and x9, x18 and x36 input and output bus width selections. Note that register bit 8 (the 9th bit) of the LSB register is not used for either Empty Offset, or Full Offset for interspersed parity. The first chart for each device depicts the **Default Value** loaded into the Empty and Full Offset Registers during **Master Clear**. The charts for each device show the bit assignments for the **Programmable** (Parallel and Serial), writing and reading of the Empty and Full Offset Registers for each input and output bus configuration. The write and read cycles reference parallel mode.

J72V3630, J72V3640, J72V3650, J72V3660, J72v3670, J72V3680, J72V3690
9-Bit Organization

Default Values Programmed Into Empty and Full Offset Registers	3	7	15	31	63	127	255	511
FSEL0	H	H	L	L	H	L	H	L
FSEL1	H	L	H	L	H	L	L	H
LD	H	H	H	H	L	L	L	L

Input x9 Output x9	**Empty Offset (LSB) Write/Read Cycle 1**									**Empty Offset (MSB) Write/Read Cycle 2[2]**								
Register Bits	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Offset Bits[1]	**x**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**x**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**

Input x9 Output x9	Dummy Write/Read Cycle Write/Read Cycle 3									**Full Offset (LSB) Write/Read Cycle 4**								
Register Bits	8	7	6	5	4	3	2	1	0	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Offset Bits[1]	x	x	x	x	x	x	x	x	x	**x**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**

Input x9 Output x9	**Full Offset (MSB) Write/Read Cycle 5[2]**									Dummy Write/Read Cycle Write/Read Cycle 6								
Register Bits	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	8	7	6	5	4	3	2	1	0
Offset Bits[1]	**x**	**x**	**x**	**Y_5**	**Y_4**	**Y_3**	**Y_2**	**Y_1**	**8**	x	x	x	x	x	x	x	x	x

Note: 1. The "Y" bits listed in the table (above) are not required for the J72V3630 device. For the J72V3640, Y_1 becomes bit value 9 (10 bits total) for either reading from or writing into the offset registers. For the J72V3650, Both Y_1 is used for bit value 9 and Y_2 is used for bit value 10 (11 bits total) for either reading from or writing into the offset registers. The same convention of using additional Y bits occurs for each larger device. Non required Y bits are not used and are "do not care".

2. Write cycles 2 and 5, (above) utilize the same 8 inputs bits to load or read the high order addresses.

Default Values Programmed Into Empty and Full Offset Registers	3	7	15	31	63	127	255	511
FSEL0	H	H	L	L	H	L	H	L
FSEL1	H	L	H	L	H	L	L	H
LD	H	H	H	H	L	L	L	L

Input x18 Output x18	Empty Offset (Non-Interspersed Parity) Write/Read Cycle 1																	
Register Bits	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Offset Bits[2]	x	x	x	x	x	x	Y_2	Y_1	9	8	7	6	5	4	3	2	1	0

Input x18 Output x18	Empty Offset (Non-Interspersed Parity) Write/Read Cycle 2[1]																	
Register Bits	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Offset Bits	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Input x18 Output x18	Full Offset (Non-Interspersed Parity) Write/Read Cycle 3																	
Register Bits	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Offset Bits[2]	x	x	x	x	x	x	Y_2	Y_1	9	8	7	6	5	4	3	2	1	0

Input x18 Output x18	Full Offset (Non-Interspersed Parity) Write/Read Cycle 4[1]																	
Register Bits	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Offset Bits	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Notes: 1. Although these cycles are required, no data is written or read from the registers.

2. The “Y” bits listed in the table (above) are not required for the J72V3630 device. For the J72V3640, Y_1 becomes bit value 9 (10 bits total) for either reading from or writing into the offset registers. For the J72V3650, Both Y_1 is used for bit value 9 and Y_2 is used for bit value 10 (11 bits total) for either reading from or writing into the offset registers.

J72V3630, J72V3640, J72V3650 - 18 Bit Organization
Interspersed Parity

Default Values Programmed Into Empty and Full Offset Registers	3	7	15	31	63	127	255	511
FSEL0	H	H	L	L	H	L	H	L
FSEL1	H	L	H	L	H	L	L	H
LD	H	H	H	H	L	L	L	L

Input x18 Output x18	**Empty Offset (Interspersed Parity) Write/Read Cycle 1**																	
Register Bits	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Offset Bits[2]	x	x	x	x	x	Y_2	Y_1	9	8	x	7	6	5	4	3	2	1	0

Input x18 Output x18	Empty Offset (Interspersed Parity) Write/Read Cycle 2[1]																	
Register Bits	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Offset Bits	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Input x18 Output x18	**Empty Offset (Interspersed Parity) Write/Read Cycle 3**																	
Register Bits	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Offset Bits	x	x	x	x	x	Y_2	Y_1	9	8	x	7	6	5	4	3	2	1	0

Input x18 Output x18	Empty Offset (Interspersed Parity) Write/Read Cycle 4[1]																	
Register Bits	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Offset Bits	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Notes: 1. Although these cycles are required, no data is written or read from the registers.

2. The "Y" bits listed in the table (above) are not required for the J72V3630 device. For the J72V3640, Y_1 becomes bit value 9 (10 bits total) for either reading from or writing into the offset registers. For the J72V3650, Both Y_1 is used for bit value 9 and Y_2 is used for bit value 10 (11 bits total) for either reading from or writing into the offset registers.

J72V3660, J72V3670, J72V3680, J72V3690 - 18 Bit Organization
Non –Interspersed Parity

Default Values Programmed Into Empty and Full Offset Registers	7	15	31	63	127	255	511	1023
FSEL0	H	H	L	L	H	L	H	L
FSEL1	H	L	H	L	H	L	L	H
LD	H	H	H	H	L	L	L	L

Input x18 Output x18	**Empty Offset (Non-Interspersed Parity) Write/Read Cycle 1**																	
Register Bits	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Offset Bits[2]	x	x	x	Z_3	Z_2	Z_1	11	10	9	8	7	6	5	4	3	2	1	0

Input x18 Output x18	Empty Offset (Non-Interspersed Parity) Write/Read Cycle 2[1]																	
Register Bits	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Offset Bits[2]	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Input x18 Output x18	**Empty Offset (Non-Interspersed Parity) Write/Read Cycle 3**																	
Register Bits	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Offset Bits[2]	x	x	x	Z_3	Z_2	Z_1	11	10	9	8	7	6	5	4	3	2	1	0

Input x18 Output x18	Empty Offset (Non-Interspersed Parity) Write/Read Cycle 4[1]																	
Register Bits	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Offset Bits[2]	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Notes: 1. Although these cycles are required, no data is written or read from the registers.

2. The "Z" bits listed in the table (above) are not required for the J72V3660 device. For the J72V3670, Z_1 becomes bit value 12 (13 bits total) for either reading from or writing into the offset registers. For the J72V3680, Both Z_1 is used for bit value 12 and Z_2 is used for bit value 13 (14 bits total) for either reading from or writing into the offset registers. For the J72V3690, all three Z bits are used for bit value 12, 13 and 14 (15 bits total) for reading from or writing into the offset registers.

J72V3660, J72V3670, J72V3680, J72V3690 - 18 Bit Organization
Interspersed Parity

Default Values Programmed Into Empty and Full Offset Registers	7	15	31	63	127	255	511	1,023
FSEL0	H	H	L	H	L	H	L	L
FSEL1	H	L	H	H	L	L	H	L
LD	H	H	H	L	L	L	L	H

Input x18 Output x18	Empty Offset (Non-Interspersed Parity) Write/Read Cycle 1																	
Register Bits	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Offset Bits[2]	x	x	Z_3	Z_2	Z_1	11	10	9	x	8	7	6	5	4	3	2	1	0

Input x18 Output x18	Empty Offset (Non-Interspersed Parity) Write/Read Cycle 2[1]																	
Register Bits	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Offset Bits	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Input x18 Output x18	Full Offset (Non-Interspersed Parity) Write/Read Cycle 3																	
Register Bits	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Offset Bits[2]	x	x	Z_3	Z_2	Z_1	11	10	9	x	8	7	6	5	4	3	2	1	0

Input x18 Output x18	Full Offset (Non-Interspersed Parity) Write/Read Cycle 4[1]																	
Register Bits	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Offset Bits	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Notes: 1. Although these cycles are required, no data is written or read from the registers.

2. The "Z" bits listed in the table (above) are not required for the J72V3660 device. For the J72V3670, Z_1 becomes bit value 12 (13 bits total) for either reading from or writing into the offset registers. For the J72V3680, Both Z_1 is used for bit value 12 and Z_2 is used for bit value 13 (14 bits total) for either reading from or writing into the offset registers. For the J72V3690, all three Z bits are used for bit value 12, 13 and 14 (15 bits total) for reading from or writing into the offset registers.

J72V3630, J72V3640, J72V3650 - 36 Bit Organization
Non –Interspersed Parity

Default Values Programmed Into Empty and Full Offset Registers	3	7	15	31	63	127	255	511
FSEL0	H	H	L	L	H	L	H	L
FSEL1	H	L	H	L	H	L	L	H
LD	H	H	H	H	L	L	L	L

Input x36 Output x36	Empty Offset (Non-Interspersed Parity) Write/Read Cycle 1																	
Register Bits	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Offset Bits[2]	x	x	x	x	x	x	Y_2	Y_1	9	8	7	6	5	4	3	2	1	0

Input x36 Output x36	Full Offset (Non-Interspersed Parity) Write/Read Cycle 2																	
Register Bits	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Offset Bits[2]	x	x	x	x	x	x	Y_2	Y_1	9	8	7	6	5	4	3	2	1	0

Notes: 1. This cycle addresses the Full Offset register. No extra cycles are required.

2. The "Y" bits listed in the table (above) are not required for the J72V3630 device. For the J72V3640, Y_1 becomes bit value 9 (10 bits total) for either reading from or writing into the offset registers. For the J72V3650, Both Y_1 is used for bit value 9 and Y_2 is used for bit value 10 (11 bits total) for either reading from or writing into the offset registers.

J72V3630, J72V3640, J72V3650 - 36 Bit Organization
Interspersed Parity

Default Values Programmed Into Empty and Full Offset Registers	3	7	15	31	63	127	255	511
FSEL0	H	H	L	L	H	L	H	L
FSEL1	H	L	H	L	H	L	L	H
LD	H	H	H	H	L	L	L	L

Input x36 Output x36	Empty Offset (Interspersed Parity) Write/Read Cycle 1																	
Register Bits	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Offset Bits[2]	x	x	x	x	x	Y_2	Y_1	9	x	8	7	6	5	4	3	2	1	0

Input x36 Output x36	Full Offset (Interspersed Parity) Write/Read Cycle 2																	
Register Bits	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Offset Bits[2]	x	x	x	x	x	Y_2	Y_1	9	x	8	7	6	5	4	3	2	1	0

Notes: 1. This cycle addresses the Full Offset register contents. No extra cycles are required.

2. The "Y" bits listed in the table (above) are not required for the J72V3630 device. For the J72V3640, Y_1 becomes bit value 9 (10 bits total) for either reading from or writing into the offset registers. For the J72V3650, Both Y_1 is used for bit value 9 and Y_2 is used for bit value 10 (11 bits total) for either reading from or writing into the offset registers.

Status Flags: Normal Mode

The following table illustrates the state of the status flags for varying amounts of data in the FIFO. Please see the programmable **Offset Registers Default and Programmable Bit Assignments** beginning on page 8 of this data sheet.

J72V3630	*J72V3640*	*J72V3650*	*J72V3660*	*J72V3670*	*J72V3680*	*J72V3690*	EF	HF	FF	PAE	PAF
512	1024	2048	4096	8192	16384	32768	H	L	L	H	L
(512-m) to 511	(1024-m) to 1023	(2048-m) to 2047	(4096-m) to 4095	(8192-m) to 8191	(16384-m) to 16383	(32768-m) to 32767	H	L	H	H	L
257 to (512-(m+1))	513 to (1024-(m+1))	1025 to (2048-(m+1))	2049 to (4096-(m+1))	4097 to (8192-(m+1))	8193 to (16384-(m+1))	65,537 to (131,072-(m+1))	H	L	H	H	H
(n+1) to 256	(n+1) to 512	(n+1) to 1024	(n+1) to 2048	(n+1) to 4096	(n+1) to 8192	(n+1) to 16384	H	H	H	H	H
1 to n	1 to n	1 to n	1 to n	1 to n	1 to n	1 to n	H	H	H	L	H
0	0	0	0	0	0	0	L	H	H	L	H

Table 2. Status Flags- Normal Mode

Status Flags: Fall Through Mode (FWFT)

The following table illustrates the state of the status flags for varying amounts of data in the FIFO.

J72V3630	*J72V3640*	*J72V3650*	*J72V3660*	*J72V3670*	*J72V3680*	*J72V3690*	OR	HF	IR	PAE	PAF
513	1025	2049	4097	8193	16385	32769	L	L	H	H	L
(513-m) to 512	(1025-m) to 1024	(2049-m) to 2048	(4097-m) to 4096	(8193-m) to 8192	(16385-m) to 16384	(32769-m) to 32768	L	L	L	H	L
258 to (513-(m+1))	514 to (1025-(m+1))	1026 to (2049-(m+1))	2050 to (4097-(m+1))	4098 to (8193-(m+1))	8194 to (16385-(m+1))	16386 to (32769-(m+1))	L	L	L	H	H
(n+2) to 257	(n+2) to 513	(n+2) to 1025	(n+2) to 2049	(n+2) to 4097	(n+2) to 8193	(n+2) to 16385	L	H	L	H	H
1 to (n+1)	1 to (n+1)	1 to (n+1)	1 to (n+1)	1 to (n+1)	1 to (n+1)	1 to (n+1)	L	H	L	L	H
0	0	0	0	0	0	0	H	H	L	L	H

Table 3. Status Flags – FWFT Mode

Status Flag Offset Programming [1]:

LD	REN	SEN	WEN	WCLK	RCLK	*Selection*
0	1	1	0	Rising Edge	x	Parallel Write To Registers [2]
0	0	1	1	x	Rising Edge	Parallel Read From Registers [2]
0	1	0	1	Rising Edge	x	Serial Shift To Registers [3]
x	1	1	1	x	x	No Operation
1	x	x	0	Rising Edge	x	Write Memory
1	0	x	x	x	Rising Edge	Read Memory
1	1	x	1	x	x	No Operation

Notes: 1. Status Flags can only be programmed during Master Reset.

2. Writing and reading to registers occur in the following order:

   A. Empty offset (LSB)
   B. Empty Offset (MSB)
   C. Full Offset (LSB)
   D. Full Offset (MSB)

3. Each rising WCLK edge clocks in one bit starting with the LSB. The number of bits shifted for each device are as follows:

   For the J72V3630 - 18 Bits
   For the J72V3640 - 20 Bits
   For the J72V3650 - 22 Bits
   For the J72V3660 - 24 bits
   For the J72V3670 - 26 bits
   For the J72V3680 - 28 bits
   For the J72V3690 - 30 bits

Table 4. Status Flag Offset Programming

Parallel Programming Sequence For Setting PAE and PAF Flags:

If the J72V3630 series FIFOs are selected to be programmed in parallel mode as outlined in the programming tables starting on page 8, with the PAE and PAF values loaded in with combinations of WEN, LD and WCLK. Various values for each flag are programmed into the device via the Data Input pins, and clocked in with WCLK.

Parallel PAF and PAE value setup is accomplished as follows:

Once the device has been set to receive parallel input during Master Clear ($\overline{MRS}$), the device will accept parallel loaded offset values. To set the Programmable Almost Empty Flag (PAE) and the programmable Almost Full Flag (PAF), LD and WEN are held low and REN and SEN are held High. Then, the data present on the Data Input Pins is written into the Empty Offset Register on the first low to high transition of WCLK. The values desired for each of the many various combinations of values for the multiple organizations of input and output bus widths are detailed in the programming tables, and as shown, various quantities of loads and/or reads are utilized based upon the bus widths selected. The registers are loaded in the order outlined in **Table 4**, **Status Flag Offset Programming** and it's respective notes.

Serial Programming Sequence For Setting PAE and PAF Flags:

If the J72V3630 series FIFOs have been selected for programming in serial mode, then the $\overline{PAE}$ and $\overline{PAF}$ values are loaded through the single bit SI input pin. Combinations of SEN, LD and WCLK are used to accomplish the loading of the bit values.

Serial $\overline{PAF}$ and $\overline{PAE}$ value setup is accomplished as follows:

Once the device has been set to receive serial input during Master Clear (MRS), the device will accept serially loaded offset values input via the SI pin. To set the Programmable Almost Empty Flag (PAE) and the programmable Almost Full Flag (PAF), LD and SEN are held low and REN and WEN are held High. Various values for each flag are loaded in one bit at a time with each rising edge of the WCLK starting with the LSB of the Empty Offset Register and ending with the MSB of the Full Offset register. The values desired for each of the many various combinations of values for the multiple organizations of input and output bus widths are shown in detail under the programming tables starting on page 8. The registers are loaded in the manner outlined in **Table 4**, **Status Flag Offset Programming** and it's respective notes.

Retransmit (RT) Operation:

The J72V3630 series FIFOs allow re-accessing of data already read from the device in two separate modes. The first mode is "Zero Latency" and the second is "Normal Latency". Each type of Retransmit requires a setup procedure consisting of two distinctly different events. First, the Read Pointer must be set to the first location in memory, the actual "Retransmit" starts at the beginning of memory.

Retransmit setup is initialized by holding the $\overline{RT}$ signal low during the rising edge of RCLK. Then for Normal Latency, prior to returning RCLK to its low state WEN and REN must be held high. If being operated with "zero latency, REN is not required to be in the high state prior to taking RT low. For Retransmit to properly occur, at least 2 words but no more than "Y-2" words should have been written to the FIFO and have also been read from the FIFO between either a Master Clear or Partial Clear and the setup of Retransmit. The value of "Y" for various FIFOs and their bus organizations are listed in the table below.

Device Type	Input / Output Bus Widths[1]	Mode	Value of "Y"
J72V3630	Any	Standard	512
J72V3630	Any	FWFT	513
J72V3640	Any	Standard	1024
J72V3640	Any	FWFT	1025
J72V3650	Any	Standard	2048
J72V3650	Any	FWFT	2049
J72V3660	Any	Standard	4096
J72V3660	Any	FWFT	4097
J72V3670	Any	Standard	8192
J72V3670	Any	FWFT	8193
J72V3680	Any	Standard	16384
J72V3680	Any	FWFT	16385
J72V3690	Any	Standard	32768
J72V3690	Any	FWFT	32769

Note: 1. The Memory depth supported by this function is equivalent to the depth of the RAM for each device type.

Table 5. FIFO Word Quantities For Retransmit

If the **Standard Mode** has been selected, the FIFO indicates the start of Reread by taking $\overline{EF}$ low. The change can only be observed if $\overline{EF}$ was in the high state before setup. During a Reread, the Internal Read Pointer initialized at the first location of the RAM. The $\overline{EF}$ signal returns to a high state when the retransmit setup has been completed, and the read operations can begin starting at the first location in the RAM. Every word to be read requires a low on $\overline{REN}$ and then a rising edge of RCLK. Please see **Figure 19, Retransmit Timing –Standard Mode** for timing details.

If the **FWFT Mode** has been selected, the FIFO marks the beginning of setup by taking OR to its high state. At this point, the Internal read pointer is initialized at the first location of the RAM. The OR signal returns to a low state when the retransmit setup has been completed, and without the necessity of REN being low the contents of the first location in the RAM are present on the device outputs. Reading of the subsequent words in the RAM requires a low on REN during the rising edge of a RCLCK. Please see **Figure 17, Retransmit Timing- FWFT Mode** for timing details.

The $\overline{PAF}$, $\overline{PAE}$ and $\overline{HF}$ Flags update with on the rising edge of RCLK that $\overline{RT}$ was setup on in either Standard or FWFT mode. $\overline{PAE}$ is fully synchronized to RCLK and will be updated on the second rising edge of RCLK after $\overline{RT}$ is setup. $\overline{HF}$ is an asynchronous and will be updated by the RCLK that sets up $\overline{RT}$. $\overline{PAF}$ is synchronized to WCLK and will update on the second rising edge of WCLK occurring tskew after the rising edge of the RCLK that $\overline{RT}$ was setup with. $\overline{RT}$ is synchronized to RCLK.

The Retransmit function can either operate in **"Zero Latency"** or **"Normal Latency"**. The term "Zero Latency indicates that the first word to be read from the RAM is placed into the device Output Register by the RCLK rising edge that initiated Reread. "Normal Latency" indicates that the device operates in a fully synchronous mode requiring an additional RCLK to move the first word to the device output register for reading. Please see **Figure 18, Zero Latency Retransmit timing-FWFT Mode**, and **Figure 20, Zero Latency Retransmit Timing- Normal Mode** for timing details.

Bus matching:

The following table outlines the control signal values for Big Endian ($\overline{BE}$), Bus Matching (BM) Input Width (IW) and Output width (OW) and the resulting byte order on the output ports for data read from the device. Bus matching is not offered for x36 to x36 operation.

IW	OW	BE	BM	Endian Programming	Data On O_{35} to O_{27} Outputs [1]	Data On O_{26} to O_{18} Outputs [1]	Data On O_{17} to O_9 Outputs [1]	Data On O_8 to O_0 Outputs [1]
L	L	X	L	None (x36 to x36)	D_{35} to D_{27}	D_{26} to D_{18}	D_{17} to D_9	D_8 to D_0
L	L	L	H	Big Endian x36 to x18	N/A	N/A	D_{35} to D_{27} 1st Read D_{17} to D_9 2nd Read	D_{26} to D_{18} 1st Read D_8 to D_0 2nd Read
L	L	H	H	Little Endian x36 to x18	N/A	N/A	D_{17} to D_9 1st Read D_{35} to D_{27} 2nd Read	D_8 to D_0 1st Read D_{26} to D_{18} 2nd Read
L	H	L	H	Big Endian x36 to x9	N/A	N/A	N/A	D_{35} to D_{27} 1st Read D_{26} to D_{18} 2nd Read D_{17} to D_9 3rd Read D_8 to D_0 4th Read
L	H	H	H	Little Endian x36 to x9	N/A	N/A	N/A	D_8 to D_0 1st Read D_{17} to D_9 2nd Read D_{26} to D_{18} 3rd Read D_{35} to D_{27} 4th Read
H	L	L	H	Big Endian x18 to x36	D_{17} to D_9 1st Write	D_8 to D_0 1st Write	D_{17} to D_9 2nd Write	D_8 to D_0 2nd Write
H	L	H	H	Little Endian x18 to x36	D_{17} to D_9 2nd Write	D_8 to D_0 2nd Write	D_{17} to D_9 1st Write	D_8 to D_0 1st Write
H	H	L	H	Big Endian x9 to x36	D_8 to D_0 1st Write	D_8 to D_0 2nd Write	D_8 to D_0 3rd Write	D_8 to D_0 4th Write
H	H	H	H	Big Endian x9 to x36	D_8 to D_0 4th Write	D_8 to D_0 3rd Write	D_8 to D_0 2nd Write	D_8 to D_0 1st Write

Notes:
1. Table indicates the relative bits available on these pins for each Endian mode. Data always exits the FIFO in the order received until the FIFO is empty.

Table 6. Endian Byte Programming

Timing Diagrams:

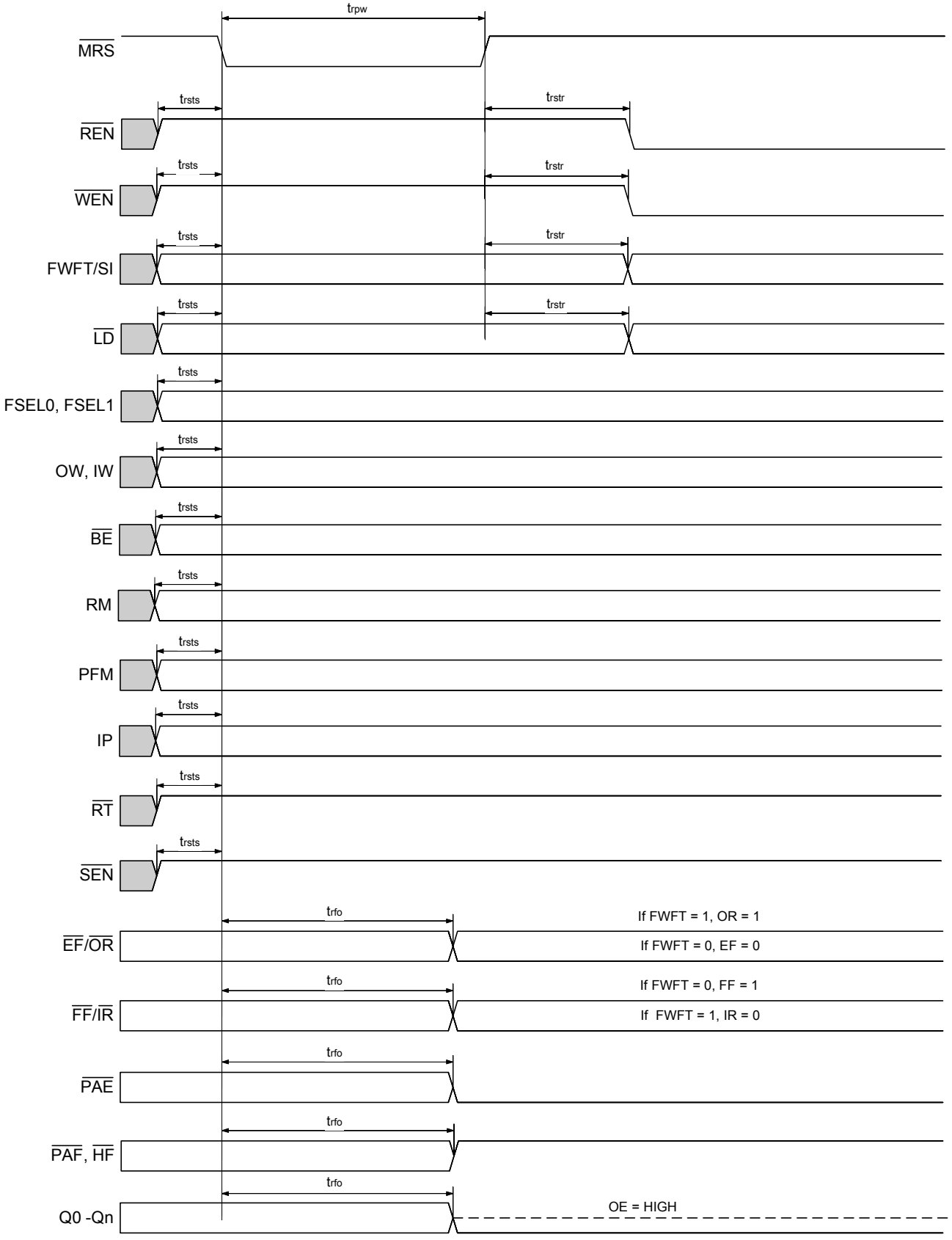


Figure 3. Master Clear (MRS) Timing

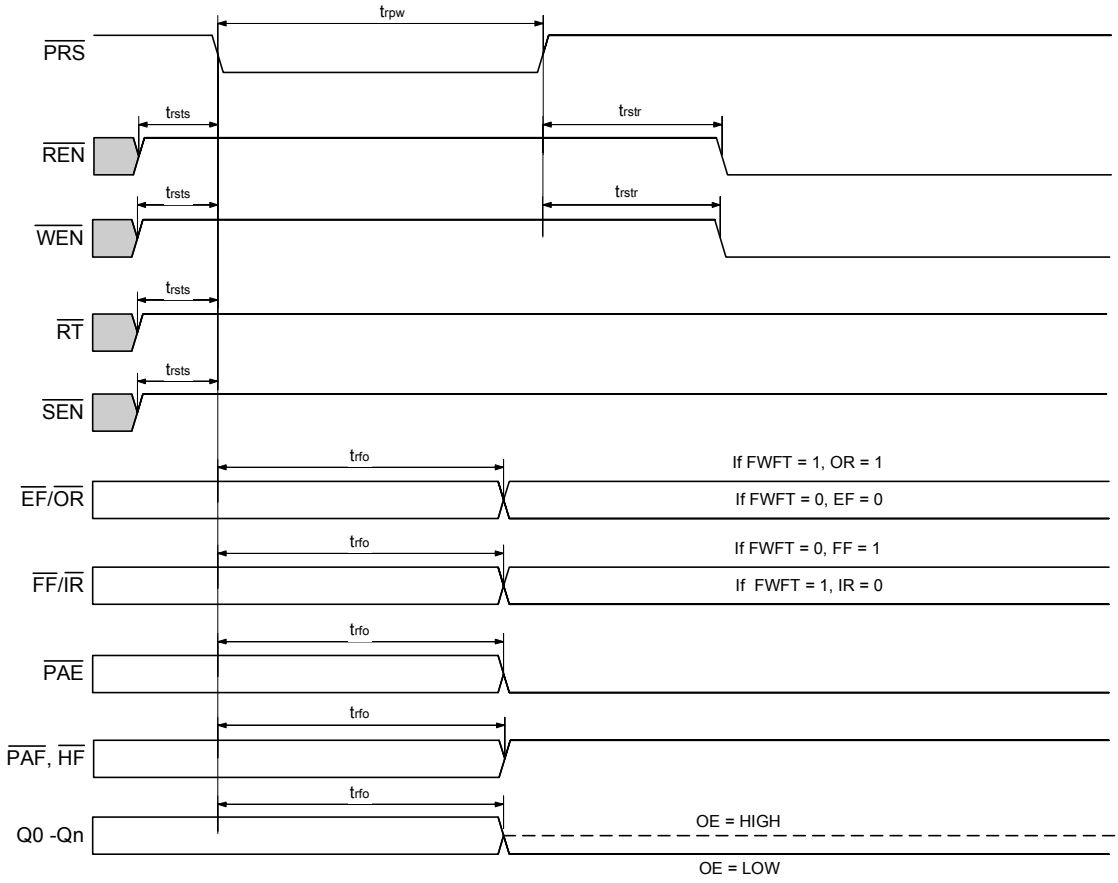
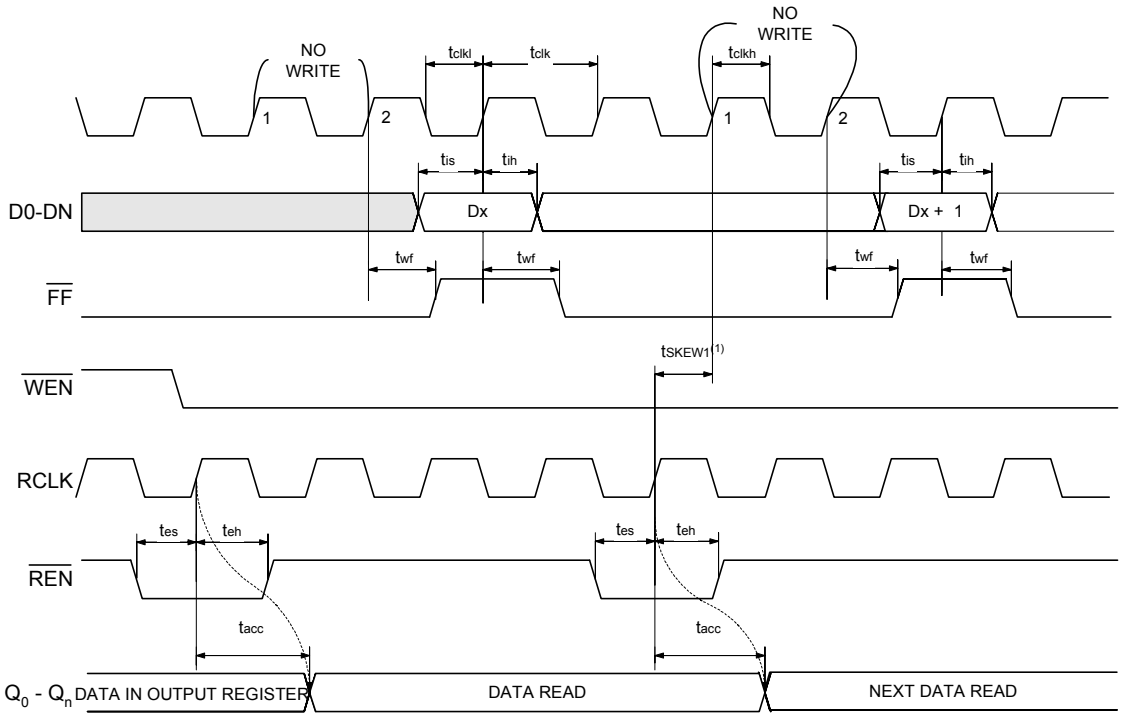


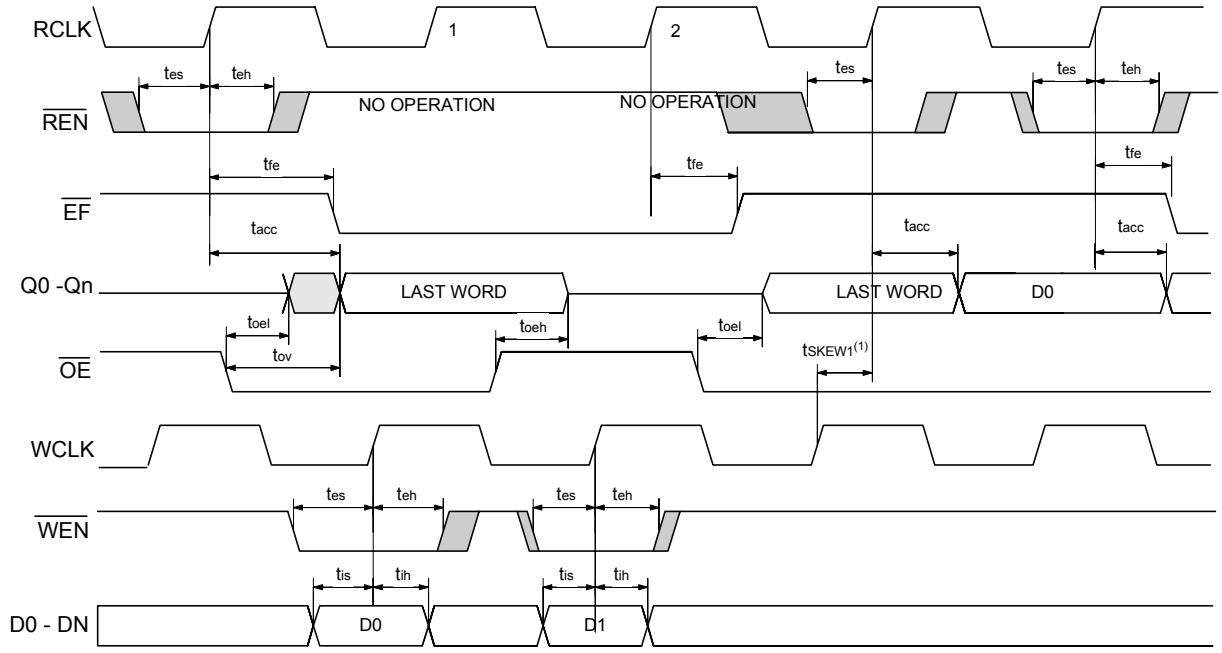
Figure 4. Partial Clear (PRS) Timing



Notes: 1. t_{skew1} indicates the minimum amount of time needed for FF to go high after one clock cycle plus twf. If the time between the RCLK rising edge and thw WCLK rising edge is less than . t_{skew1}, then FF going high may be delayed until the second WCLK.

2. OE equals LOW, EF and LD equals HIGH.

Figure 5. Write Cycle and Full Flag (FF) Timing (Standard Mode)

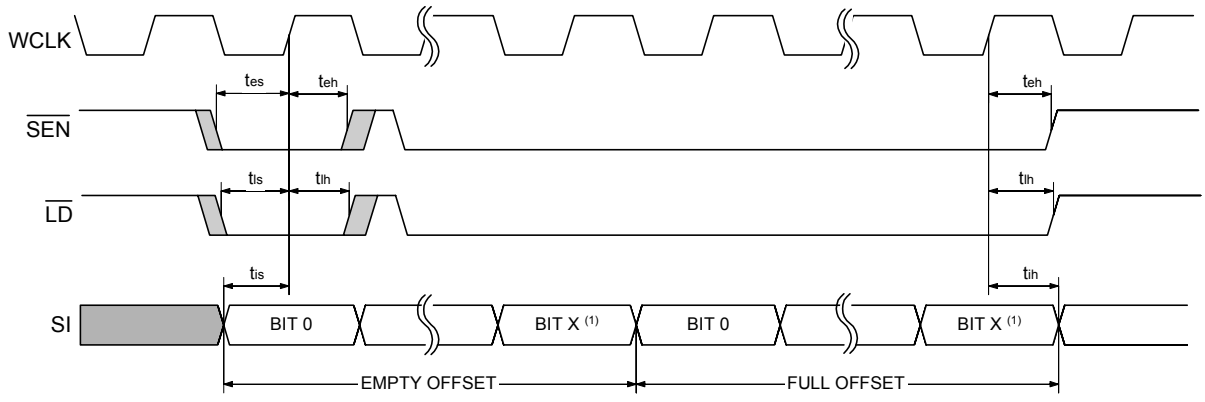


Notes: 1. t_{skew1} indicates the minimum amount of time needed for EF to go high after one clock cycle plus twf. If the time between the WCLK rising edge and the RCLK rising edge is less than t_{skew1}, then FF going high may be delayed until the second RCLK.

2. First data word latency is equal to $t_{skew1,}$ Plus T RCLK, plus tfe.

3. LD equals HIGH.

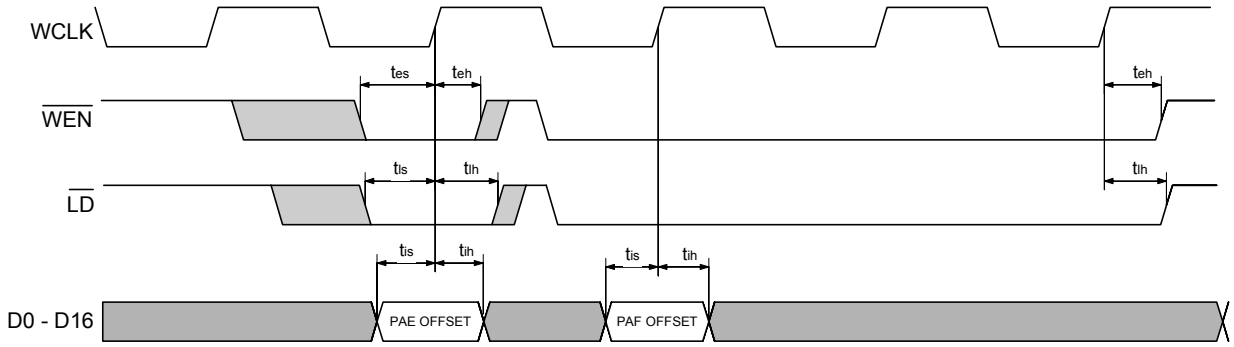
Figure 6. Read Cycle, First Data Latency and Empty Flag (EF) Timing (Standard Mode)



Note: 1. Bit “X” indicates the last bit loaded as shown in chart (above). Bit “X” equals the following for each device type.

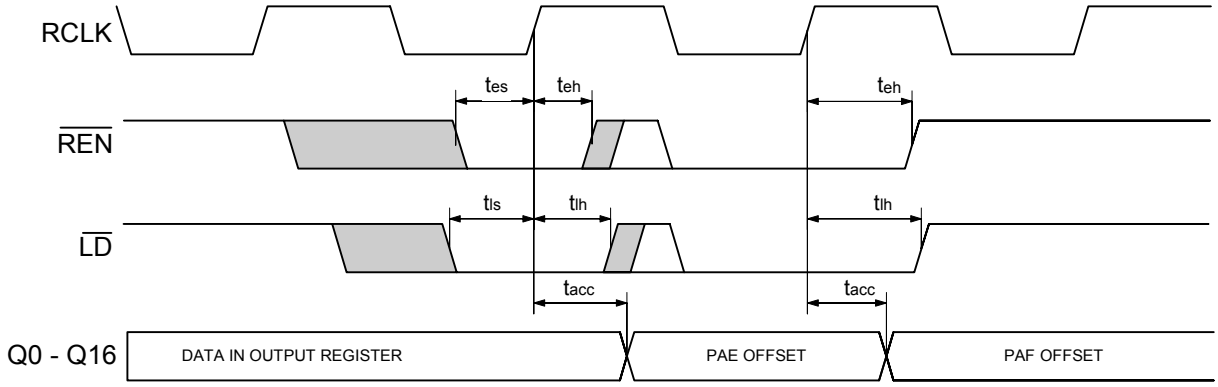
3630 - Bit X = 8 Bits
3640 - Bit X = 9 Bits
3650 - Bit X = 10 Bits
3660 - Bit X = 11 Bits
3670 - Bit X = 12 Bits
3680 - Bit X = 13 Bits
3690 - Bit X = 14 Bits

Figure 7. Programmable Flag Register Serial Loading (Standard and FWFT Modes)



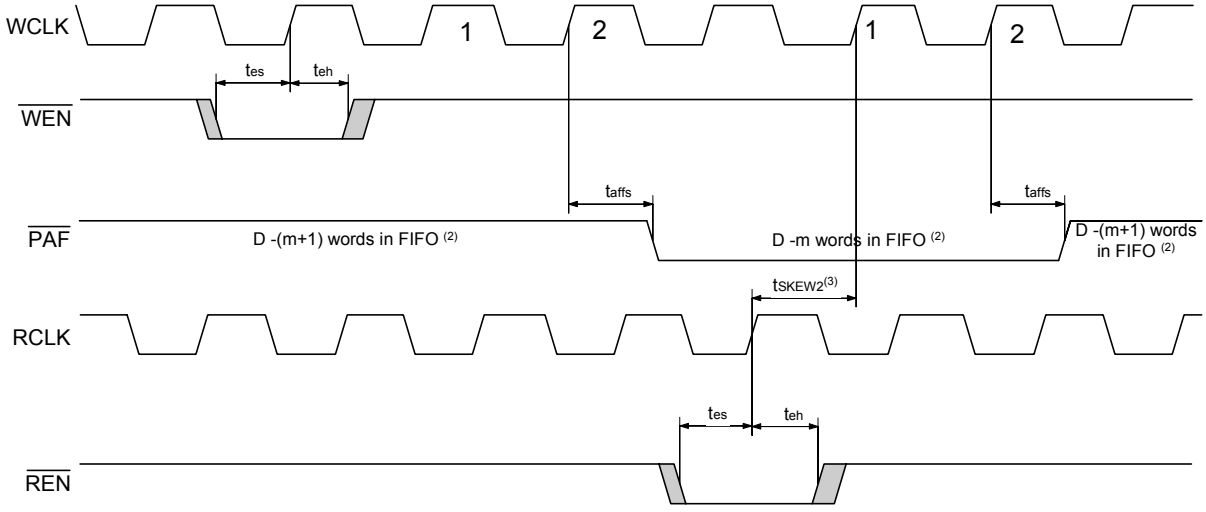
Note: 1. This timing illustrates a 36-Bit input bus width.

Figure 8. Programmable Flag Register Parallel Loading (Standard and FWFT Modes)



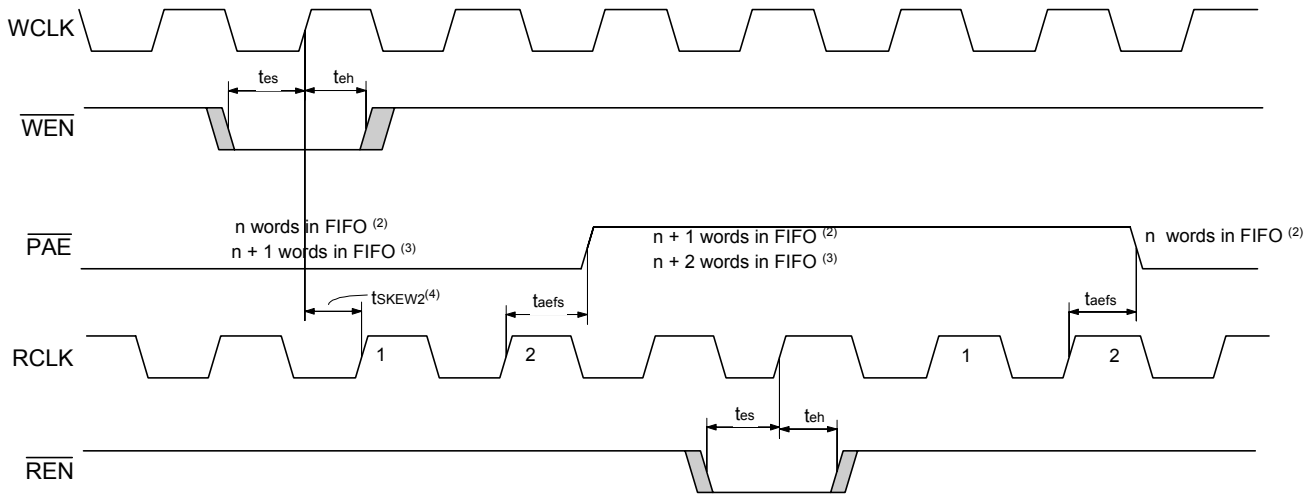
Note: 1. This timing illustrates a 36-Bit output bus width.
2. OE is lOW.

Figure 9. Programmable Flag Register Parallel Reading (Standard and FWFT Modes)



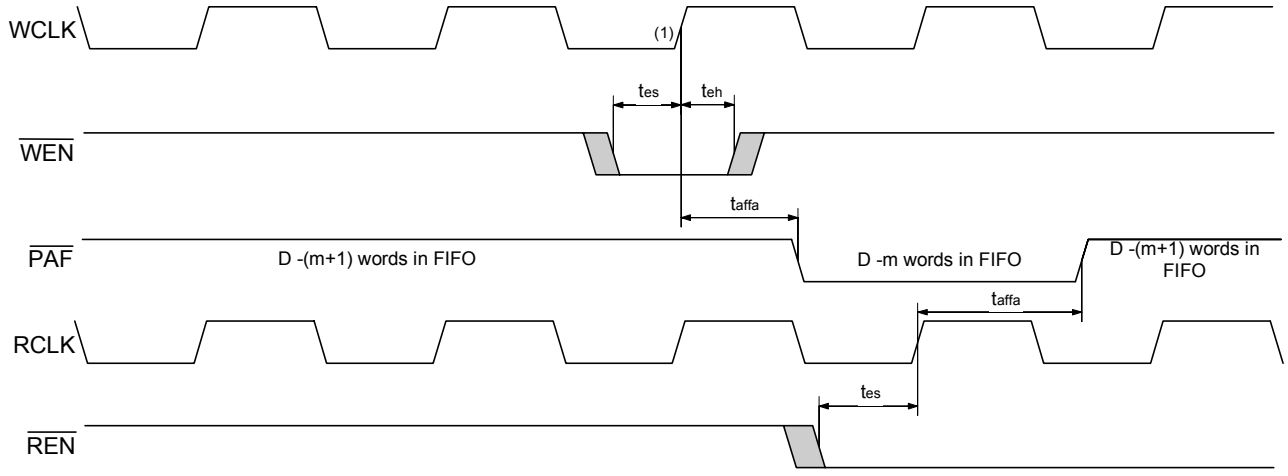
Note: 1. D (above) equals the maximum FIFO depth, 512 for the 3630, 1024 for the 3640, etc.
2. m equals the PAF offset.
3. t_{skew2} indicates the minimum amount of time needed for PAF to go high after one clock cycle plus taffs. If the time between the RCLK rising edge and the WCLK rising edge is less than then PAF may be delayed one extra WCLK clock cycle.
4. PAF goes low on the rising edge of RCLK only.
5. This mode is selected by setting PFM high during master clear (MRS).

Figure 10. Synchronous Programmable Almost Full (PAF) Timing (Standard and FWFT Modes)



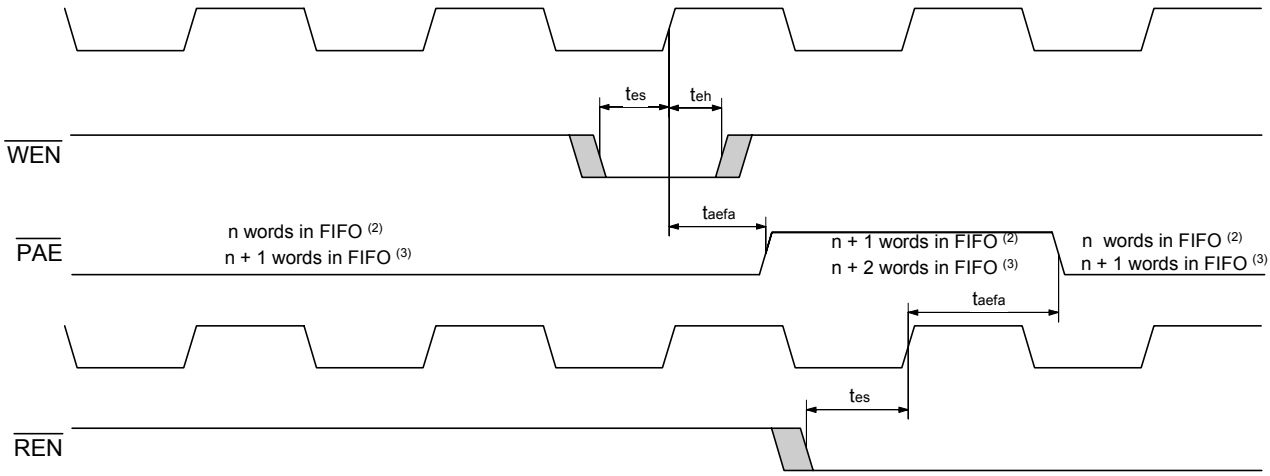
Notes: 1. n equals the PAE offset.
2. For Standard mode
3. For FWFT Mode
4. t_{skew2} indicates the minimum amount of time needed for PAE to go high after one RCLK clock cycle plus taefs. If the time between the WCLK rising edge and the RCLK rising edge is less than t_{skew2} then PAF may be delayed one extra RCLK clock cycle.
5. PAE goes low on the rising edge of WCLK only.
6. This mode is selected by setting PFM High during master clear (MRS).

Figure 11. Synchronous Programmable Almost Full (PAE) Timing (Standard and FWFT Modes)



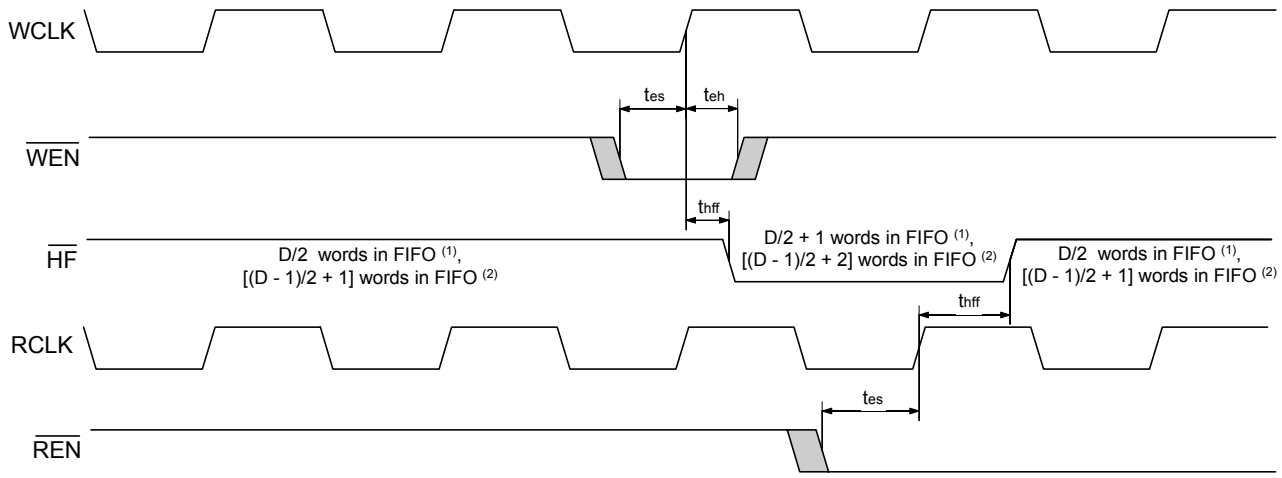
Notes: 1. D (above) equals the maximum FIFO depth, 512 for the 3630, 1024 for the 3640, etc.
2. m equals the PAF offset.
3. PAF goes high due to a RCLK rising edge transition, and goes low due to the rising edge of a WCLK transition.
4. This mode is selected by setting PFM low during master clear (MRS).

Figure 12. Asynchronous Programmable Almost Full (PAF) Timing (Standard and FWFT Modes)



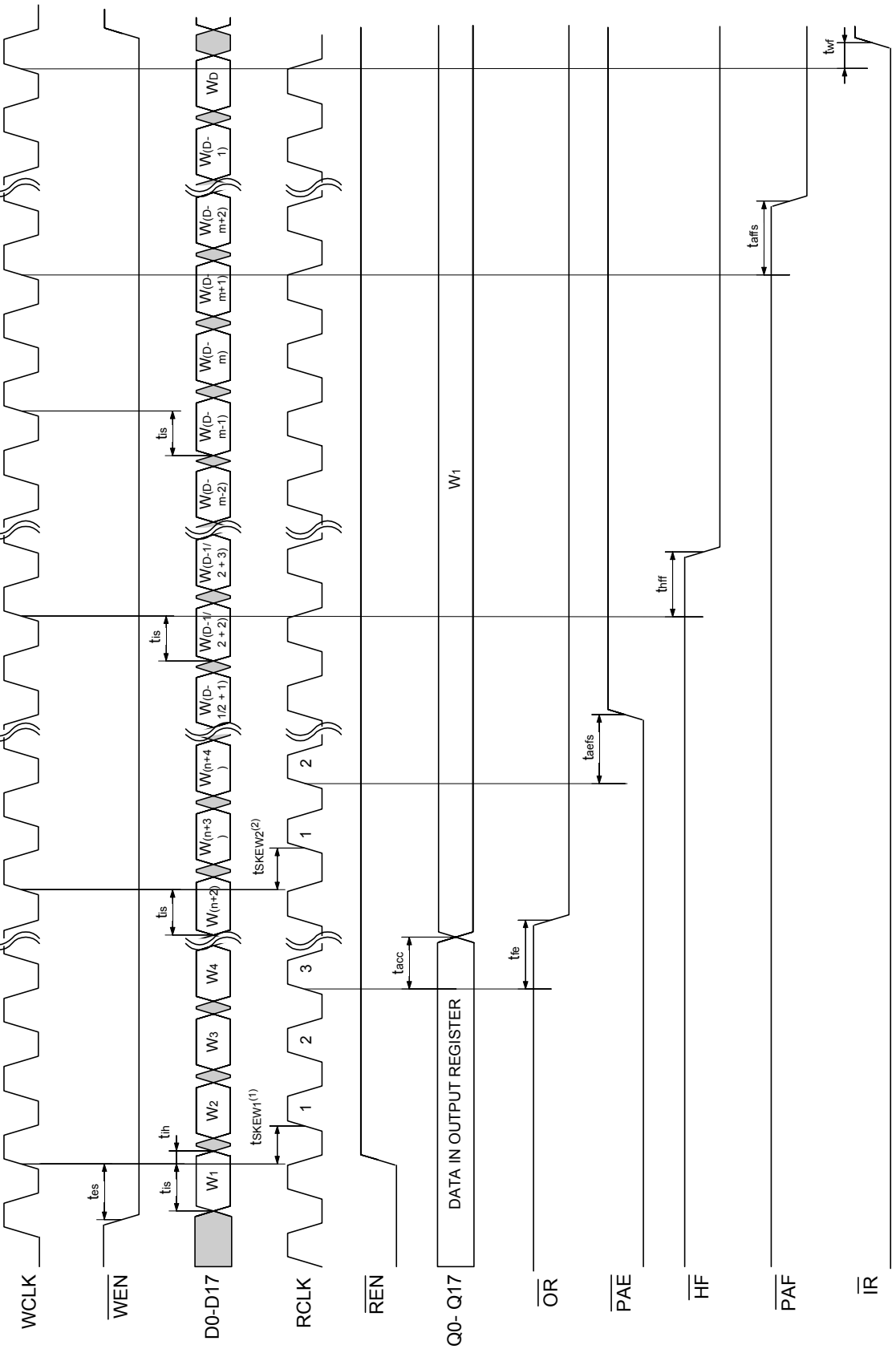
Notes: 1. n equals the PAE offset.
2. For Standard mode
3. For FWFT Mode
4. PAE goes high due to a WCLK rising edge transition, and goes low due to the rising edge of a RCLK transition.
5. This mode is selected by setting PFM High during master clear (MRS).

Figure 13. Asynchronous Programmable Almost Empty (PAE) Timing (Standard and FWFT Modes)



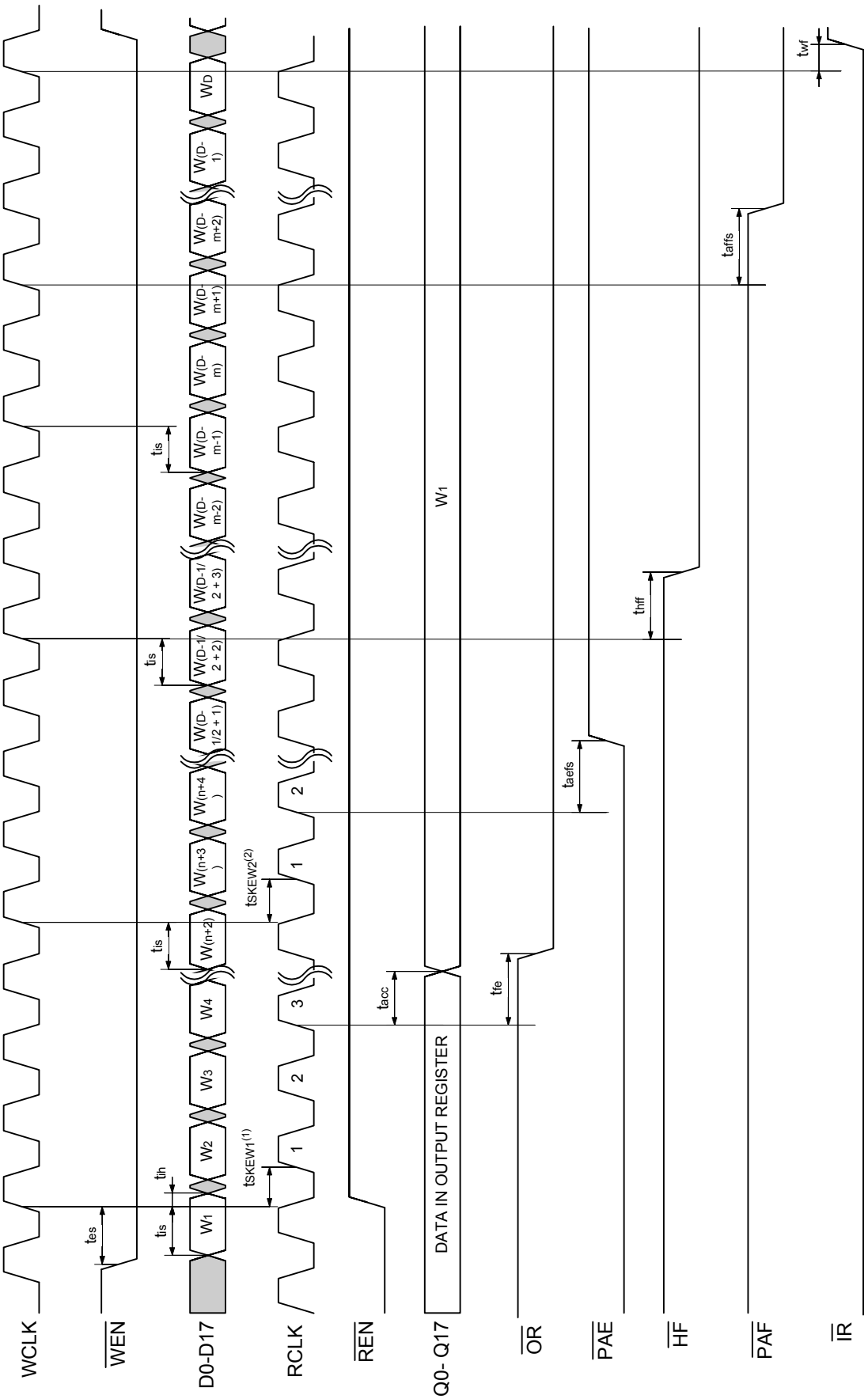
Notes: 1. For Standard Mode, D (above) equals the maximum FIFO depth, 512 for the 3630, 1024 for the 3640, etc.
2. For FWFT Mode, D (above) equals the maximum FIFO depth plus 1, 513 for the 3630, 1025 for the 3640, etc.

Figure 14. Half Full Flag (HF) Timing (Standard and FWFT modes)



Notes:
1. The minimum time needed between the rising edge of WCLK and the rising edge of RCLK for OR to go low after two RCLK cycles plus tfe is indicated by t_{SKEW1}. IR may be delayed one extra RCLK cycle if the time between rising edges of WCLK and RCLK are less than t_{SKEW1}. If the time between
2. The minimum time between the rising edge of WCLK and the rising edge of RCLK for PAE to go high after one RCLK cycle plus taefs is t_{SKEW2}. If the rising edges of WCLK and RCLK are less than t_{SKEW2}, PAE going high may be delayed one extra RCLK cycle.
3. m equals the PAF offset, n equals the PAE offset.
4. LD equals high, OE equals low.
5. D equals one more than the total length of the FIFO. D equals 513 for the 3630, D equals 1025 for the 3640, and so forth.

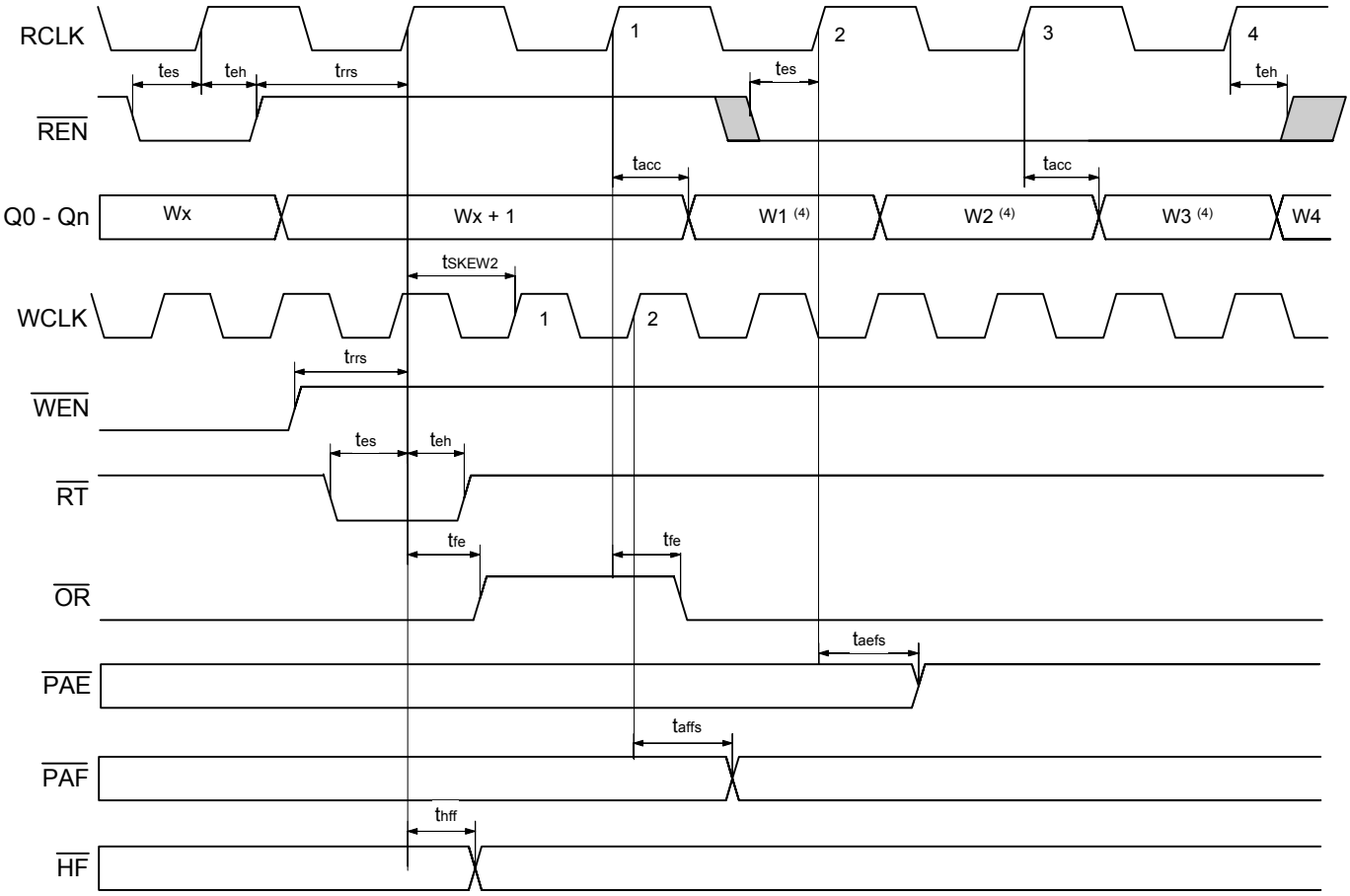
Figure 15. Write Timing – First Word Fall Through



Notes:

1. The minimum time needed between the rising edge of RCLK and the rising edge of WCLK for IR to Go low after one WCLK cycle plus twf is indicated by t_{SKEW1}. IR may be delayed an extra WCLK if the time between rising edges of RCLK and WCLK are less than t_{SKEW1}.
2. The minimum time between the rising edge of RCLK and the rising edge of WCLK for PAF to go high after one RCLK clock cycle plus tafs is indicated by t_{SKEW2}. If the time between rising edges of RCLK and WCLK are less than tSKEW2, PAF going high may be delayed an extra WCLK cycle.
3. m equals the PAF offset, n equals the PAE offset.
4. LD equals high.
5. D equals one more than the total length of the FIFO. D equals 513 for the 3630, 1025 for the 3640, and so forth.

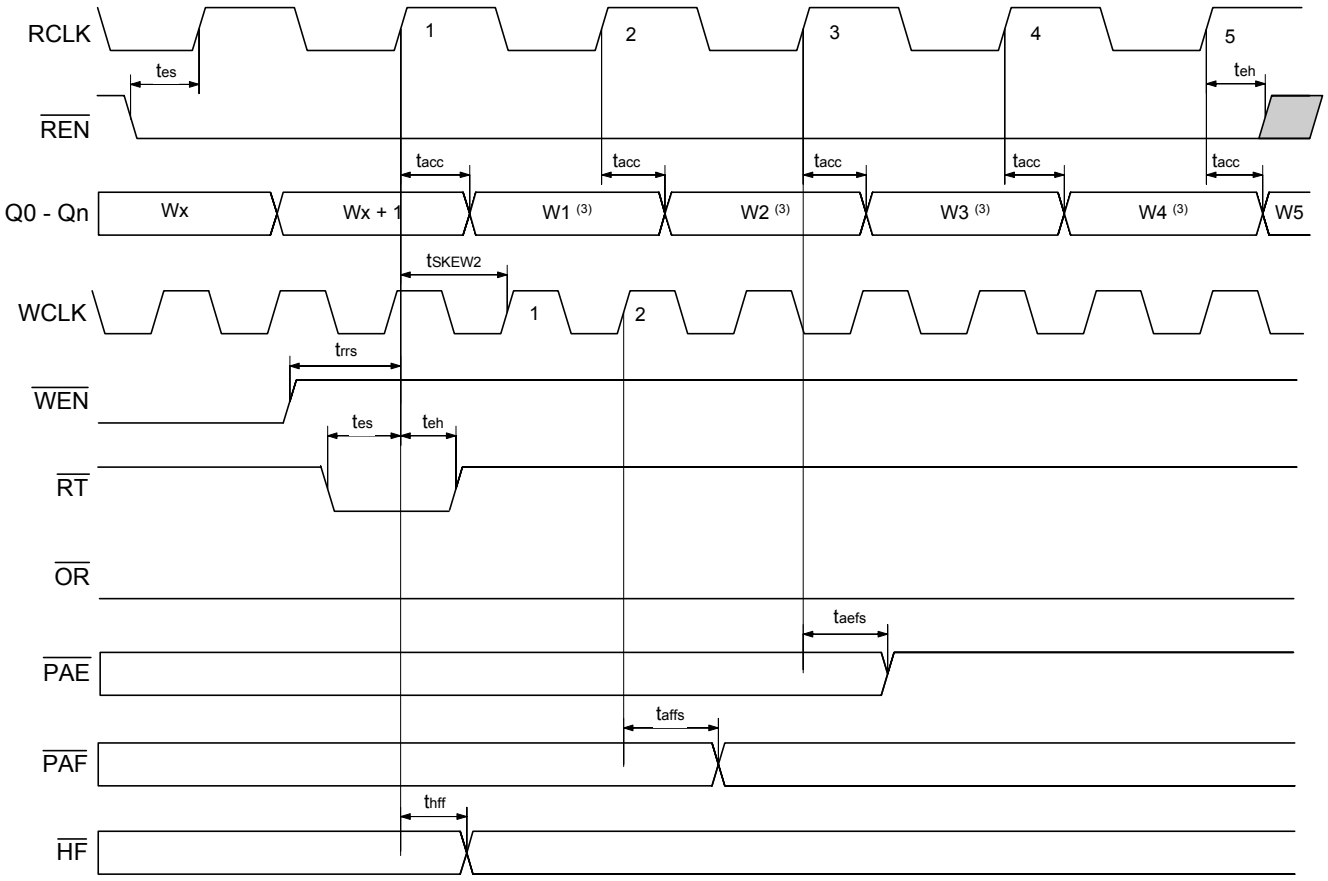
Figure 16. Read Timing – First Word Fall Through



Notes:

1. OR Returns low after Retransmit setup is complete.
2. Between either Master Clear (MRS) or Partial Clear (PRS) and Retransmit setup no more than D-2 words can be written to the FIFO.
3. A minimum of two words must be written to the FIFO before Retransmit can be activated.
4. The first words written into the FIFO after Master Clear (MRS) are indicated by W1, W2 and W3.
5. OE equals low, and RM is set high during Master Clear (MRS).

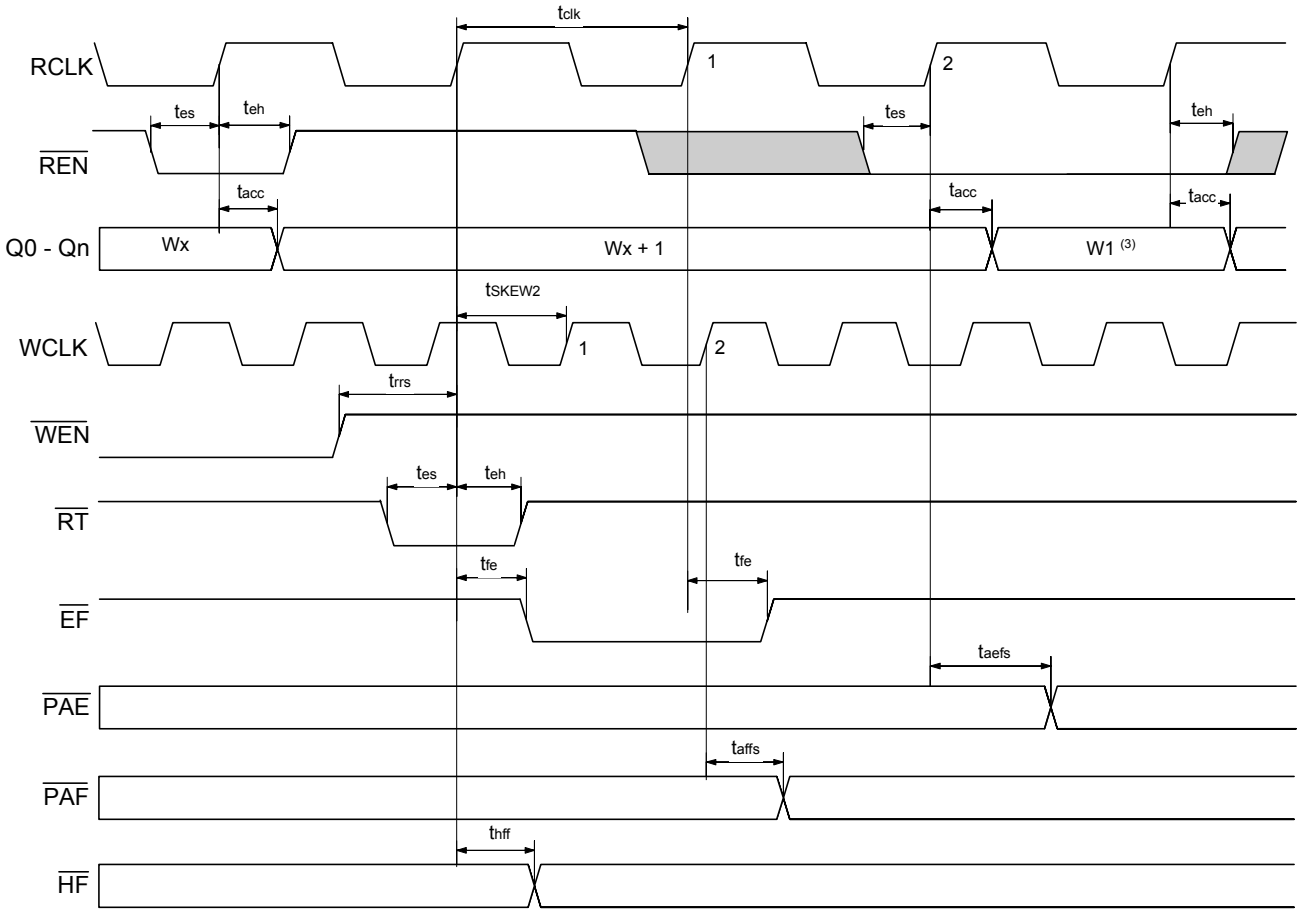
Figure 17. Retransmit Timing - FWFT Mode



Notes:

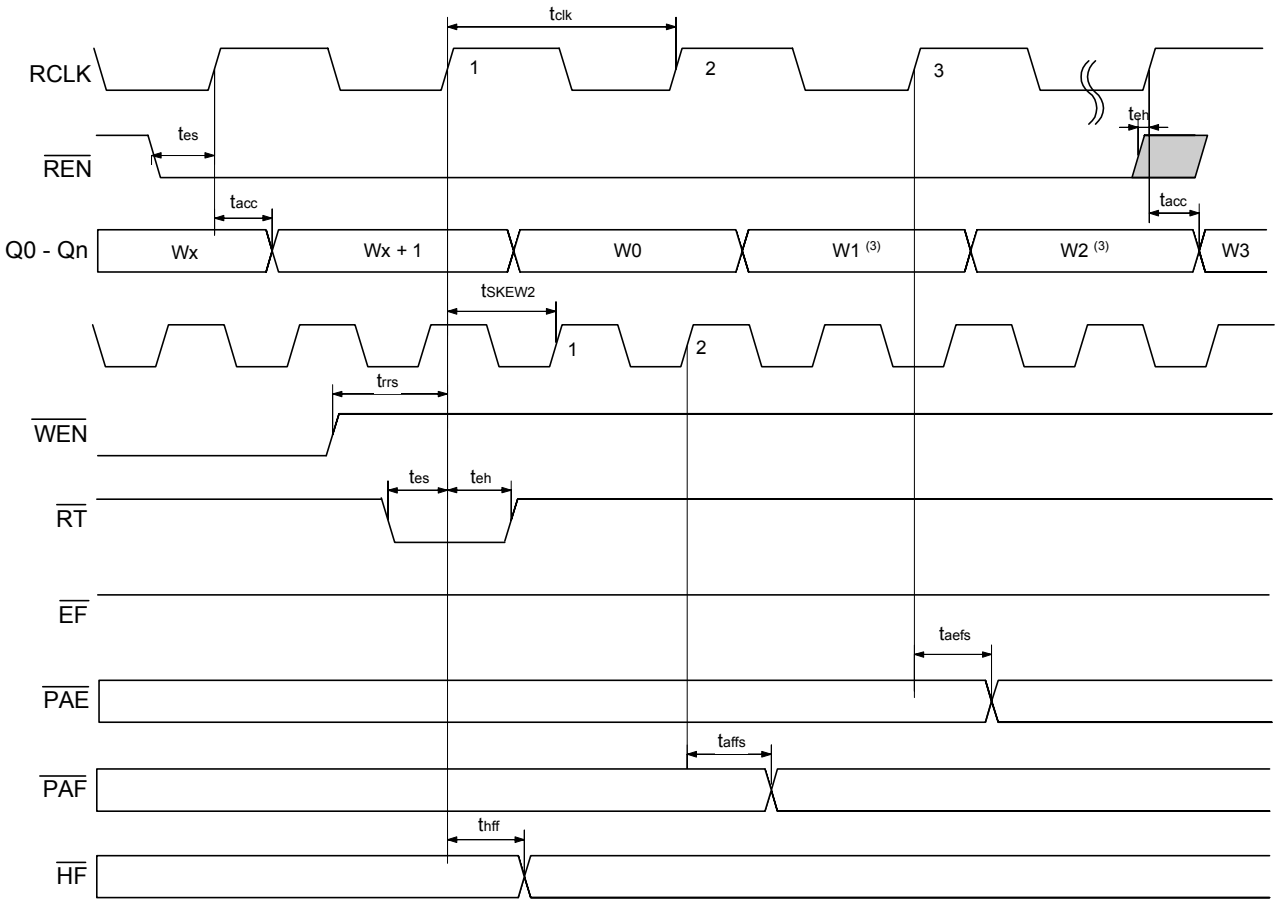
1. OR will update based upon RCLK (Retransmit Clock Cycle) if the FIFO is empty when Retransmit starts. The outputs will also contain valid data.
2. Between either Master Clear (MRS) or Partial Clear (PRS) and Retransmit setup no more than D-2 words can be written to the FIFO. D equals 513 for the 3630, 1025 for the 3640, and so forth. This means that IR will be low for the entire Retransmit setup.
3. A minimum of two words must be written to the FIFO before Retransmit can be activated.
4. The first few words written into the FIFO after Master Clear (MRS) are indicated by W1, W2 and W3.
5. OE equals low, and RM is set high during Master Clear (MRS).

Figure 18. Zero Latency Retransmit Timing, FWFT Mode



1. Between either Master Clear (MRS) or Partial Clear (PRS) and Retransmit setup no more than D-2 words can be written to the FIFO. D equals the total size of the FIFO, 512 for the 3630, 1024 for the 3640, and so forth. This means that FF will be high for the entire retransmit setup.
2. A minimum of two words must be written to the FIFO before Retransmit can be activated.
3. The first two words written into the FIFO after Master Clear (MRS) are indicated by W1 and W2.
4. OE equals low, and RM is set high during Master Clear (MRS).
5. EF will return high after Retransmit setup is complete. A read operation can only begin after that point.

Figure 19. Retransmit Timing - Standard Mode



Notes:

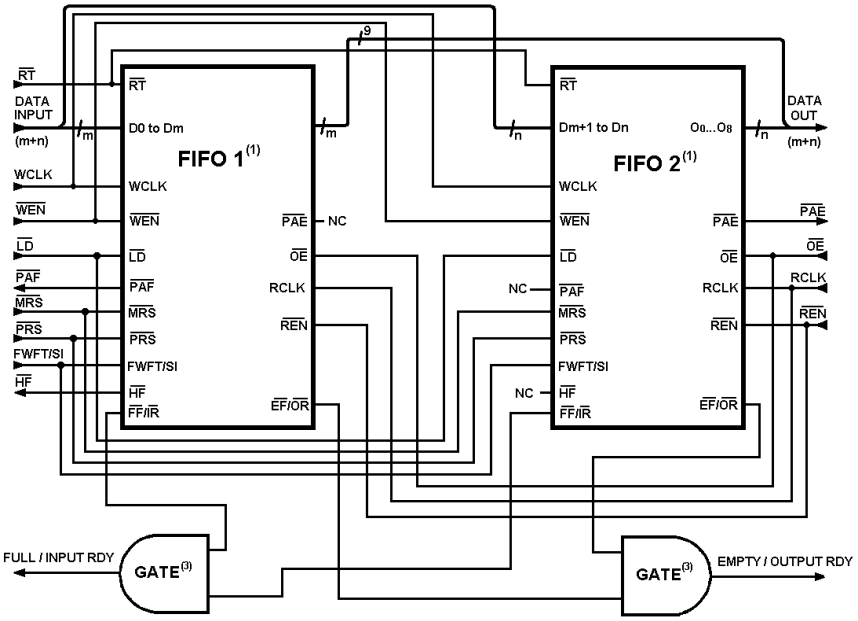
1. The Empty Flag (EF) will update based upon RCLK (Retransmit Clock Cycle) If the FIFO is empty when Retransmit starts. The outputs will also contain valid data.
2. Between either Master Clear (MRS) or Partial Clear (PRS) and Retransmit setup no more than D-2 words can be written to the FIFO. D equals 512 for the 3630, 1024 for the 3640, and so forth. This means that FF will be high for the entire Retransmit setup.
3. A minimum of two words must be written to the FIFO before Retransmit can be activated.
4. The first two words written into the FIFO after Master Clear (MRS) are indicated by W1 and W2.
5. OE equals low, and RM is set low during Master Clear (MRS).

Figure 20. Zero latency Retransmit Timing - Standard Mode

FIFO Applications and Operation:

JSI VeloSync+ FIFOs offer a high degree of design flexibility for various configurations. They can be utilized as a single device, connected in parallel for wider bus applications, or can be organized for deeper FIFO applications.

Multiple Device Width Expansion:



Notes:

1. Similar FIFO depths must be used, but word widths may be different.
2. Output control signals should never be directly tied together.
3. For standard Mode an “AND “ gate is required. For FWFT Mode, an “OR” Gate is required.

Figure 21. Width Expansion

These FIFOs can be easily expanded to support wider word widths by connecting the control inputs of multiple devices in the manner shown above. The Full Flag/Input Ready ($\overline{FF}/\overline{IR}$) and Empty Flag/Output Ready ($\overline{EF}/\overline{OR}$) of each device must combined via either an “AND” gate for FIFO Operation in Standard Mode, or an “OR” gate for FIFO operation in FWFT Mode to create a combined Full Flag/Input Ready and an Empty Flag/Output Ready that indicates the combined status of the FIFOs.

Multiple Device Depth Expansion:

Each of the J72V3630 Series FIFOs can be connected in series without the requirement for extra logic as long as the FWFT mode of operation is selected during Master clear ($\overline{MRS}$). As long as matching x9 or x18 configurations are selected for each device, combinations of FIFOs can be connected in series to provide a total FIFO with a depth equivalent to the sum off the individual FIFOs. The diagram shows two FIFOs connected in such a fashion.

The requirement for FWFT operation means that the first, and each additional word that is written into the leading FIFO will automatically ripple down to the last FIFO and will be available to be read from the last FIFO outputs. This is accomplished by having a free running Transfer Clock between each series connected FIFO.

When the FIFOs are empty the time taken for the first word written into the first FIFO to ripple to the last FIFO outputs equals the sum of all delays of each FIFO in the chain, plus one Transfer Clock time for each additional FIFO added in series. The ripple delay will only be apparent when writing to empty FIFOs. The Ripple time has no effect when data has already rippled down to the last FIFO.

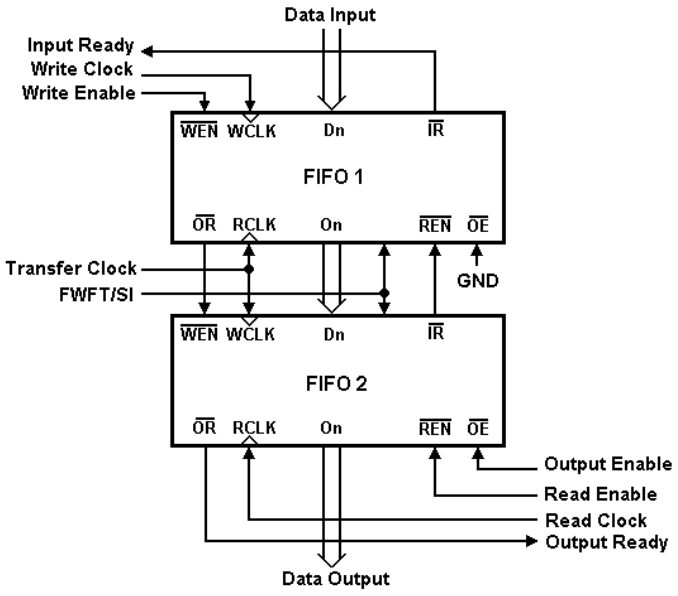
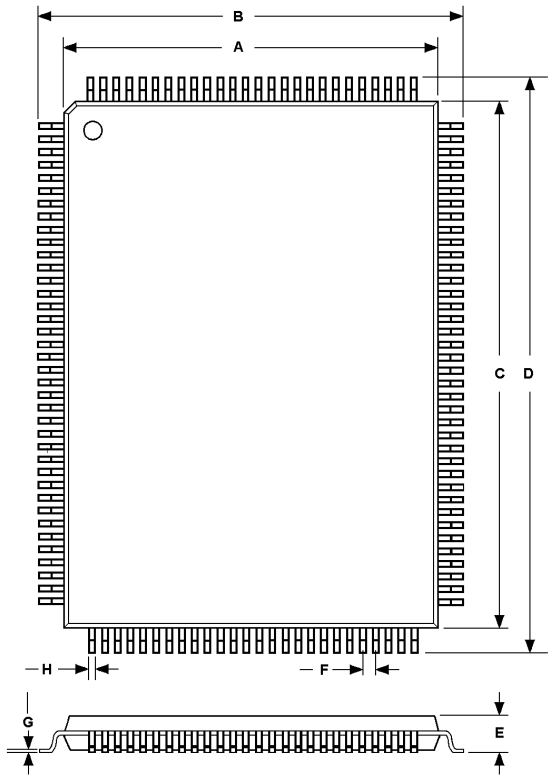


Figure 22. Depth Expansion

Packaging: 128 pin Thin Quad Flat Pack (TQFP)



	128 Pin TQFP
A	14.0 mm
B	16.0 mm
C	20.0 mm
D	22.0 mm
E	1.60 mm
F	0.50 mm
G	.05 mm Min .15 mm Max
H	0.22 mm

Please contact JMAR Semiconductor, Inc. for full package drawings and tolerances.

Figure 23. Package Outline

Ordering Information:

J JSI

72V XXXX Device Type
- 3630 (512 x 36 Bits)
- 3640 (1024 x 36 Bits)
- 3650 (2048 x 36 Bits)
- 3660 (4096 x 36 Bits)
- 3670 (8192 x 36 Bits)
- 3680 (16,384 x 36 Bits)
- 3690 (32,768 x 36 Bits)

L Power
- L= Low Power

X.X Speed
- 15 = 66 MHz
- 10 = 100 MHz
- 7.5 = 133MHz

T Package
- T= Thin Quad Flat Pack

X Temperature Range
- Blank - Commercial (0°C to +70° C)
- I = Industrial (-40°C to +85° C)

Product Replacement Chart

Size	Speed	JSI Part Number	IDT Part Number
512 x 36	133 MHz	**J72V3630L7.5**	IDT72V3630L7.5
1024 x 36	133 MHz	**J72V3640L7.5**	IDT72V3640L7.5
2048 x 36	133 MHz	**J72V3650L7.5**	IDT72V3650L7.5
4096 x 36	133 MHz	**J72V3660L7.5**	IDT72V3660L7.5
8192 x 36	133 MHz	**J72V3670L7.5**	IDT72V3670L7.5
16384 x 36	133 MHz	**J72V3680L7.5**	IDT72V3680L7.5
32768 x 36	133 MHz	**J72V3690L7.5**	IDT72V3690L7.5
512 x 36	100 MHz	**J72V3630L10**	IDT72V3630L10
1024 x 36	100 MHz	**J72V3640L10**	IDT72V3640L10
2048 x 36	100 MHz	**J72V3650L10**	IDT72V3650L10
4096 x 36	100 MHz	**J72V3660L10**	IDT72V3660L10
8192 x 36	100 MHz	**J72V3670L10**	IDT72V3670L10
16384 x 36	100 MHz	**J72V3680L10**	IDT72V3680L10
32768 x 36	100 MHz	**J72V3690L10**	IDT72V3690L10
512 x 36	66 MHz	**J72V3630L15**	IDT72V3630L15
1024 x 36	66 MHz	**J72V3640L15**	IDT72V3640L15
2048 x 36	66 MHz	**J72V3650L15**	IDT72V3650L15
4096 x 36	66 MHz	**J72V3660L15**	IDT72V3660L15
8192 x 36	66 MHz	**J72V3670L15**	IDT72V3670L15
16384 x 36	66 MHz	**J72V3680L15**	IDT72V3680L15
32768 x 36	66 MHz	**J72V3690L15**	IDT72V3690L15

JSI's FIFOs utilize an internally regulated 2.5V core to provide high performance at Low Power

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