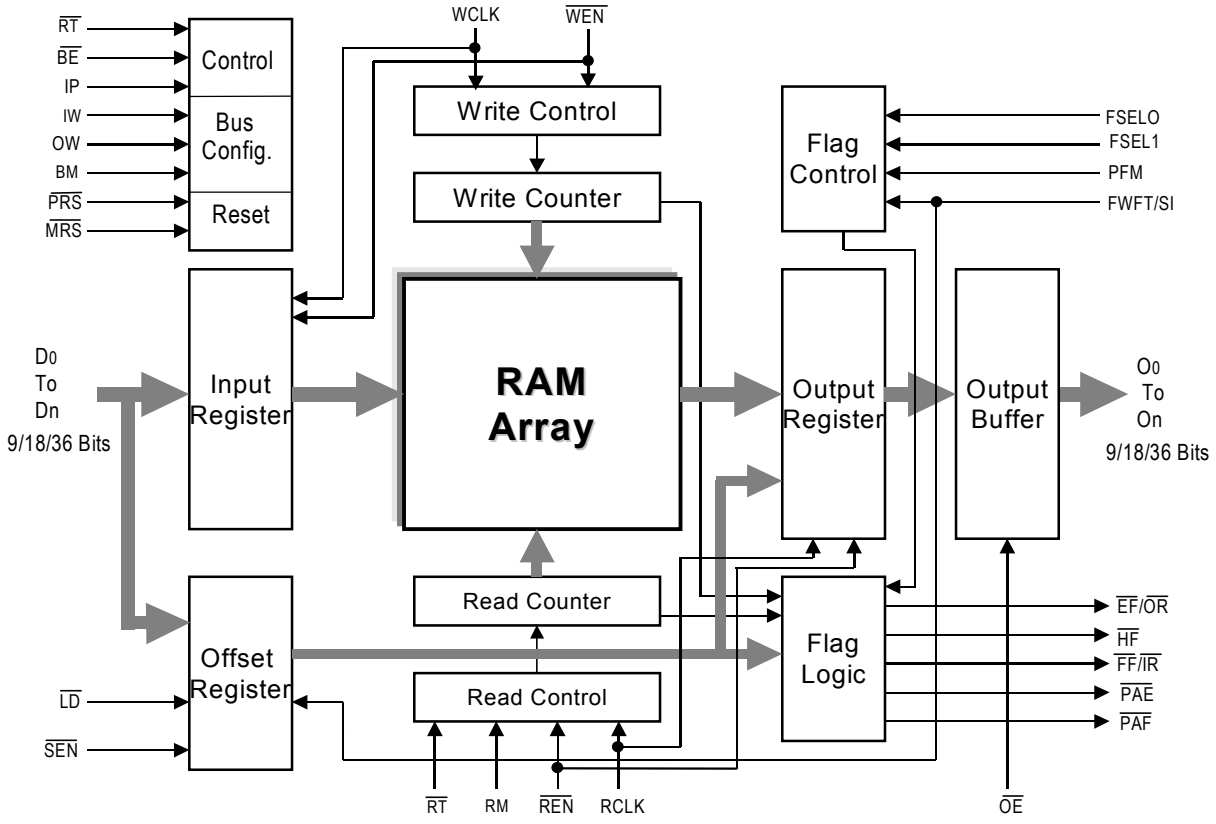
Product Summary

J72V3630 512 x 36 Bits J72V3640 1,024 x 36 Bits J72V3650 2,048 x 36 Bits J72V3660 4,096 x 36 Bits
J72V3670 8,192 x 36 Bits J72V3680 16,384 x 36 Bits J72V3690 32,768 x 36 Bits

VeloSync+$_{TM}$ High Performance 36 Bit Wide 3.3V Synchronous FIFO

Features:

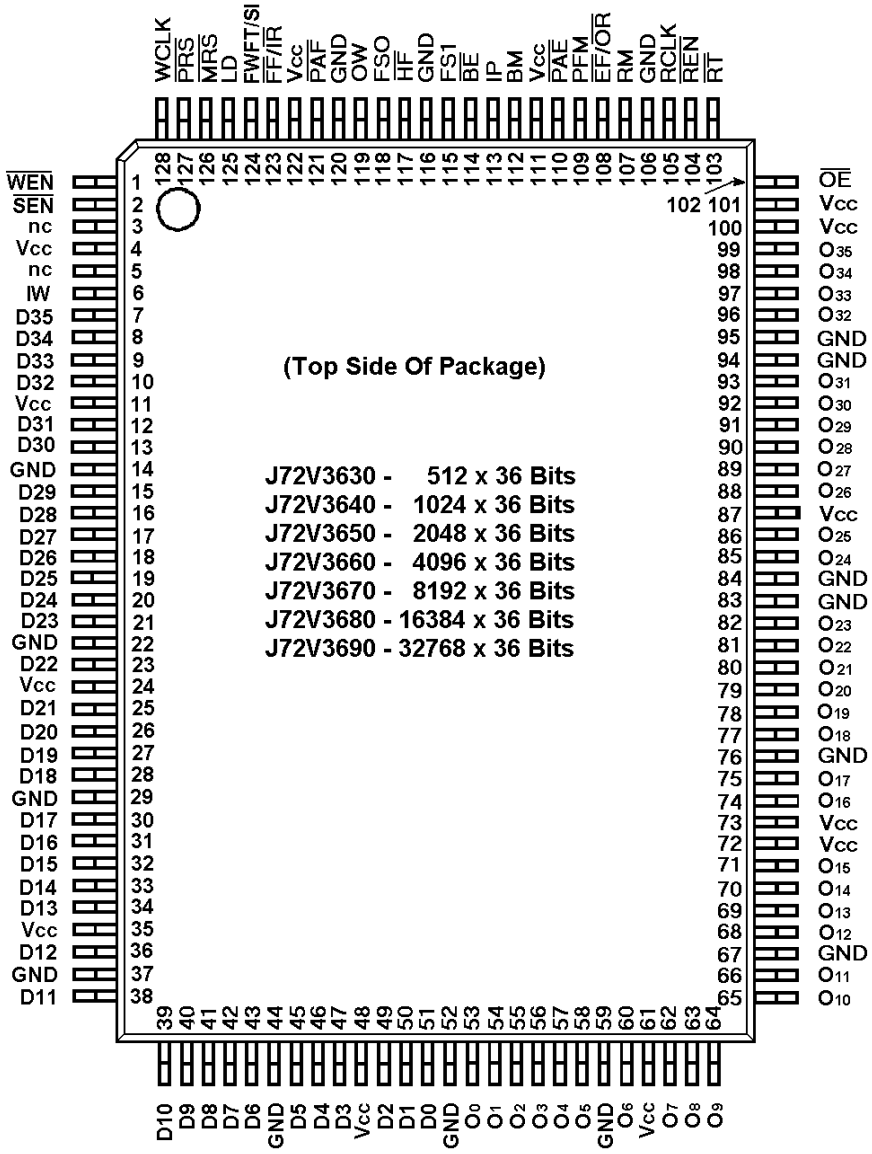
- **Very High Performance – 133 MHz Max Clock Rate**
- **Low Power Requirements**
- **5 ns Data Access Time**
- **7.5 ns Read/Write Cycle Times**
- **Separate and Independent Read / Write Clocking**
- **Bus Configuration Select Pins For x9, x18, and x36 Input and Output Widths**
- **FIFO Empty, FIFO Half Full and FIFO Full Status Flags**
- **Choice of Partial Clear or Master Clear**
- **3.3 V Operation, 5V Tolerant Device Inputs**
- **Cascade Capability to Expand Width and Depth**
- **Designed For Zero Fall-Through Timing**
- **Retransmit Feature With Zero Latency**
- **Almost Empty and Almost Full Flags Are Programmable With Default To One Of Eight Pre-selected Offsets**
- **Fixed, Low First Word Latency**
- **Programmable Endian Byte Views**
- **Programmable Flags Can Be Set Up in Parallel or Serial Fashion**
- **Programmable Flags Can Be Set Up for Asynchronous or Synchronous Operation**
- **Output Enable for 3-State Mode Control of Data Bus**
- **Offered in 128-Pin Plastic Thin Quad Flat Pack (TQFP)**
- **Commercial (0°C to +70°C) and Industrial (-40° C to +85° C.) Temperatures Available**
- **High Performance, Lower-Power Replacement For Industry Standard FIFOs (See Page 31)**



Device Description:

These very high-performance, low-power synchronous First-In/First-Out (FIFO) buffer memories are directly pin and function compatible with currently available industry standard FIFOs. They offer independently clocked read and write controls, provide maximum operational flexibility, and utilize synchronous read and write clocking for easy system design. An Input Bus Configuration of x36 may have either a x9, x18, or x36 Output Bus Configuration. An Output Bus Configuration of x36 may have either a x9, x18, or x36 Input Bus Configuration. Bus Configurations are programmed by the $\overline{IW}$, $\overline{OW}$, and BM input pins during Master Clear. These FIFOs offer high performance, while providing lower power than similar devices when utilized at comparable clock rates. They are offered in 1,024, 2048, 4096, 8,192, 16,384, 32,768, 65,536, and 131,072 x36 bit wide organizations with cascading capability in both width and depth to match a variety of data buffering requirements. These FIFOs are a cost effective solution to provide elastic data buffering for data communications, multi-processing, networking, video, and graphics applications. The data input port is controlled by WCLK, a free-running clock, and $\overline{WEN}$, a Write Enable pin. Each rising edge of the clock writes data into the FIFO when the write enable pin is active. RCLK and the Read Enable pin $\overline{REN}$, control reading the FIFO in the same manner. Both the Read Clock and the Write Clock can be tied together for single clock operation or each clock can be utilized asynchronously for dual, separate clock operation. $\overline{OE}$ provides control of the read output 3-state buffer for use in direct bus applications.

For maximum flexibility and ease of use, these FIFOs offer two programmable flags to indicate Almost Full and Almost Empty as well as the standard Full ($\overline{FF}$), Half Full (HF), and Empty ($\overline{EF}$) flags. The programmable flag offsets are set to default values during Master Clear ($\overline{MRS}$) by one of the eight states of the LD, FSEL0, and FSEL1 input pins. Parallel and Serial loading of these offsets to any value is also available. Parallel loading occurs via the Data Inputs on the rising edge of the Write Clock (WCLK) when Write Enable (WEN) and Load ($\overline{LD}$) inputs are low. Serial loading of these offsets via the Serial Input (SI of the FWFT/SI pin) occurs on each rising edge of the Write Clock (WCLK) when the Serial Load (SL) and Load ($\overline{LD}$) inputs are low. Master Clear ($\overline{MRS}$) and Partial Clear ($\overline{PRS}$) are asynchronous low signals that reset the output register, the output register, the write pointer and the read pointer to zero. During Master Clear ($\overline{MRS}$), the state of the FWFT/SI input pin selects either the Normal Mode or the Fall Through Mode of FIFO operation. If this input pin is high during Master Clear, the Fall Through Mode is selected, and the Input Ready ($\overline{IR}$) and Output Ready ($\overline{OR}$) functions are active. After 3 transitions of the Read Clock (RCLK), the first word input to an empty FIFO is available on the data outputs regardless of the state of Read Enable ($\overline{REN}$) input pin. Additional words input to the FIFO do require a low state of REN in order to be read. Chaining the Data Outputs of one FIFO to the Data Inputs of a second FIFO accomplishes depth expansion when the Fall Through Mode (FWFT) is selected without requiring any other logic. A low on the FWFT/SI pin during Master Clear ($\overline{MRS}$) selects Normal Mode of FIFO operation, and the Full Flag ($\overline{FF}$) an Empty Flag ($\overline{EF}$) functions are active. The first word input to an empty FIFO is available at the data outputs on the first enabled ($\overline{REN}$) rising edge of the Read Clock (RCLK). The functions of the Programmable Almost Full, Almost Empty and Half Full Flags are not affected by the mode selected.



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Product Replacement Chart

Size	Speed	JSI Part Number	IDT Part Number
512 x 36	133 MHz	**J72V3630L7.5**	IDT72V3630L7.5
1024 x 36	133 MHz	**J72V3640L7.5**	IDT72V3640L7.5
2048 x 36	133 MHz	**J72V3650L7.5**	IDT72V3650L7.5
4096 x 36	133 MHz	**J72V3660L7.5**	IDT72V3660L7.5
8192 x 36	133 MHz	**J72V3670L7.5**	IDT72V3670L7.5
16384 x 36	133 MHz	**J72V3680L7.5**	IDT72V3680L7.5
32768 x 36	133 MHz	**J72V3690L7.5**	IDT72V3690L7.5
512 x 36	100 MHz	**J72V3630L10**	IDT72V3630L10
1024 x 36	100 MHz	**J72V3640L10**	IDT72V3640L10
2048 x 36	100 MHz	**J72V3650L10**	IDT72V3650L10
4096 x 36	100 MHz	**J72V3660L10**	IDT72V3660L10
8192 x 36	100 MHz	**J72V3670L10**	IDT72V3670L10
16384 x 36	100 MHz	**J72V3680L10**	IDT72V3680L10
32768 x 36	100 MHz	**J72V3690L10**	IDT72V3690L10
512 x 36	66 MHz	**J72V3630L15**	IDT72V3630L15
1024 x 36	66 MHz	**J72V3640L15**	IDT72V3640L15
2048 x 36	66 MHz	**J72V3650L15**	IDT72V3650L15
4096 x 36	66 MHz	**J72V3660L15**	IDT72V3660L15
8192 x 36	66 MHz	**J72V3670L15**	IDT72V3670L15
16384 x 36	66 MHz	**J72V3680L15**	IDT72V3680L15
32768 x 36	66 MHz	**J72V3690L15**	IDT72V3690L15

JSI's FIFOs utilize an internally regulated 2.5V core to provide high performance at Low Power

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