Product Summary

J72V201…. 256 x 9 Bits **J72V221…. 1024 x 9 Bits** **J72V241…. 4096 x 9 Bits**
J72V211…. 512 x 9 Bits **J72V231…. 2048 x 9 Bits** **J72V251…. 8192 x 9 Bits**

VeloSync™ High Performance 9-Bit 3.3V Synchronous FIFO

Features:

- **Advanced 0.25 Micron CMOS Technology**
- **Very High Performance – 133 MHz Max Clock Rate**
- **7.5 ns Read/Write Cycle Times**
- **5 Volt Tolerant Inputs**
- **Low Power Requirements**
- **Separate and Independent Read / Write Clocking**
- **FIFO Empty and FIFO Full Status Flags**
- **3.3 V Operation, 5V Tolerant Device Inputs**
- **Dual Ported For Zero Fall-Through Timing**
- **High Performance, Lower-Power Replacement For Industry Standard FIFOs**
- **Almost-Empty and Almost-Full Flags are Programmable, With Default To Empty +7, and Full -7**
- **Output Enable for 3-State Mode Control of Data Bus**
- **Packages - 32-Pin Plastic Thin Quad Flat Pack (TQFP) and 32-Pin Plastic Leaded Chip Carrier (PLCC)**
- **Meets Commercial Temperature (0°C to +70°C) and Industrial Temperature (-40°C to +85°C.)**

Device Description:

JSI's VeloSync™ Series very high-performance, low power synchronous First-In/First-Out (FIFO) buffer memories are directly pin and function compatible with currently available industry standard FIFOs for most applications. Independently clocked read and write controls provide maximum operational flexibility, with synchronous read and write clocking providing easy system design. These FIFOs offer much higher performance, while requiring lower power and increased timing margins when utilized at clock rates less than 133 MHz, They are offered in 256, 512, 1,024, 2,048, 4,096 and 8,192 x 9-bit wide organizations to match a variety of data buffering requirements. JSI's FIFOs are a cost effective solution to provide elastic data buffering for data communications, multi-processing, networking, video, and graphics applications. Their input port is controlled by WCLK, a free-running clock, plus WEN1 and WEN2/LD Write Enable pins. Each rising edge of the clock writes data into the FIFO when the write enable pins are active. RCLK and two Read Enable pins REN1, REN2 control reading the FIFO in the same manner. Both the Read Clock and the Write Clock can be tied together for single clock operation or each clock can be utilized asynchronously for dual, separate clock operation. OE provides control of the read output 3-state buffer for use in direct bus applications.

For maximum flexibility and ease of use, these FIFOs offer two programmable flags to indicate Almost Full and Almost Empty as well as the standard Full and Empty flags. The programmable flags are organized to automatically default to Empty +7, and Full -7, and can be easily modified via activation of the WEN2/LD signal.