

**Formerly Available As FSJ055R4,
Radiation Hardened, SEGR Resistant,
N-Channel Power MOSFETs**

The Discrete Products Operation of Intersil has developed a series of Radiation Hardened MOSFETs specifically designed for commercial and military space applications. Enhanced Power MOSFET immunity to Single Event Effects (SEE), Single Event Gate Rupture (SEGR) in particular, is combined with 100 krad of total dose hardness to provide devices which are ideally suited to harsh space environments. The dose rate and neutron tolerance necessary for military applications have not been sacrificed.

The Intersil portfolio of SEGR resistant radiation hardened MOSFETs includes N-Channel and P-Channel devices in a variety of voltage, current and on-resistance ratings. Numerous packaging options are also available.

This MOSFET is an enhancement-mode silicon-gate power field-effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to be radiation tolerant. The MOSFET is well suited for applications exposed to radiation environments such as switching regulation, switching converters, motor drives, relay drivers and drivers for high-power bipolar switching transistors requiring high speed and low gate drive power. This type can be operated directly from integrated circuits.

Also available at other radiation and screening levels. See us on the web, Intersil's home page: www.intersil.com. Contact your local Intersil Sales Office for additional information.

Die Family TA17650.

MIL-PRF-19500/654.

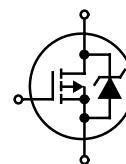
Ordering Information

PART NUMBER	PACKAGE	BRAND
JANSR2N7430T1	TO-254AA	JANSR2N7430T1

Features

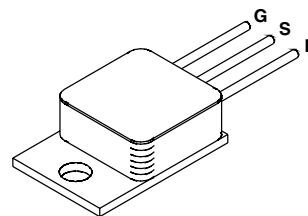
- 70A (Current Limited by Package), 60V, $r_{DS(ON)} = 0.012\Omega$
- Total Dose
 - Meets Pre-Rad Specifications to 100 krad (Si)
- Single Event
 - Safe Operating Area Curve for Single Event Effects
 - SEE Immunity for LET of 36MeV/mg/cm² with V_{DS} up to 80% of Rated Breakdown and V_{GS} of 10V Off-Bias
- Dose Rate
 - Typically Survives 3E9 Rad (Si)/s at 80% BV_{DSS}
 - Typically Survives 2E12 if Current Limited to I_{DM}
- Photo Current
 - 6nA Per-Rad (Si)/s Typically
- Neutron
 - Maintain Pre-Rad Specifications for 3E13 Neutrons/cm²
- Usable to 3E14 Neutrons/cm²

Symbol



Packaging

TO-254AA



CAUTION: Beryllia Warning per MIL-PRF-19500 refer to package specifications.

JANSR2N7430

Absolute Maximum Ratings $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

	JANSR2N7430	UNITS
Drain to Source Voltage V_{DS}	60	V
Drain to Gate Voltage ($R_{GS} = 20k\Omega$) V_{DGR}	60	V
Continuous Drain Current $T_C = 25^\circ\text{C}$ I_D	70 (Note)	A
$T_C = 100^\circ\text{C}$ I_D	54	A
Pulsed Drain Current I_{DM}	200	A
Gate to Source Voltage V_{GS}	± 20	V
Maximum Power Dissipation $T_C = 25^\circ\text{C}$ P_T	151	W
$T_C = 100^\circ\text{C}$ P_T	60	W
Linear Derating Factor	1.20	W/ $^\circ\text{C}$
Single Pulsed Avalanche Current, $L = 100\mu\text{H}$, (See Test Figure) I_{AS}	200	A
Continuous Source Current (Body Diode) I_S	70	A
Pulsed Source Current (Body Diode) I_{SM}	200	A
Operating and Storage Temperature T_J, T_{STG}	-55 to 150	$^\circ\text{C}$
Lead Temperature (During Soldering) T_L (Distance $>0.063\text{in}$ (1.6mm) from Case, 10s Max)	300	$^\circ\text{C}$
Weight (Typical)	9.3	g

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE: Current is limited by the package capability.

Electrical Specifications $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	$I_D = 1\text{mA}, V_{GS} = 0\text{V}$		60	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 1\text{mA}$	$T_C = -55^{\circ}\text{C}$	-	-	5.0	V
			$T_C = 25^{\circ}\text{C}$	1.5	-	4.0	V
			$T_C = 125^{\circ}\text{C}$	0.5	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 48\text{V}, V_{GS} = 0\text{V}$	$T_C = 25^{\circ}\text{C}$	-	-	25	μA
			$T_C = 125^{\circ}\text{C}$	-	-	250	μA
Gate to Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20\text{V}$	$T_C = 25^{\circ}\text{C}$	-	-	100	nA
			$T_C = 125^{\circ}\text{C}$	-	-	200	nA
Drain to Source On-State Voltage	$V_{DS(ON)}$	$V_{GS} = 12\text{V}, I_D = 70\text{A}$		-	-	0.88	V
Drain to Source On Resistance	$r_{DS(ON)12}$	$I_D = 54\text{A}, V_{GS} = 12\text{V}$	$T_C = 25^{\circ}\text{C}$	-	0.008	0.012	Ω
			$T_C = 125^{\circ}\text{C}$	-	-	0.022	Ω
Turn-On Delay Time	$t_{d(ON)}$	$V_{DD} = 30\text{V}, I_D = 70\text{A}, R_L = 0.43\Omega, V_{GS} = 12\text{V}, R_{GS} = 2.35\Omega$		-	-	40	ns
Rise Time	t_r			-	-	200	ns
Turn-Off Delay Time	$t_{d(OFF)}$			-	-	70	ns
Fall Time	t_f			-	-	40	ns
Total Gate Charge (Not on slash sheet)	$Q_g(TOT)$	$V_{GS} = 0\text{V to } 20\text{V}$	$V_{DD} = 30\text{V}, I_D = 70\text{A}$	-	-	280	nC
Gate Charge at 12V	$Q_g(12)$	$V_{GS} = 0\text{V to } 12\text{V}$		-	150	170	nC
Threshold Gate Charge (Not on slash sheet)	$Q_g(TH)$	$V_{GS} = 0\text{V to } 2\text{V}$		-	-	12	nC
Gate Charge Source	Q_{gs}			-	35	43	nC
Gate Charge Drain	Q_{gd}			-	59	81	nC
Thermal Resistance Junction to Case	$R_{\theta JC}$			-	-	0.83	$^{\circ}\text{C/W}$
Thermal Resistance Junction to Ambient	$R_{\theta JA}$			-	-	40	$^{\circ}\text{C/W}$

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Forward Voltage	V_{SD}	$I_{SD} = 70A$	0.6	-	1.8	V
Reverse Recovery Time	t_{rr}	$I_{SD} = 70A$, $dI_{SD}/dt = 100A/\mu s$	-	-	250	ns

Electrical Specifications up to 100 krad $T_C = 25^\circ C$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
Drain to Source Breakdown Volts (Note 3)	BV_{DSS}	$V_{GS} = 0$, $I_D = 1mA$	60	-	V
Gate to Source Threshold Volts (Note 3)	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = 1mA$	1.5	4.0	V
Gate to Body Leakage (Notes 2, 3)	I_{GSS}	$V_{GS} = \pm 20V$, $V_{DS} = 0V$	-	100	nA
Zero Gate Leakage (Note 3)	I_{DSS}	$V_{GS} = 0$, $V_{DS} = 48V$	-	25	μA
Drain to Source On-State Volts (Notes 1, 3)	$V_{DS(ON)}$	$V_{GS} = 12V$, $I_D = 70A$	-	0.88	V
Drain to Source On Resistance (Notes 1, 3)	$r_{DS(ON)12}$	$V_{GS} = 12V$, $I_D = 54A$	-	0.012	Ω

NOTES:

1. Pulse test, 300 μs Max.
2. Absolute value.
3. Insitu Gamma bias must be sampled for both $V_{GS} = 12V$, $V_{DS} = 0V$ and $V_{GS} = 0V$, $V_{DS} = 80\% BV_{DSS}$.

Single Event Effects (SEB, SEGR) Note 4

TEST	SYMBOL	ENVIRONMENT (NOTE 5)			APPLIED V_{GS} BIAS (V)	(NOTE 6) MAXIMUM V_{DS} BIAS (V)
		ION SPECIES	TYPICAL LET (MeV/mg/cm ²)	TYPICAL RANGE (μ)		
Single Event Effects Safe Operating Area	SEESO A	Ni	26	43	-20	60
		Br	37	36	-10	60
		Br	37	36	-15	48
		Br	37	36	-20	36
		I	60	31	0	60
		I	60	31	-5	48
		I	60	31	-10	36
		I	60	31	-15	24
		I	60	31	-20	12

NOTES:

4. Testing conducted at Brookhaven National Labs; sponsored by Naval Surface Warfare Center (NSWC), Crane, IN.
5. Fluence = 1E5 ions/cm² (typical), $T_C = 25^\circ C$.
6. Does not exhibit Single Event Burnout (SEB) or Single Event Gate Rupture (SEGR).

Performance Curves

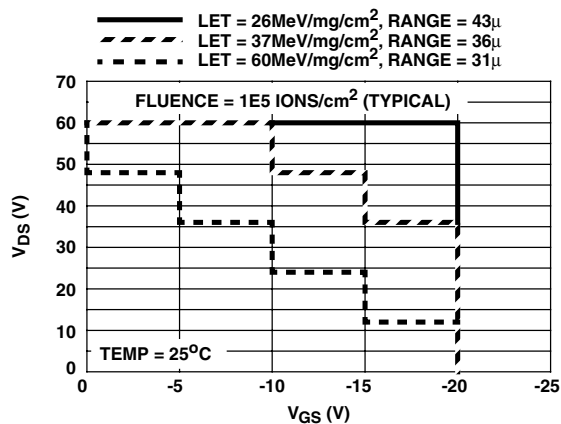


FIGURE 1. SINGLE EVENT EFFECTS SAFE OPERATING AREA

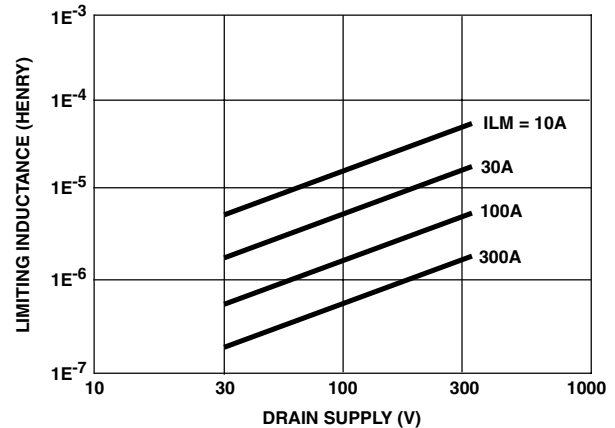


FIGURE 2. TYPICAL DRAIN INDUCTANCE REQUIRED TO LIMIT GAMMA DOT CURRENT TO I_{AS}

Performance Curves (Continued)

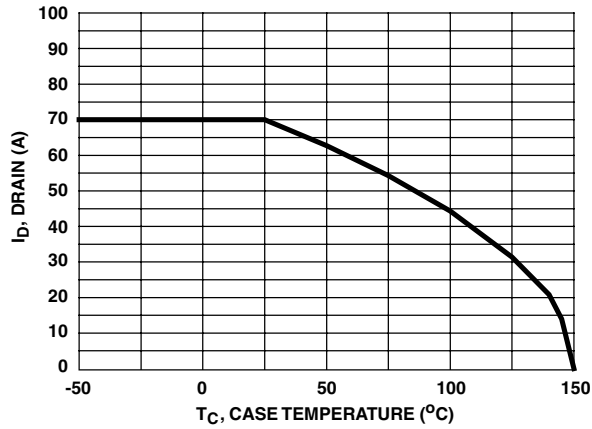


FIGURE 3. MAXIMUM CONTINUOUS DRAIN CURRENT vs TEMPERATURE

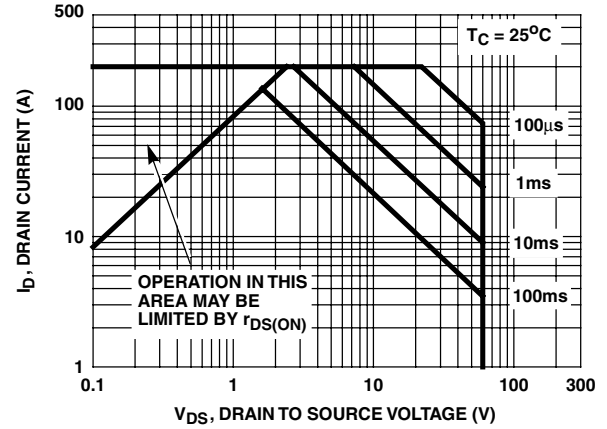


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

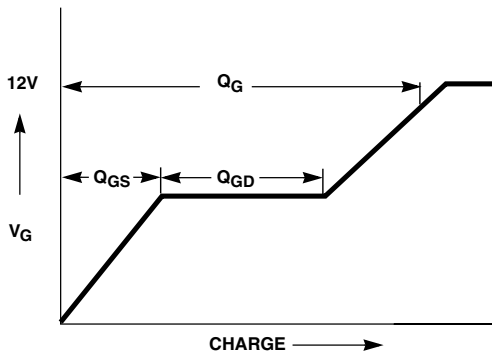


FIGURE 5. BASIC GATE CHARGE WAVEFORM

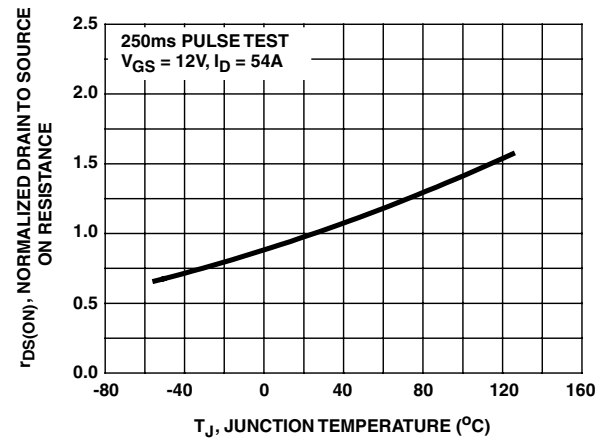


FIGURE 6. TYPICAL NORMALIZED $r_{DS(ON)}$ vs JUNCTION TEMPERATURE

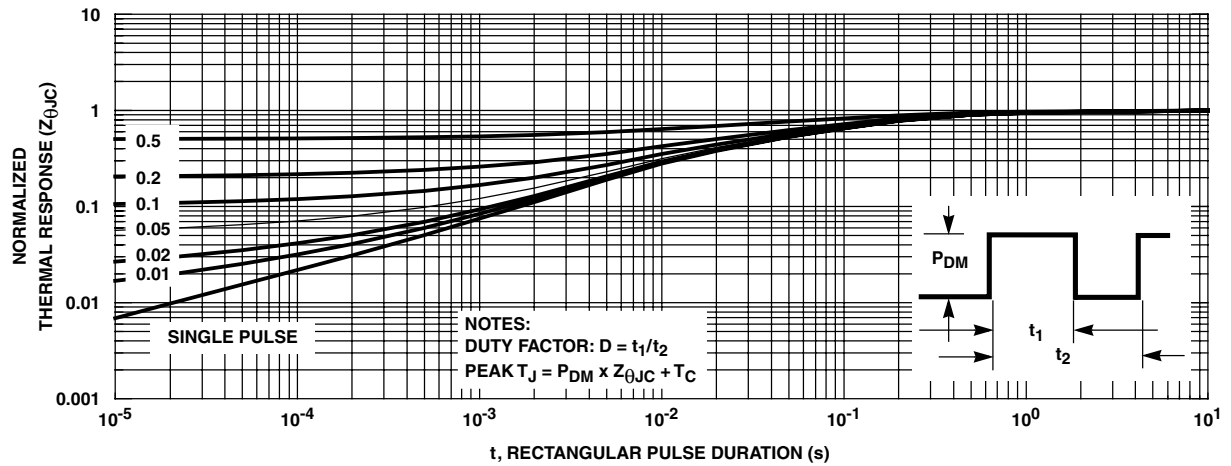


FIGURE 7. NORMALIZED MAXIMUM TRANSIENT THERMAL RESPONSE

Performance Curves (Continued)

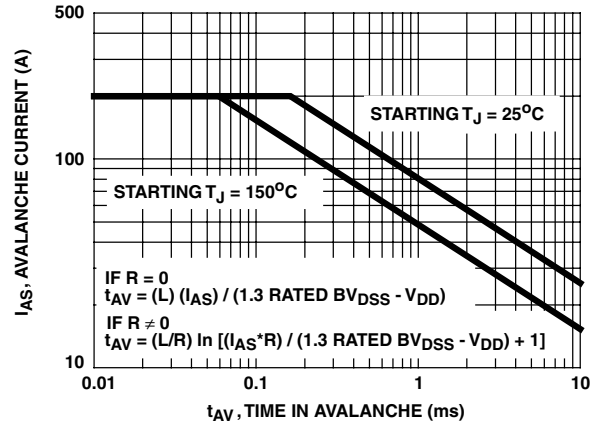


FIGURE 8. UNCLAMPED INDUCTIVE SWITCHING

Test Circuits and Waveforms

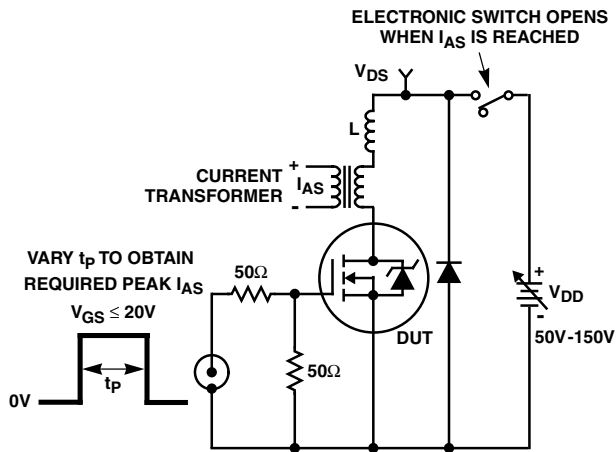


FIGURE 9. UNCLAMPED ENERGY TEST CIRCUIT

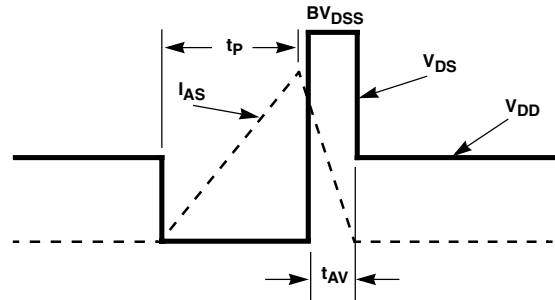


FIGURE 10. UNCLAMPED ENERGY WAVEFORMS

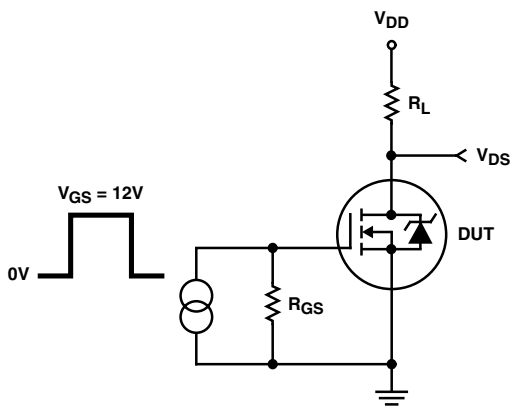


FIGURE 11. RESISTIVE SWITCHING TEST CIRCUIT

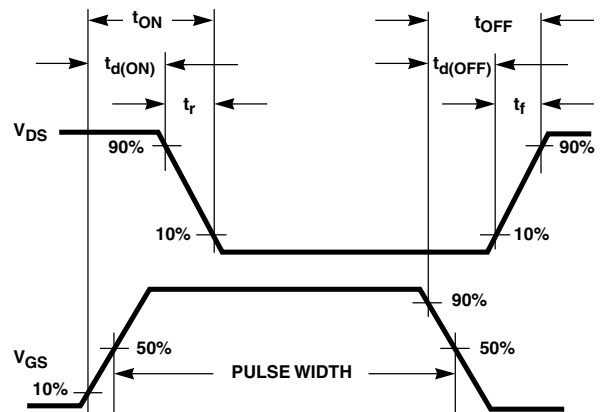


FIGURE 12. RESISTIVE SWITCHING WAVEFORMS

JANSR2N7430

Screening Information

Screening is performed in accordance with the latest revision in effect of MIL-PRF-19500, (Screening Information Table).

Delta Tests and Limits (JANS) $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MAX	UNITS
Gate to Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20\text{V}$	± 20 (Note 7)	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 80\%$ Rated Value	± 25 (Note 7)	μA
Drain to Source On Resistance	$r_{DS(ON)}$	$T_C = 125^\circ\text{C}$ at Rated I_D	$\pm 20\%$ (Note 8)	Ω
Gate Threshold Voltage	$V_{GS(TH)}$	$I_D = 1.0\text{mA}$	$\pm 20\%$ (Note 8)	V

NOTES:

7. Or 100% of Initial Reading (whichever is greater).

8. Of Initial Reading.

Screening Information

TEST	JANS
Unclamped Inductive Switching	$V_{GS(PEAK)} = 15\text{V}$, $L = 0.1\text{mH}$; Limit = 200A
Thermal Response	$t_H = 100\text{ms}$; $V_H = 25\text{V}$; $I_H = 4\text{A}$; Limit = 120mV
Gate Stress	$V_{GS} = 30\text{V}$, $t = 250\mu\text{s}$
Pind	Required
Pre Burn-In Tests (Note 9)	MIL-PRF-19500 Group A, Subgroup 2 (All Static Tests at 25°C)
Steady State Gate Bias (Gate Stress)	MIL-PRF-750, Method 1042, Condition B $V_{GS} = 80\%$ of Rated Value, $T_A = 150^\circ\text{C}$, Time = 48 hours
Interim Electrical Tests (Note 9)	All Delta Parameters Listed in the Delta Tests and Limits Table
Steady State Reverse Bias (Drain Stress)	MIL-PRF-750, Method 1042, Condition A $V_{DS} = 80\%$ of Rated Value, $T_A = 150^\circ\text{C}$, Time = 240 hours
PDA	5%
Final Electrical Tests (Note 9)	MIL-PRF-19500, Group A, Subgroups 2 and 3

NOTE:

9. Test limits are identical pre and post burn-in.

Additional Screening Tests

PARAMETER	SYMBOL	TEST CONDITIONS	MAX	UNITS
Safe Operating Area	SOA	$V_{DS} = 48\text{V}$, $t = 10\text{ms}$	11	A
Thermal Impedance	ΔV_{SD}	$t_H = 500\text{ms}$; $V_H = 25\text{V}$; $I_H = 4\text{A}$	200	mV

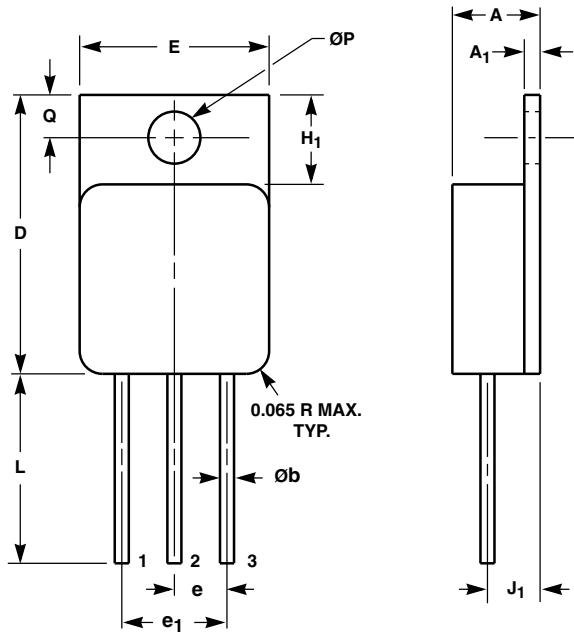
Rad Hard Data Packages - Intersil Power Transistors

1. JANS Rad Hard - Standard Data Package

- A. Certificate of Compliance
- B. Serialization Records
- C. Assembly Flow Chart
- D. SEM Photos and Report
- E. Preconditioning
 - Attributes Data Sheet
 - HTRB - Hi Temp Gate Stress Post Reverse Bias Data and Delta Data
 - HTRB - Hi Temp Drain Stress Post Reverse Bias Delta Data
- F. Group A
 - Attributes Data Sheet
- G. Group B
 - Attributes Data Sheet
- H. Group C
 - Attributes Data Sheet
- I. Group D
 - Attributes Data Sheet

2. JANS Rad Hard - Optional Data Package

- A. Certificate of Compliance
- B. Serialization Records
- C. Assembly Flow Chart
- D. SEM Photos and Report
- E. Preconditioning
 - Attributes Data Sheet
 - HTRB - Hi Temp Gate Stress Post Reverse Bias Data and Delta Data
 - HTRB - Hi Temp Drain Stress Post Reverse Bias Delta Data
 - X-Ray and X-Ray Report
- F. Group A
 - Attributes Data Sheet
 - Subgroups A2, A3, A4, A5 and A7 Data
- G. Group B
 - Attributes Data Sheet
 - Subgroups B1, B3, B4, B5 and B6 Data
- H. Group C
 - Attributes Data Sheet
 - Subgroups C1, C2, C3 and C6 Data
- I. Group D
 - Attributes Data Sheet
 - Pre and Post Radiation Data

TO-254AA**3 LEAD JEDEC TO-254AA HERMETIC METAL PACKAGE**

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.249	0.260	6.33	6.60	-
A ₁	0.040	0.050	1.02	1.27	-
Øb	0.035	0.045	0.89	1.14	2, 3
D	0.790	0.800	20.07	20.32	-
E	0.535	0.545	13.59	13.84	-
e	0.150 TYP		3.81 TYP		4
e ₁	0.300 BSC		7.62 BSC		4
H ₁	0.245	0.265	6.23	6.73	-
J ₁	0.140	0.160	3.56	4.06	4
L	0.520	0.560	13.21	14.22	-
ØP	0.139	0.149	3.54	3.78	-
Q	0.110	0.130	2.80	3.30	-

NOTES:

1. These dimensions are within allowable dimensions of Rev. A of JEDEC outline TO-254AA dated 11-86.
2. Add typically 0.002 inches (0.05mm) for solder coating.
3. Lead dimension (without solder).
4. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
5. Die to base BeO isolated, terminals to case ceramic isolated.
6. Controlling dimension: Inch.
7. Revision 1 dated 1-93.

WARNING!**BERYLLIA WARNING PER MIL-PRF-19500**

Packages containing beryllium oxide (BeO) shall not be ground, machined, sandblasted, or subject to any mechanical operation which will produce dust containing any beryllium compound. Packages containing any beryllium compound shall not be subjected to any chemical process (etching, etc.) which will produce fumes containing beryllium or its' compounds.

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DenseTrench TM	HiSeC TM	QS TM	TinyLogic TM
DOMET TM	ISOPLANAR TM	QT Optoelectronics TM	UHC TM
EcoSPARK TM	LittleFET TM	Quiet Series TM	UltraFET [®]
E ² CMOS TM	MicroFET TM	SILENT SWITCHER [®]	VCX TM
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FACT TM	OPTOLOGIC TM	Star [*] Power TM	
FACT Quiet Series TM	OPTOPLANAR TM	Stealth TM	

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.