J72V201…. 256 x 9 Bits
J72V211…. 512 x 9 Bits
J72V221…. 1024 x 9 Bits
J72V231…. 2048 x 9 Bits
J72V241…. 4096 x 9 Bits
J72V251…. 8192 x 9 Bits

VeloSync™ High Performance 9-Bit 3.3V Synchronous FIFO *Data Sheet*

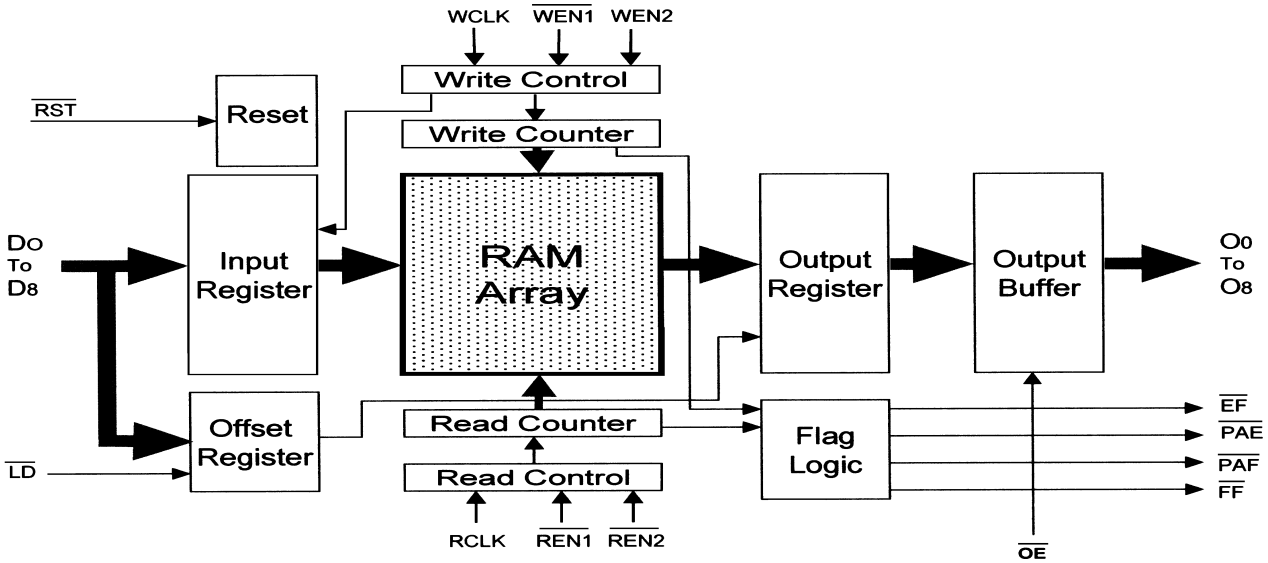
Features:

- Advanced 0.25 Micron CMOS Technology
- Very High Performance – 133 MHz Max Clock Rate
- 7.5 ns Read/Write Cycle Times
- 5 Volt Tolerant Inputs
- Low Power Requirements
- Separate and Independent Read / Write Clocking
- FIFO Empty and FIFO Full Status Flags
- 3.3 V Operation, 5V Tolerant Device Inputs
- Dual Ported For Zero Fall-Through Timing
- High Performance, Lower-Power Replacement For Industry Standard FIFOs (See page 15)
- Almost-Empty and Almost-Full Flags are Programmable, With Default To Empty +7, and Full -7
- Output Enable for 3-State Mode Control of Data Bus
- Packages - 32-Pin Plastic Thin Quad Flat Pack (TQFP) and 32-Pin Plastic Leaded Chip Carrier (PLCC)
- Meets Commercial Temperature (0°C to +70°C) and Industrial Temperature (-40°C to +85°C.)

Device Description:

JSI's VeloSync™ Series very high-performance, low power synchronous First-In/First-Out (FIFO) buffer memories are pin and function compatible with currently available industry standard FIFOs for most applications. Independently clocked read and write controls provide maximum operational flexibility, with synchronous read and write clocking providing easy system design. These FIFOs offer much higher performance, while requiring lower power and increased timing margins when utilized at clock rates less than 133 MHz, They are offered in 256, 512, 1,024, 2,048, 4,096 and 8,192 x 9-bit wide organizations to match a variety of data buffering requirements. JSI's FIFOs are a cost effective solution to provide elastic data buffering for data communications, multi-processing, networking, video, and graphics applications. Their input port is controlled by WCLK, a free-running clock, plus WEN1 and WEN2/LD Write Enable pins. Each rising edge of the clock writes data into the FIFO when the write enable pins are active. RCLK and two Read Enable pins REN1, REN2 control reading the FIFO in the same manner. Both the Read Clock and the Write Clock can be tied together for single clock operation or each clock can be utilized asynchronously for dual, separate clock operation. OE Provides control of the read output 3-state buffer for use in direct bus applications.

For maximum flexibility and ease of use, these FIFOs offer two programmable flags to indicate Almost Full and Almost Empty as well as the standard Full and Empty flags. The programmable flags are organized to automatically default to Empty +7, and Full -7, and can be easily modified via activation of the WEN2/LD signal.



Maximum Ratings:

Symbol	Rating	Unit	Range
I_{out}	Output Current (DC)	mA	-50 to +50
V_{input}	Terminal Voltage vs. GND	V	-0.5 to +5
T_{store}	Storage Temperature	°C	-55 to +125

Note:

Exceeding maximum stress ratings may possibly cause permanent damage to the device. The device is designed to operate only within the conditions specified for normal operation, and should never be operated beyond those normal operating limits. Reliability may be compromised if the device is exposed to absolute maximum rating conditions for extended periods of time.

Recommended Operating Conditions:

Symbol	Parameter	Unit	Min.	Max.
Vil	Input Low Voltage	V	--	0.8
Vih	Input High Voltage	V	2.0	5.0
To	Operating Temperature	°C	-40	+85
Vcc	Supply Voltage	V	3.0	3.6
GND	Ground Reference Voltage	V	0	0

DC Electrical Characteristics:

Commercial Temperature Range (0°C to + 70°C) with Vcc of +3.0V to +3.6V. RCLK and WCLK may either be static or running.

Parameter	Symbol	Unit	Min	Max
Output Leakage Current (All Outputs)	I_{out}	µA	-10	10
Input Leakage Current (All Inputs)	I_{in} (1)	µA	-1	1
Power Supply Current (Active)	I_{cc} (2,3)	mA	-	20
Stand-By Current	I_{ccx}	mA	-	5
Voh (Output Voltage High) Ioh=-2mA	V_{oh}	V	2.4	-
Vol (Output Voltage Low) Iol=8mA	V_{ol}	V	-	0.4

NOTES:

1. Measured with a voltage input range of +0.4V to Vcc.
2. Data inputs are switched at 10 MHz with WCLK and RCLK running at 20 MHz.
3. Outputs are disabled during test.
4. All Inputs = GND + 0.2V or Vcc – 0.2V . WCLK and RCLK, are running at 20 MHz.

Input/Output Capacitance: (Clock Frequency = 2.0 MHz, Ambient Temperature = +25°C)

Symbol	Parameter	Unit	Conditions	Max.
C_i (2)	Input Capacitance	pF	Vin = 0V	10
C_o (1,2)	Output Capacitance	pF	Vout = 0V	10

NOTES:

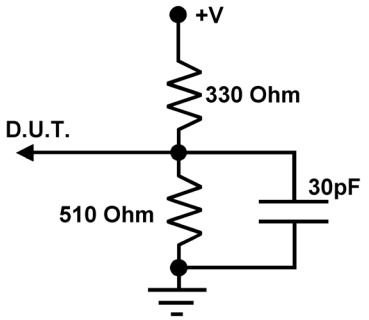
1. With output set to 3-state high impedance ($\overline{OE} \geq Vih$).
2. Not currently tested specifications (characterized only).

Pin Functions and Description:

Pin	Symbol	I/O	Description
Power	Vcc	N/A	Positive power supply pin (+3.3 Volts)
Ground	GND	N/A	Ground pin (Zero Volts)
Data Input Pins	D0… D8	Input	Input data (9 bits wide)
Reset	$\overline{RST}$	Input	Device general reset is required before initial writes. Low activation of this signal causes the internal read and write pointers to be reset to the first location of the RAM array, $\overline{FF}$ and $\overline{PAF}$ go HIGH, and $\overline{PAE}$ and $\overline{EF}$ go low.
Write Enable 1	$\overline{WEN1}$	Input	$\overline{WEN1}$ becomes the only Write Enable pin if the FIFO is setup to have programmable Flags. If the FIFO is setup to operate with two write enable pins, $\overline{WEN1}$ must be set low, and WEN2/$\overline{LD}$ set high to write in data. When $\overline{WEN1}$ is LOW, data is written into the FIFO on every LOW to-HIGH transition WCLK. IF $\overline{FF}$ is Low, data cannot be written into the FIFO.
Write Enable 2 / Load	WEN2/$\overline{LD}$	Input	$\overline{RST}$ is used to program the FIFO to operate with either two write enables or programmable flags. If WEN2/$\overline{LD}$ is set high during activation of $\overline{RST}$, WEN2/$\overline{LD}$ will operate as a second write enable. If it is held low during $\overline{RST}$, it becomes a control pin used to input and read the programmable flag offsets. $\overline{WEN1}$ must be LOW, and WEN2/$\overline{LD}$ must be HIGH to write data into the FIFO If the FIFO is setup to have two write enables. $\overline{FF}$ must also be low to write data into the FIFO. If the FIFO is setup to operate with programmable flags, then WEN2/$\overline{LD}$ must be LOW to read or write programmable flag offsets.
Write Clock	WCLK	Input	Low to high transitions of WCLK Writes data into the FIFO if the Write Enable(s) are set to their active state.
Data Outputs	O0… O8	Output	Output Data (9 bits wide)
Read Clock	RCLK	Input	The rising edge of this clock causes data to be read from the FIFO when $\overline{REN1}$ and $\overline{REN2}$ are low.
Read Enable 1	$\overline{REN1}$	Input	Data is read from the FIFO on every LOW-to-HIGH transition of RCLK whenever $\overline{REN1}$ and $\overline{REN2}$ are in their active state (low). If the $\overline{EF}$ flag is low, the FIFO is empty, and no data will be read.
Read Enable 2	$\overline{REN2}$	Input	Data is read from the FIFO on every LOW-to-HIGH transition of RCLK whenever $\overline{REN1}$ and $\overline{REN2}$ are in their active state (low). If the $\overline{EF}$ flag is low, the FIFO is empty, and no data will be read.
Output Enable	$\overline{OE}$	Input	The data output bus is active whenever $\overline{OE}$ is Low, the output data bus is in a high-impedance state whenever $\overline{OE}$ is high.
Empty Flag	$\overline{EF}$	Output	When the $\overline{EF}$ pin goes low, there is no data in the FIFO, and further data reads from the FIFO are blocked. When $\overline{EF}$ is HIGH, the FIFO contains data and reads are allowed. EF and RCLK are synchronous.
Programmable Almost-Empty Flag	$\overline{PAE}$	Output	This signal indicates when the FIFO is almost empty, and is based upon the offset previously loaded into the FIFO. When $\overline{PAE}$ is low, it indicates that the FIFO is almost-empty. $\overline{RST}$ sets its default value to “EMPTY +7”. $\overline{PAE}$ and RCLK are synchronous. The data for the PAE offset must only be loaded immediately after reset. If it is loaded with data in the FIFO, PAE may activate erroneously.
Programmable Almost-Full Flag	$\overline{PAF}$	Output	This signal indicates when the FIFO is almost full, and is based upon the offset previously loaded into the FIFO. When $\overline{PAF}$ is low, it indicates that the FIFO is almost-full. $\overline{RST}$ sets its default value to “FULL -7”. $\overline{PAF}$ and WCLK are synchronous. The data for the PAF offset must only be loaded immediately after reset. If it is loaded with data in the FIFO, PAF may activate erroneously.
Full Flag	$\overline{FF}$	Output	When low, This signal indicates when the FIFO is full, This also blocks any further data writes into FIFO. When it is High, there is room in the FIFO and more data can be written into the FIFO. $\overline{FF}$ and WCLK are synchronous.

AC Test Conditions:

Input Levels	GND to +3.0V
Input Rise/Fall Times	1 ns
Input Reference Levels	1.5 V
Output Reference Levels	1.5 V
Output Load	See Diagram



Equivalent Test Load Circuit

AC Electrical Characteristics: (VCC = +3.0V to +3.6V, Temperature = 0°C to + 70°C)

Symbol	Parameter	J72VxxxL7.5		J72VxxxL10		J72VxxxL15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
fcy	Clock Cycle Frequency	--	133	--	100	--	66.7	MHz
tacc	Data Access Time	1.5	4.5	2	6.5	2	10	ns
tclk	Read/Write Clock Cycle Time	7.5	--	10	--	15	--	ns
tclkh	Read/Write Clock High Time	3.4	--	4.5	--	6.0	--	ns
tclkl	Read/Write Clock Low Time	3.4	--	4.5	--	6.0	--	ns
tis	Data Set-up Time for Input	3.0	--	3.0	--	4.0	--	ns
tih	Data Hold Time for Input	0.5	--	1	--	1	--	ns
tes	Set-up Time for Enable	3.0	--	3.0	--	4.0	--	ns
teh	Hold Time for Enable	0.5	--	1	--	1	--	ns
trpw	Pulse Width of RST	7.5	--	10	--	15	--	ns
trsts	Set-up Time from RST	6.5	--	8	--	10	--	ns
trstr	Recovery Time from RST	6.5	--	8	--	10	--	ns
trfo	Time from Reset to Flag and Outputs	--	4.4	--	10	--	15	ns
toel	Output Enable to Output in Low-Z[(2)]	0	--	0	--	0	--	ns
tov	Output Enable to Output Valid	2.75	--	3	--	3	8	ns
toeh	Output Enable to Output in High-Z[(2)]	2.75	--	3	--	3	8	ns
twf	Write Clock to Full Flag delay	--	4.4	--	6.5	--	10	ns
tre	Read Clock to Empty Flag delay	--	4.4	--	6.5	--	10	ns
taff	Write Clock to Almost-Full Flag delay	--	4.4	--	6.5	--	10	ns
taef	Read Clock to Almost Empty Flag delay	--	4.4	--	6.5	--	10	ns
t_{SKEW1}	Read Clock & Write Clock skew time for Empty Flag & Full Flag	3.75	--	5	--	6	--	ns
t_{SKEW2}	Read Clock & Write Clock skew time for Almost-Empty Flag & Almost – Full Flag	10	--	14	--	18	--	ns

NOTES:

1. Minimum pulse widths must not be violated.
2. These values are not specifically tested, but are guaranteed by design.
3. Commercial only.

Signal Descriptions and Operation:

(DO …D8) Inputs:

(Data Inputs) - 9 Bit wide data inputs used for data to be written into the FIFO.

(WCLK) Write Clock

Write cycles are initiated on the LOW-to-HIGH transition (rising edge) of the Write Clock (WCLK). Data set-up and hold times must be met in respect to the LOW-to-HIGH transition of the Write Clock (WCLK). The Full Flag ($\overline{FF}$) and Programmable Almost-Full Flag ($\overline{PAF}$) are synchronized with respect to the LOW-to-HIGH transition of the Write Clock (WCLK). Write and Read clocks can be asynchronous or coincident.

($\overline{RST}$) Reset

When this signal is taken low, the FIFO resets, setting the read and write pointers to the first location. After power-up, a reset is required before a write operation can take place. After reset and t_{rfo}, the Full-Flag ($\overline{FF}$) and Programmable Almost-Full Flag ($\overline{PAF}$) will be reset to high and the Empty Flag ($\overline{EF}$) and Programmable Almost-Empty Flag ($\overline{PAE}$) will be reset to LOW. Reset initializes the offset registers to their default values and the output register to zero.

($\overline{WEN1}$) Write Enable 1

$\overline{WEN1}$ is the only Write Enable control pin used if the FIFO is configured to have programmable flags. When the FIFO is set for programmable flags, and when Write Enable 1 ($\overline{WEN1}$) is low… data can be written into the input register and RAM array on the rising edge of each Write Clock (WCLK). When Write Enable ($\overline{WEN1}$) is high… the previous data is held in the input register and no new data can be loaded into the register. Due to the dual-port design of the FIFO, read operations are unaffected by write operations.

When the FIFO is programmed to have two write enables (allowing for depth expansion), two enable control pins are available. Data overflow is prevented by the Full Flag ($\overline{FF}$) going LOW which blocks any additional write operations. After completing a valid read operation, the Full Flag ($\overline{FF}$) will go High after t_{wf}, allowing writes to occur. If the FIFO is full $\overline{WEN1}$ is ignored.

(RCLK) Read Clock

The rising edge of RCLK allows data to be read on the outputs. Both the Empty Flag ($\overline{EF}$) and Programmable Almost-Empty Flag ($\overline{PAE}$) are synchronously activated with to the LOW-to-HIGH transition of the Read Clock (RCLK). Read Clocks and Write Clocks can be entirely independent due to the dual-port design of the FIFO.

($\overline{REN1}$, $\overline{REN2}$) Read Enables

If both ($\overline{REN1}$, $\overline{REN2}$) are LOW, data is read from the RAM array to the output register on the rising edge of RCLK. If either $\overline{REN1}$or $\overline{REN2}$) is HIGH, the previous data remains in the output register and no new data can be loaded in.

When all data has been read out of the FIFO, $\overline{EF}$ goes low inhibiting any further reads. As soon as a valid write operation occurs, $\overline{EF}$ goes HIGH, and reads can begin. When the FIFO is empty, REN1, $\overline{REN2}$ are ignored.

($\overline{OE}$) Output Enable

When $\overline{OE}$ is activated by being taken low, the output buffers go from a high-impedance state to the active state, placing the data in the output register onto the output buffers. When $\overline{OE}$ is high, the outputs are placed in a high-impedance state.

(WEN2/$\overline{LD}$) WRITE ENABLE 2/$\overline{LOAD}$

This pin provides two separate functions that are programmed upon reset. It can be setup to have programmable flags or two write enables to allow depth expansion.

1. If used as a 2nd write enable for expansion, WEN2/$\overline{LD}$ is set high at reset. The pin then functions as a second Write Enable for the FIFO. Data can be written into the FIFO on the rising edge of each Write Clock. Whenever $\overline{WEN1}$ is HIGH and/or WEN2/$\overline{LD}$ is LOW, the input register contains the previous data and no new data can be loaded. The Full Flag ($\overline{FF}$) prevents any additional write operations once the FIFO is full, preventing the possibility of any data overruns.
2. These FIFOs provide programmable flags if WEN2/$\overline{LD}$ is set low during Reset. Each FIFO has four 8-bit offset registers that can be either loaded or read. Data from the D inputs can then be written into the “Empty” Least Significant Offset register on the rising edge of WCLK. Data is written into the “Empty” Most Significant Offset register on the second rising edge of WCLK, into the “Full” Least Significant Offset register on the third rising edge, and into the ”Full” Most Significant Offset register on the fourth rising edge.

Writing of the offset registers must be done prior to writing data to the FIFO. When WEN2/$\overline{LD}$ is set low as well as $\overline{REN1}$ and $\overline{REN2}$, the offset registers can be read on the FIFO outputs. Data is read on the rising edge of RCLK. Reads and writes to offset registers should not be performed simultaneously.

LD	WEN 1	WCLK	Selection
0	0	Rising Edge	Empty Offset (LSB) Empty Offset (MSB) Full Offset (LSB) Full Offset (MSB)
0	1	Rising Edge	No Operation
1	0	Rising Edge	Write Into FIFO
1	1	Rising Edge	No Operation

Outputs:

($\overline{FF}$) FULL FLAG

When $\overline{FF}$ goes low , any further write operations are inhibited. If no reads occur after $\overline{RST}$, the Full Flag ($\overline{FF}$) will go low after the full quantity of writes allowed for each device in the family. $\overline{FF}$ is activated synchronous with the rising edge of the Write Clock (WCLK).

($\overline{EF}$) EMPTY FLAG

When $\overline{EF}$ goes low, any further read operations are inhibited. If no writes occur after $\overline{RST}$, the Empty Flag ($\overline{EF}$) will go low after all the data has been completely read out of the FIFO. $\overline{EF}$ is activated synchronous with the rising edge of the Read Clock (RCLK).

($\overline{PAF}$) PROGRAMMABLE ALMOST-FULL FLAG

$\overline{PAF}$ goes low when the FIFO is almost-full. If no reads are performed after $\overline{RST}$, the Programmable Almost-Full flag ($\overline{PAF}$) will go low after the total number of words of data for each member of the FIFO family is written in. An "Offset' can be defined by utilizing the "Full Offset" registers. If an offset not specified, the Programmable Almost-Full flag ($\overline{PAF}$) is automatically set to go low at full-7 words. $\overline{PAF}$ is synchronized to the rising edge of WCLK.

($\overline{PAE}$) PROGRAMMABLE ALMOST-EMPTY FLAG

$\overline{PAE}$ goes low when the FIFO is almost-empty at n+1 locations less than the write pointer. An "Offset" can be defined by utilizing the "Empty Offset" registers. If an offset is not specified, the Programmable Almost-Empty flag ($\overline{PAE}$) is automatically set to go low at empty-7 words. $\overline{PAE}$ is synchronized to the rising edge of RCLK.

DATA OUTPUTS (O_0-O_8)

O_0… O_8 (Data Outputs) 9-Bit wide Data Outputs used for data to be read from the FIFO.

Status Flags:

The following tables illustrate the state of the status flags for varying amounts of data in the FIFO.

J72V201	J72V211	J72V221	EF	PAE	FF	PAF
256	512	1024	H	H	L	L
(256-m) to 255	(512-m) to 511	(1024-m) to 1023	H	H	H	L
(n +1) to (256-(m+1))	(n +1) to (512-(m+1))	(n +1) to (1024-(m+1))	H	H	H	H
1 to n	1 to n	1 to n	H	L	H	H
0	0	0	L	L	H	H

J72V231	J72V241	J72V251	EF	PAE	FF	PAF
2048	4096	8192	H	H	L	L
(2048-m) to 2047	(4096-m) to 4095	(8192-m) to 8191	H	H	H	L
(n +1) to (2048-(m+1))	(n +1) to (4096-(m+1))	(n +1) to (8192-(m+1))	H	H	H	H
1 to n	1 to n	1 to n	H	L	H	H
0	0	0	L	L	H	H

Note:

1. m = PAF offset, n = PAE offset.

Offset Register Bit Assignment and Default Values:

The following chart indicates the bit assignments and default register values for these FIFOs. Each FIFO utilizes a different number of bits for programming the offset, and all the FIFOs automatically default to the same value upon reset ($\overline{RST}$). Please note that bit number 8 (the 9th bit) of the LSB Registers are not used for either Empty Offset, or Full Offset. Instead, The MSB Registers are loaded with values above 256 starting with bit 0.

J72V201-256 x 9-Bit

	Empty Offset (MSB)									Empty Offset (LSB)								
Register Bits	8	7	6	5	4	3	2	1	0	8	7	6	5	4	3	2	1	0
Offset Bits	x	x	x	x	x	x	x	x	x	x	7	6	5	4	3	2	1	0
Default Value										0	0	7	H					

	Full Offset (MSB)									Full Offset (LSB)								
Register Bits	8	7	6	5	4	3	2	1	0	8	7	6	5	4	3	2	1	0
Offset Bits	x	x	x	x	x	x	x	x	x	x	7	6	5	4	3	2	1	0
Default Value										0	0	7	H					

J72V211- 512 x 9-Bit

	Empty Offset (MSB)									Empty Offset (LSB)								
Register Bits	8	7	6	5	4	3	2	1	0	8	7	6	5	4	3	2	1	0
Offset Bits	x	x	x	x	x	x	x	x	8	x	7	6	5	4	3	2	1	0
Default Value										0	0	7	H					

	Full Offset (MSB)									Full Offset (LSB)								
Register Bits	8	7	6	5	4	3	2	1	0	8	7	6	5	4	3	2	1	0
Offset Bits	x	x	x	x	x	x	x	x	8	x	7	6	5	4	3	2	1	0
Default Value										0	0	7	H					

J72V221-1,024 x 9-Bit

	Empty Offset (MSB)									Empty Offset (LSB)								
Register Bits	8	7	6	5	4	3	2	1	0	8	7	6	5	4	3	2	1	0
Offset Bits	x	x	x	x	x	x	x	9	8	x	7	6	5	4	3	2	1	0
Default Value										0	0	7	H					

	Full Offset (MSB)									Full Offset (LSB)								
Register Bits	8	7	6	5	4	3	2	1	0	8	7	6	5	4	3	2	1	0
Offset Bits	x	x	x	x	x	x	x	9	8	x	7	6	5	4	3	2	1	0
Default Value										0	0	7	H					

J72V231-2,048 x 9-Bit

	Empty Offset (MSB)									Empty Offset (LSB)								
Register Bits	8	7	6	5	4	3	2	1	0	8	7	6	5	4	3	2	1	0
Offset Bits	x	x	x	x	x	x	10	9	8	x	7	6	5	4	3	2	1	0
Default Value										0	0	7	H					

	Full Offset (MSB)									Full Offset (LSB)								
Register Bits	8	7	6	5	4	3	2	1	0	8	7	6	5	4	3	2	1	0
Offset Bits	x	x	x	x	x	x	10	9	8	x	7	6	5	4	3	2	1	0
Default Value										0	0	7	H					

J72V241- 4,096 x 9-Bit

	Empty Offset (MSB)									Empty Offset (LSB)								
Register Bits	8	7	6	5	4	3	2	1	0	8	7	6	5	4	3	2	1	0
Offset Bits	x	x	x	x	x	11	10	9	8	x	7	6	5	4	3	2	1	0
Default Value										0	0	7	H					

	Full Offset (MSB)									Full Offset (LSB)								
Register Bits	8	7	6	5	4	3	2	1	0	8	7	6	5	4	3	2	1	0
Offset Bits	x	x	x	x	x	11	10	9	8	x	7	6	5	4	3	2	1	0
Default Value										0	0	7	H					

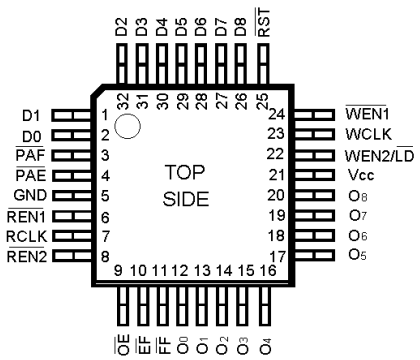
J72V251- 8,192 x 9-Bit

	Empty Offset (MSB)									Empty Offset (LSB)								
Register Bits	8	7	6	5	4	3	2	1	0	8	7	6	5	4	3	2	1	0
Offset Bits	x	x	x	x	12	11	10	9	8	x	7	6	5	4	3	2	1	0
Default Value										0	0	7	H					

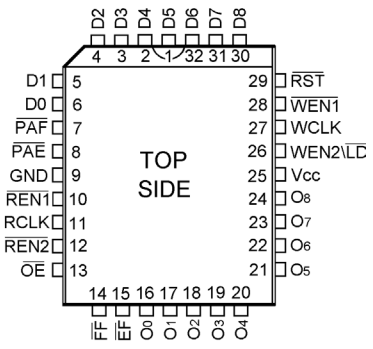
	Full Offset (MSB)									Full Offset (LSB)								
Register Bits	8	7	6	5	4	3	2	1	0	8	7	6	5	4	3	2	1	0
Offset Bits	x	x	x	x	12	11	10	9	8	x	7	6	5	4	3	2	1	0
Default Value										0	0	7	H					

Device Pin-outs:

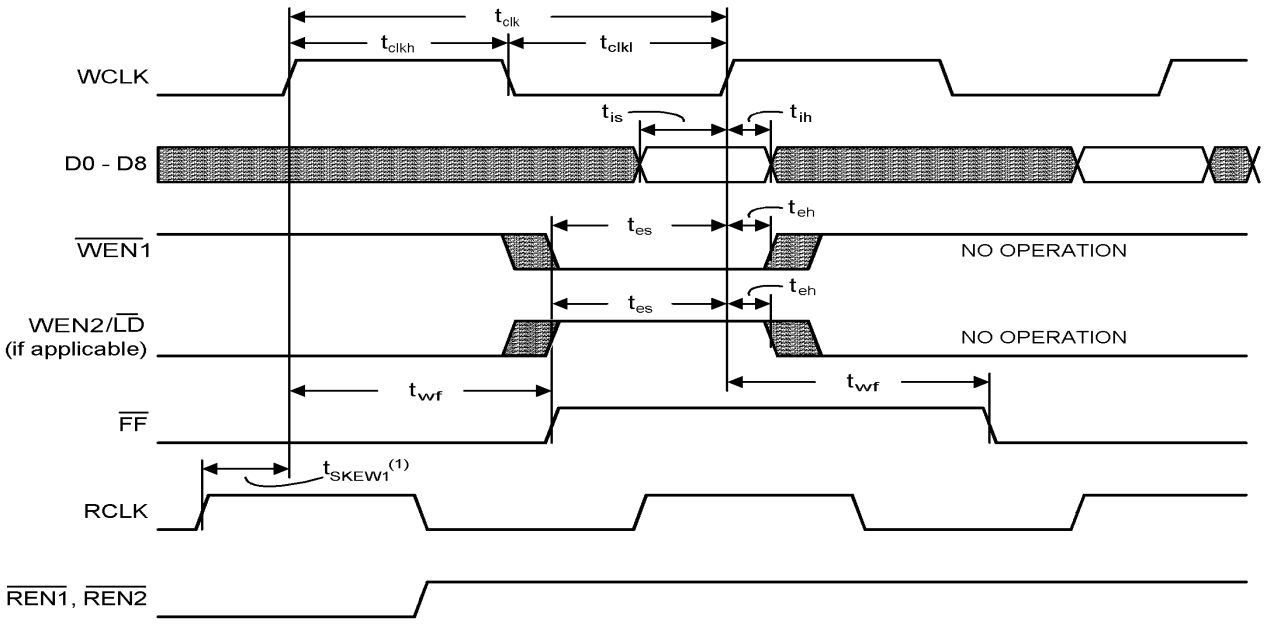
TQFP



PLCC

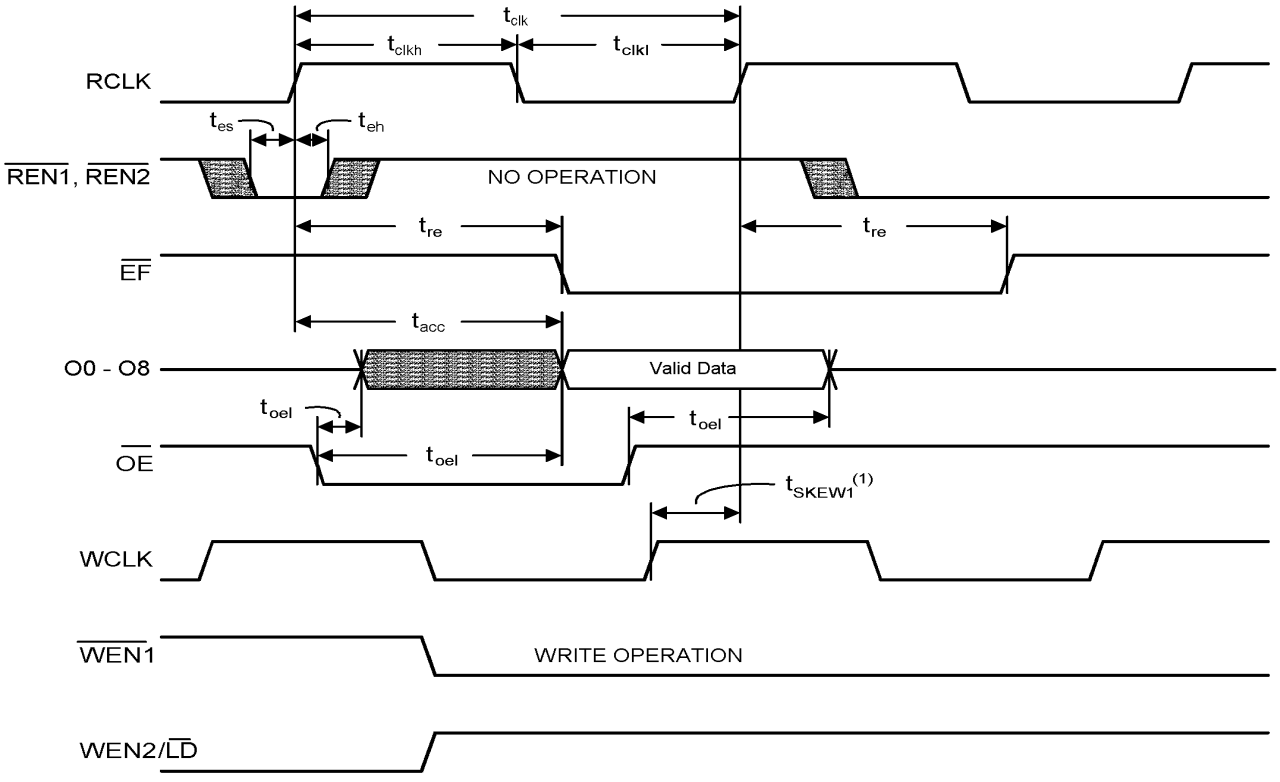


Write Timing:



Note:
1. T_{SKEW1} indicates the minimum time between the rising edge of RCLK and the rising edge of WCLK for $\overline{FF}$ to change during the current clock cycle. $\overline{FF}$ may not change until the next WCLK if the time between the rising edge of RCLK and WCLK is less than T_{SKEW1}.

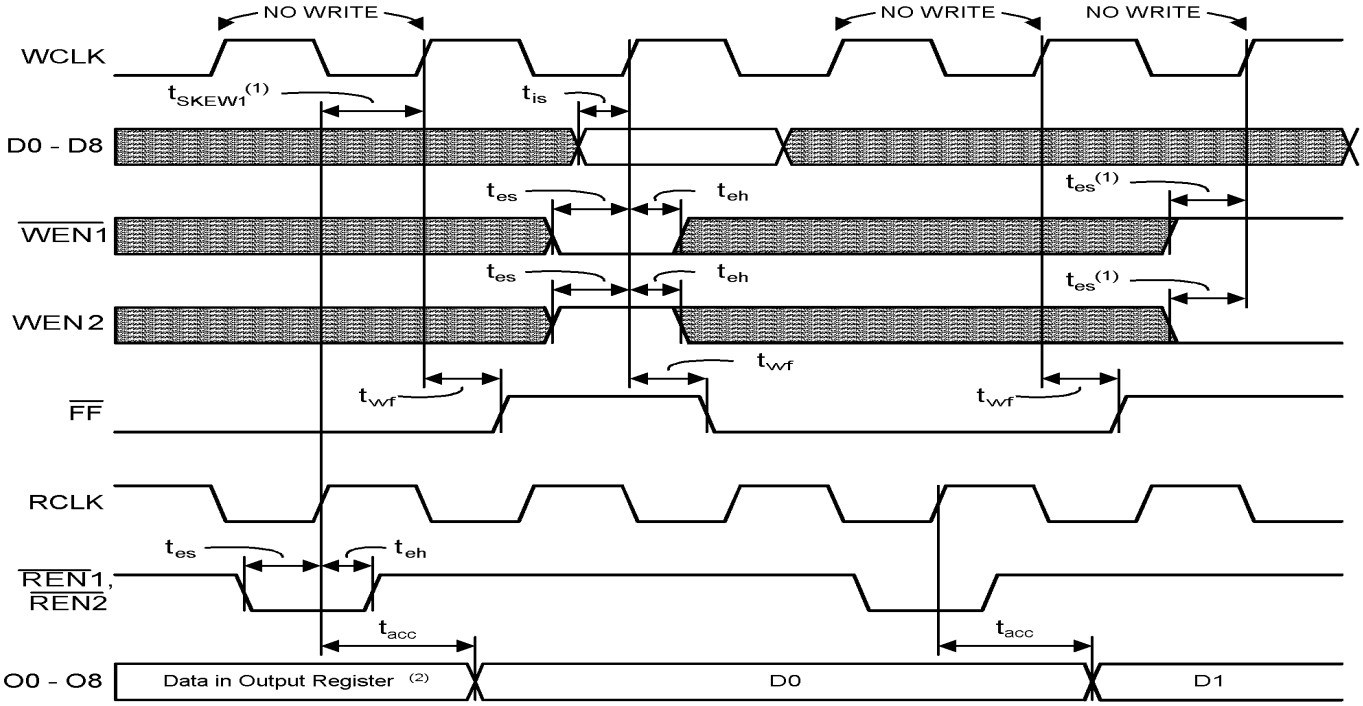
Read Timing:



Note:

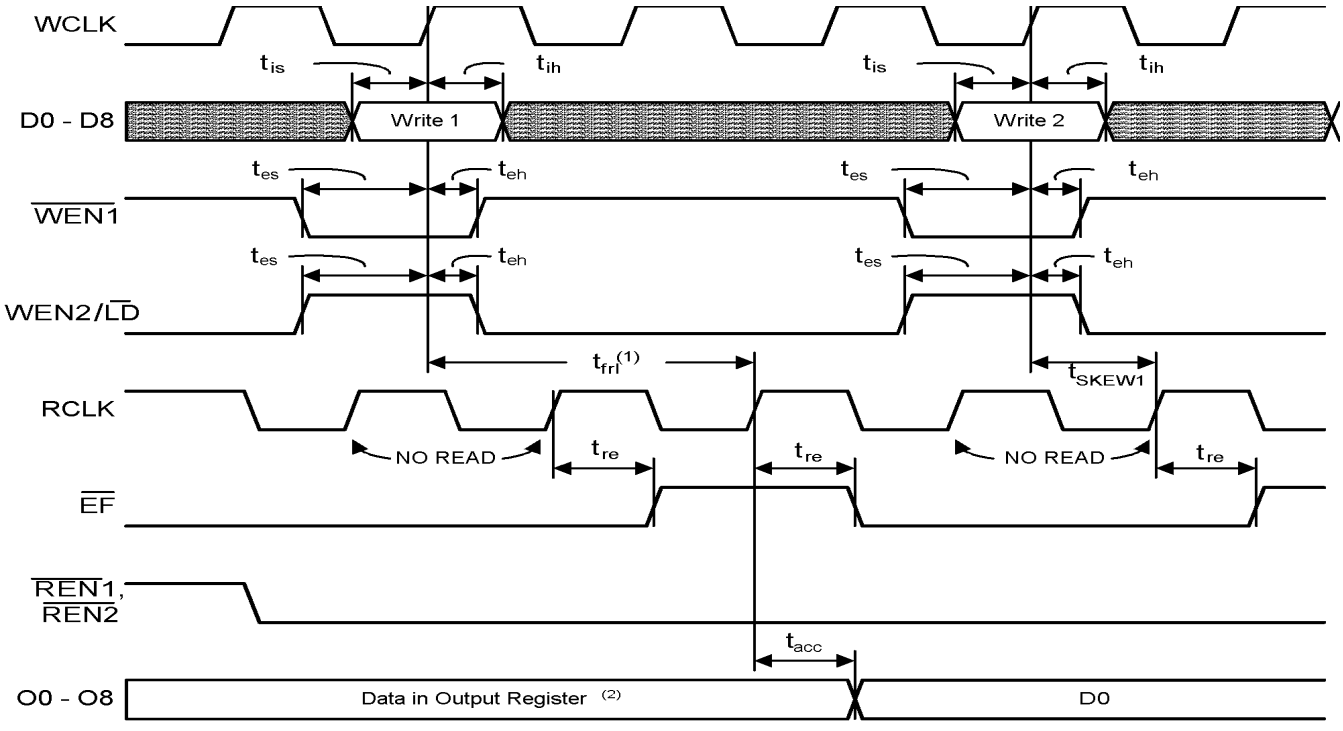
2. T_{SKEW1} indicates the minimum time between the rising edge of WCLK and the rising edge of RCLK for $\overline{EF}$ to change during the current clock cycle. $\overline{EF}$ may not change until the next RCLK if the time between The rising edge of WCLK and RCLK is less than T_{SKEW1}.

Full Flag Timing ($\overline{OE}$ is Low):



Note:
1. Either WEN1 needs to go high, or WEN2 needs to go low to prevent writes to the FIFO.

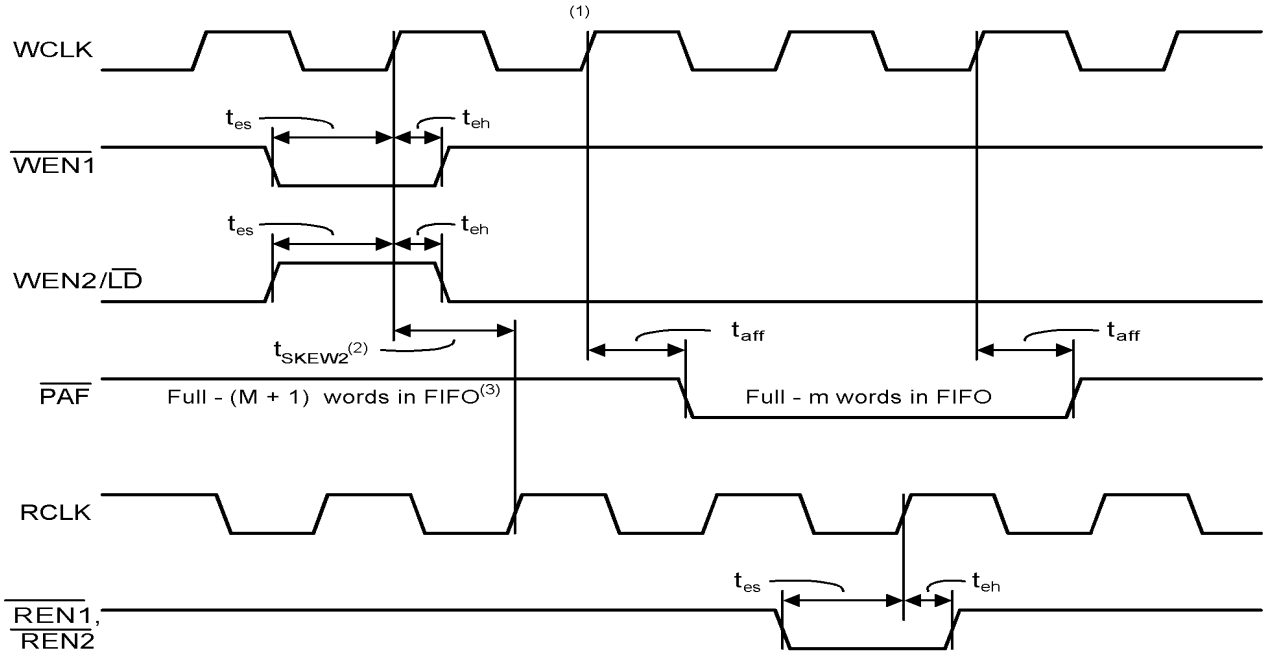
Empty Flag Timing ($\overline{OE}$ is Low):



Notes:

1. When T_{SKEW1} is greater than or equal to the minimum specification, t_{frl} maximum equals t_{clk} plus T_{SKEW1}.
2. When T_{SKEW1} is less than minimum specification, t_{rfl} maximum equals 2t_{clk} plus T_{SKEW1} or t_{clk} plus T_{SKEW1}.

Programmable Full Flag Timing:



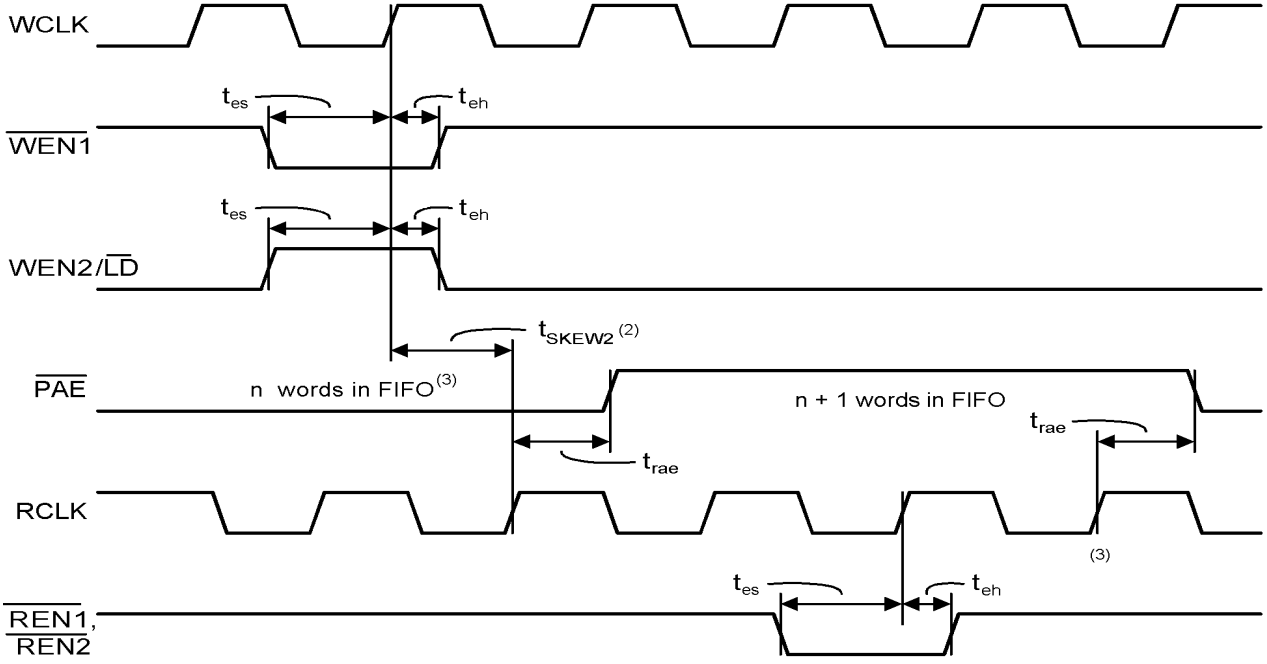
Notes:

1 If data is written into the FIFO on the rising edge of WCLK; when $\overline{PAF}$ goes low there will be (m-1) words in the FIFO.

2 The minimum time between the rising edge of RCLK and the rising edge of WCLK for $\overline{PAF}$ to change during the current cycle is defined by T_{SKEW2}. $\overline{PAF}$ may not change state until the next rising edge of WCLK if the minimum T_{SKEW2} time is not met.

3. n = $\overline{PAF}$ offset.

Programmable Empty Flag Timing:



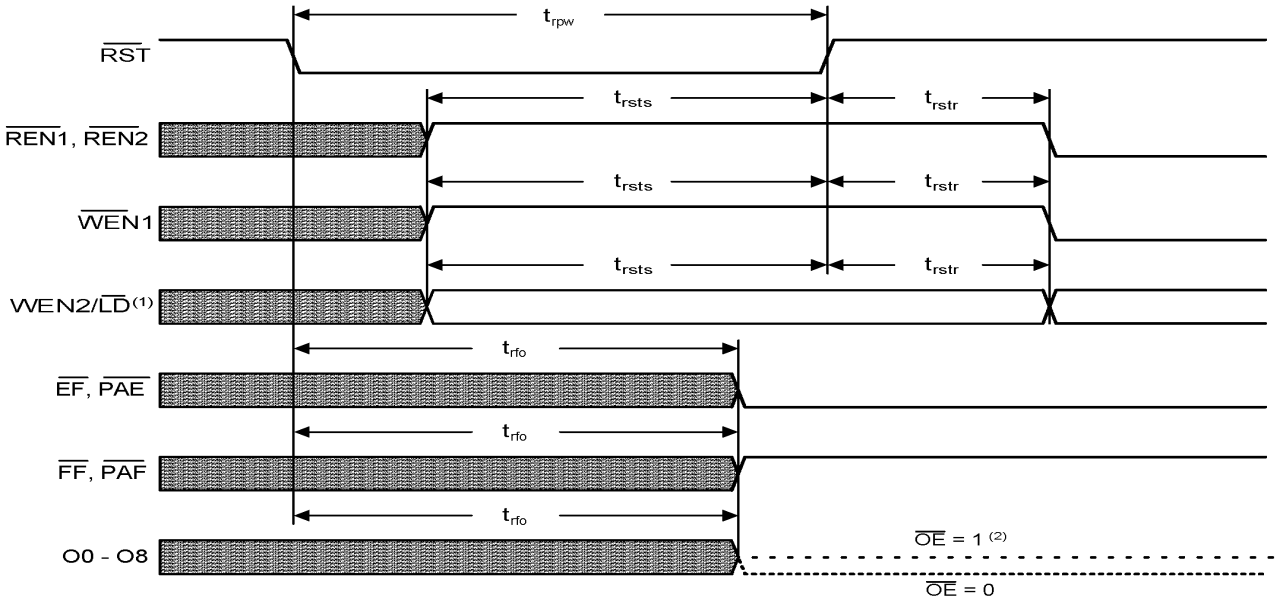
Notes:

1. If data is read from the FIFO on the rising edge of RCLK; when $\overline{PAE}$ goes low there will be empty + (n-1) words in the FIFO.

2. The minimum time between the rising edge of WCLK and the rising edge of RCLK for $\overline{PAE}$ to change during the current cycle is defined by T_{SKEW2}. $\overline{PAE}$ may not change state until the next rising edge of RCLK if the minimum T_{SKEW2} time is not met.

3.. n = $\overline{PAE}$ offset.

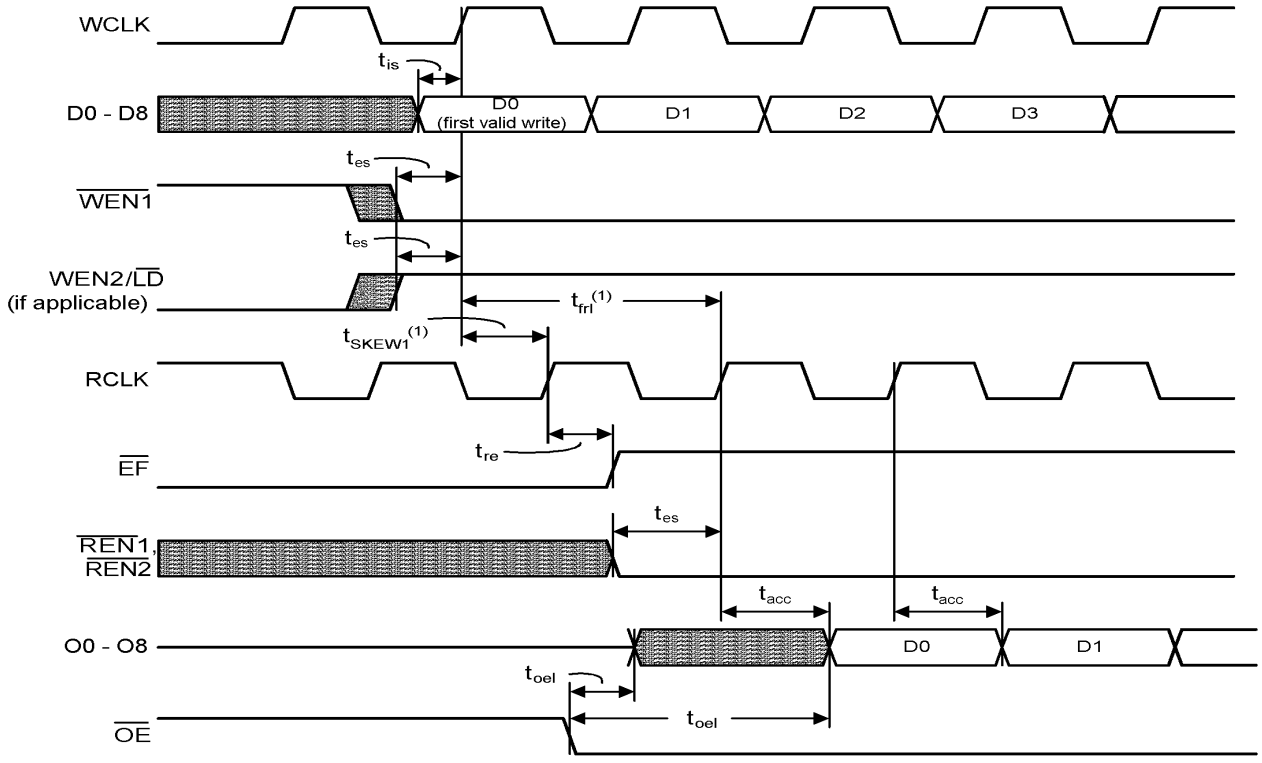
Reset Timing:



Notes:

1. If WEN2/$\overline{LD}$ is held high during reset, it will become a second Write Enable pin. If held low during reset, it becomes a load enable for the Programmable Flag Offset registers.
2. Upon device reset, all the outputs will be low if $\overline{OE}$ equals 0 and in 3-state high impedance if $\overline{OE}$ equals a 1.
3. WCLK and RCLK can both be running during reset (not shown in this diagram).

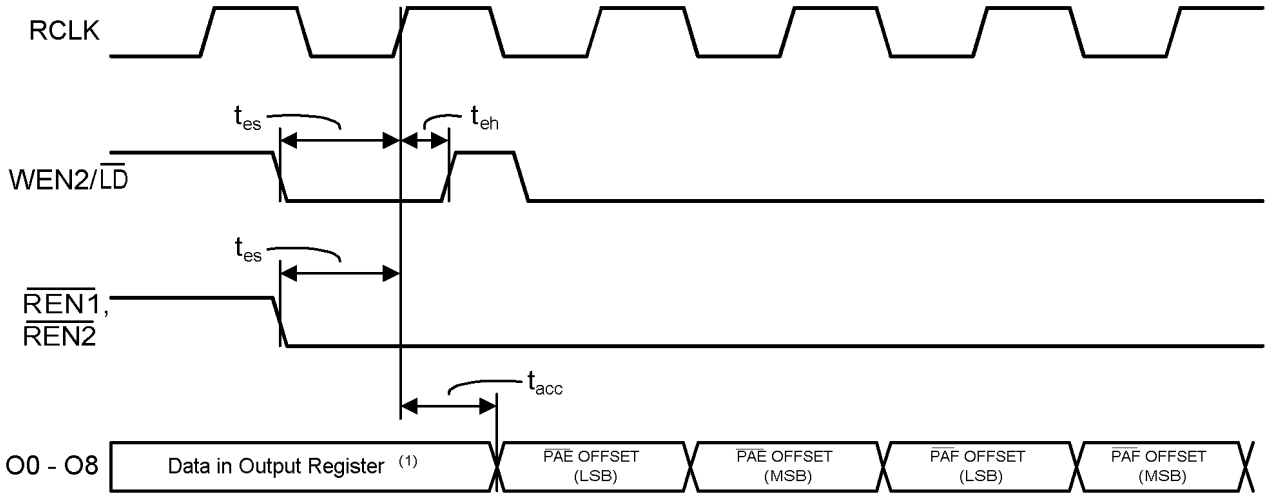
1st Data Word Latency:



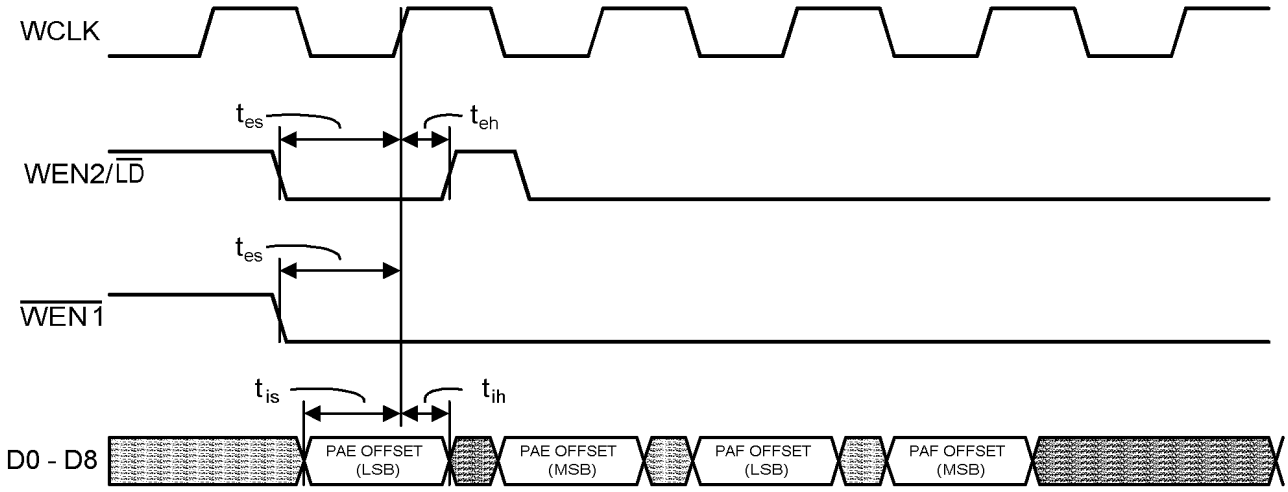
Notes:

1. $t_{frl} = t_{clk} + T_{SKEW1}$ when T_{SKEW1} is less than or equal to its minimum specification.
2. $t_{frl} = 2_{tclk} + T_{SKEW1}$ or $t_{clk} + T_{SKEW1}$ if T_{SKEW1} is greater than its minimum specification.
3. These delay timings only apply when $\overline{EF}$ is LOW.

Read Offset Register Timing:



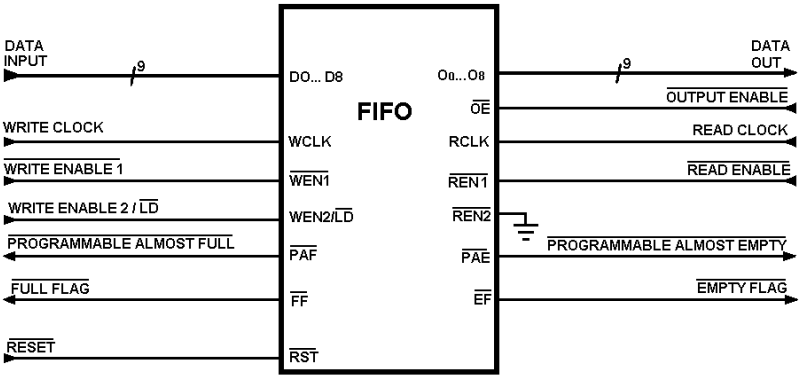
Write Offset Register Timing:



FIFO Applications and Operation:

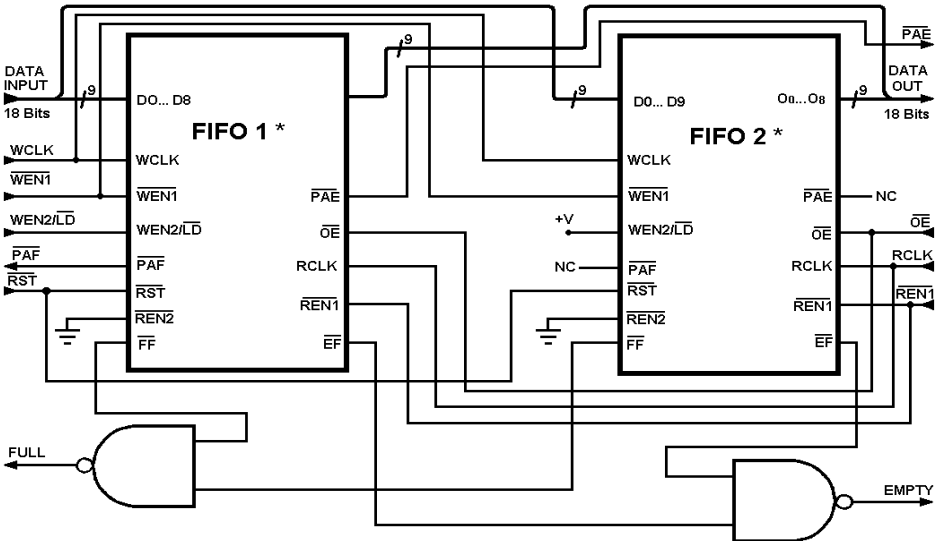
JSI VeloSync FIFOs offer a high degree of design flexibility for various configurations. They can be utilized as a single device, connected in parallel for wider bus applications, or can be organized for deeper FIFO applications.

Single Device Configuration:



Read Enable 2 ($\overline{REN2}$) is grounded since it is not required for single device operation.

Multiple Device Width (Parallel) Configuration:



*Similar FIFO sizes must be used. Any size of JSI VeloSync FIFO will operate in this manner.

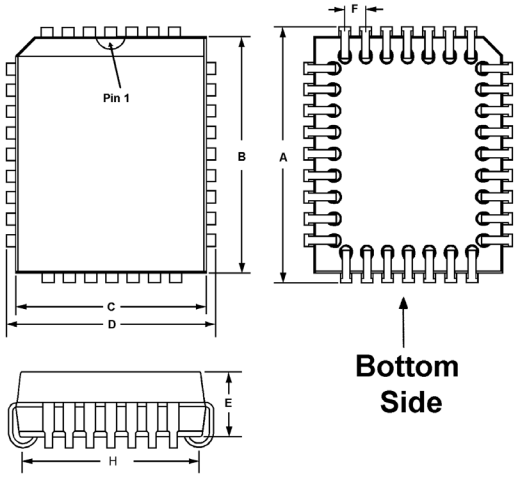
These FIFOs can be easily expanded to support wider word widths by connecting the control inputs of multiple devices in the manner shown above. The Full Flag ($\overline{FF}$) and Empty Flag ($\overline{EF}$) of each device must combined via an OR gate to create a Full and Empty flag that indicates the combined status of each FIFO's Full and Empty Flag. In this configuration, Read Enable 2 ($\overline{REN2}$) is tied to ground because it is not specifically needed to control the FIFOs, and WEN2/$\overline{LD}$ is held low during reset so that it becomes the load pin for the programmable flag offsets.

Multiple Device Depth Configuration:

JSI's FIFOs can be easily utilized in a series configuration to allow depth expansion. To accomplish this external logic for both the read and write control is required to alternately address each device for both read operations and write operations.

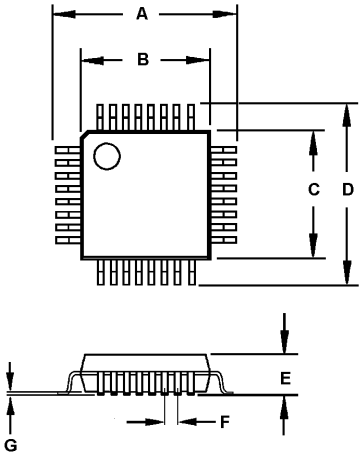
The Write Enable 2 / Load pin (WEN2/$\overline{LD}$) should be held high during reset ($\overline{RST}$) to set it up as second write enable pin. This causes the programmable flags remain at their default values (unchanged). WEN2/$\overline{LD}$) pin is then used as a second write enable pin. Setting up the FIFOs in this manner allows depth expansion by having two write enable pins and two read enable pins. The write enables and read enables are then paired, with one set used for system control and the other used for individual FIFO control with external depth expansion logic that is organized to alternately write and read each FIFO. The Almost Full and Almost Empty counters are each being used in this configuration and must be added together to obtain the offset values. Please contact JSI for applications details

Packaging:



	PLCC	TQFP
A	0.590 in	9.00 mm
B	0.553 in	7.00 mm
C	0.453 in	7.00 mm
D	0.490 in	9.00 mm
E	0.105 in	1.60 mm
F	0.050 in	0.80 mm
G	N/A	0.17 mm Max
H	0.420 in	N/A

Please contact JMAR Semiconductor, Inc. for full package drawings and tolerances.



PLCC **TQFP**

Ordering Information:

J JSI — **XXXXXX** Device Type — **X** Power — **X.X** Speed — **X** Package — **X** Temperature Range

Blank - Commercial (0° C. to +70° C.)
I - Industrial (-40° C. to +85° C.)

J – 32 Pin Plastic leaded Chip Carrier
T – Thin Quad Flat pack

7.5 – 133 MHz (Commercial / Industrial)
10 – 100 MHz (Commercial / Industrial)
15 – 66 MHz (Commercial / Industrial)

L – Low Power

72V201 (256 x 9)
72V211 (512 x 9)
72V221 (1024 x 9)
72V231 (2048 x 9)
72V241 (4096 x 9)
72V251 (8192 x 9)

Product Replacement Chart

Size	Speed	JSI Part Number	IDT Part Number	Cypress Part Number
256 x 9 Bits*	133 MHz**	J72V201L7.5	-	-
512 x 9 Bits*	133 MHz**	J72V211L7.5	-	-
1024 x 9 Bits*	133 MHz**	J72V221L7.5	-	-
2048 x 9 Bits*	133 MHz**	J72V231L7.5	-	-
4096 x 9 Bits*	133 MHz**	J72V241L7.5	-	-
8192 x 9 bits*	133 MHz**	J72V251L7.5	-	-
256 x 9 Bits	100 MHz	J72V201L10	IDT72V201L10	-
512 x 9 Bits	100 MHz	J72V211L10	IDT72V211L10	-
1024 x 9 Bits	100 MHz	J72V221L10	IDT72V221L10	-
2048 x 9 Bits	100 MHz	J72V231L10	IDT72V231L10	-
4096 x 9 Bits	100 MHz	J72V241L10	IDT72V241L10	-
8192 x 9 Bits	100 MHz	J72V251L10	IDT72V251L10	-
256 x 9 Bits	66 MHz	J72V201L15	IDT72V201L15	CY7C4201V-15
512 x 9 Bits	66 MHz	J72V211L15	IDT72V211L15	CY7C4211V-15
1024 x 9 Bits	66 MHz	J72V221L15	IDT72V221L15	CY7C4221V-15
2048 x 9 Bits	66 MHz	J72V231L15	IDT72V231L15	CY7C4231V-15
4096 x 9 Bits	66 MHz	J72V241L15	IDT72V241L15	CY7C4241V-15
8192 x 9 bits	66 MHz	J72V251L15	IDT72V251L15	CY7C4251V-15
256 x 9 Bits	50 MHz	J72V201L15***	IDT72V201L20	-
512 x 9 Bits	50 MHz	J72V211L15***	IDT72V211L20	-
1024 x 9 Bits	50 MHz	J72V221L15***	IDT72V221L20	-
2048 x 9 Bits	50 MHz	J72V231L15***	IDT72V231L20	-
4096 x 9 Bits	50 MHz	J72V241L15***	IDT72V241L20	-
8192 x 9 bits	40 MHz	J72V251L15***	IDT72V251L20	-
256 x 9 Bits	40 MHz	J72V201L15***	-	CY7C4201V-25
512 x 9 Bits	40 MHz	J72V211L15***	-	CY7C4211V-25
1024 x 9 Bits	40 MHz	J72V221L15***	-	CY7C4221V-25
2048 x 9 Bits	40 MHz	J72V231L15***	-	CY7C4231V-25
4096 x 9 Bits	40 MHz	J72V241L15***	-	CY7C4241V-25
8192 x 9 bits	40 MHz	J72V251L15***	-	CY7C4251V-25
256 x 9 Bits	28.8 MHz	J72V201L15***	-	CY7C4201V-35
512 x 9 Bits	28.8 MHz	J72V211L15***	-	CY7C4211V-35
1024 x 9 Bits	28.8 MHz	J72V221L15***	-	CY7C4221V-35
2048 x 9 Bits	28.8 MHz	J72V231L15***	-	CY7C4231V-35
4096 x 9 Bits	28.8 MHz	J72V241L15***	-	CY7C4241V-35
8192 x 9 bits	28.8 MHz	J72V251L15***	-	CY7C4251V-35

* Fastest x 9 Synchronous FIFOs available on the market today.

** JSI offers faster devices via speed selection during test.
JSI's FIFOs utilize an internally regulated 2.5V core to provide high performance with low power consumption.

*** JSI's 66MHz devices are full second sources for industry standard 50 MHz, 40 MHz and 28.6 MHz devices.

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