TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

J T 6 N 5 7

LSIs for Serial Port Controller with Built-in Non-Volatile Memory

JT6N57 is a low-power-dissipation, low-operating-voltage LSI developed using Toshiba's CMOS and EEPROM technology combined. The LSI integrates a serial I/O controller and 4-KB EEPROM on a single chip. With low power dissipation, 3- to 5-V operating voltage, Sleep mode, and battery level detector, JT6N57 is ideal for hand-held devices and battery-operated systems.

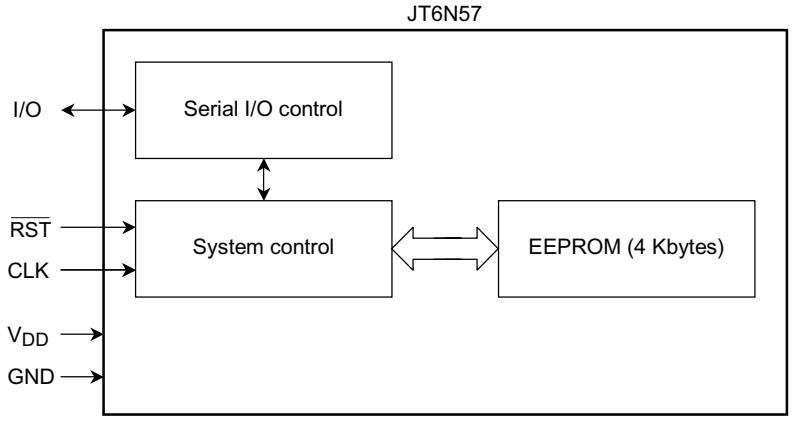
To protect data, JT6N57 can prohibit write to EEPROM when the LSI is abnormal (eg, power supply voltage is low). JT6N57 features protect bits which prevent written data from being erroneously overwritten, a response function which confirms that operation is normal, and a parity check function which confirms that data communications are performed correctly.

Features

- Built-in EEPROM: 4 Kbytes (32 bytes/page × 128 pages)
- Pins: five (V_{DD}, GND, CLK, $\overline{RST}$, I/O (I/O-port-only pin))
- Battery level detector (anti-erroneous EEPROM write operations)
- Byte/Page-write/read function
- Sleep mode (low-power dissipation at standby for input)
- Operating voltage: 2.7 to 5.5 V
- Operating frequency: 1 kHz to 1 MHz (1 kHz to 100 kHz for Page-write)
- Response function and function to display after reset information about the LSI type
- EEPROM protect bits against erroneous overwrite
- Parity check function
- Package: chip/wafer

Note: Overwrite time: 8 ms (max)
Number of writes: 10^5 times (provisional)
Year for retaining data: 10 years (provisional)

Block Diagram



Pad Functions

Pad	Input or Output	Name and Function
I/O	Input or output	I/O port: Serial interface for external devices. Internally pulled up.
$\overline{RST}$	Input	Reset: Input for reset signals from external devices. Schmitt trigger input with internal pull-up.
CLK	Input	Clock: Input for clock signals from external devices. Schmitt trigger input with internal pull-up.
V_{DD}	—	Power supply: Input for power supply from external devices.
GND	—	Ground: Input for power supply from external devices. (+0 V)

Equivalent Circuit Diagrams

(1) CLK, $\overline{RST}$

Both CLK and $\overline{RST}$ are Schmitt trigger inputs with a pull-up resistor.

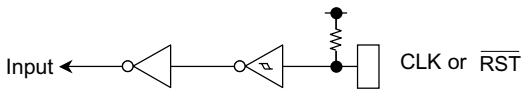


Figure 1

(2) I/O

Serial I/O interface with a pull-up resistor.

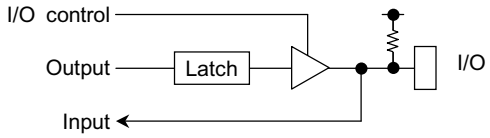
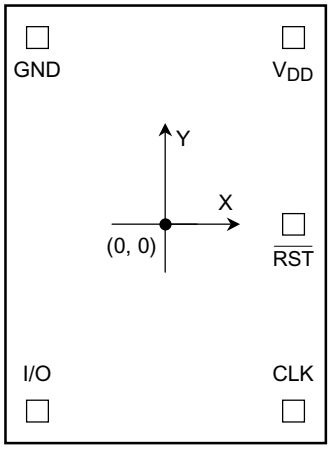


Figure 2

External View



Chip size
L_X: 2.19 mm
L_Y: 2.88 mm

Pad size
100 μm × 100 μm

Pad Coordinates

(μm, μm)

Signal	(X Point, Y Point)	Signal	(X Point, Y Point)
$\overline{RST}$	(900, −50)	V_{DD}	(900, 1060)
CLK	(900, −1030)	GND	(−880, 1050)
I/O	(−880, −1040)	—	—

1. Data Memory

Features are listed below:

- 4 Kbytes (32 bytes × 128 pages)
- Automatic byte overwrite
- Automatic page overwrite (32 bytes)
- Data protection function by protect bits
- Write cycle time: 8 ms (max)

Figure 3 below is the memory map.

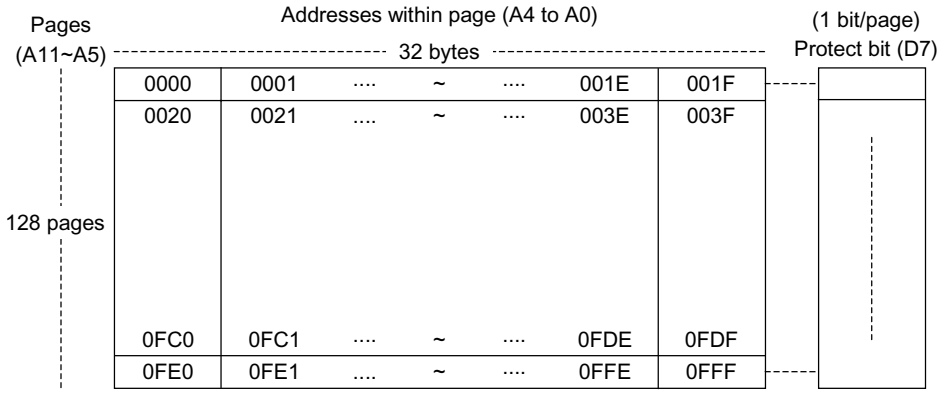


Figure 3 Memory Map

2. Write to EEPROM

JT6N57 supports a Page Write mode for 1-byte write and 32-byte (A4 to A0) write, thus implementing high-speed data storing.

3. Protect Bits

JT6N57 supports protect bits which prohibit writes to EEPROM in units of pages. A protect bit prevents data from being erroneously written to or erased from EEPROM. Writing to a protect bit is the same as writing to the EEPROM data area. A protect bit is assigned to each page. The protect bit address uses A11 to A5 to specify the page. A4 to A0 can be any value.

The data bus for input/output of a protect bit is D7.

Once a protect bit is set to disable write to EEPROM, the protect bit cannot be modified.

Protect Bit (D7) Value	Write to EEPROM Data Area
0	Disable
1	Enable

4. Basic Timing

Figure 4 shows the timing when JT6N57 is reset by a reset signal ($\overline{RST}$). To reset JT6N57, the $\overline{RST}$ pin must be Low for 3 CLKs or longer from a CLK falling edge followed by a rising edge. After the reset signal ($\overline{RST}$) goes High, information about the LSI type is output at the seventh CLK rising edge following the rising edge of the next CLK signal. I/O input can start from the 35th CLK.

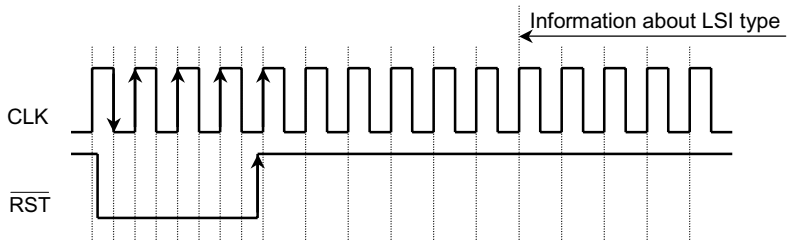


Figure 4 Timing at Reset

5. Sleep Mode

At standby for I/O input after reset or at completion of command execution, JT6N57 automatically enters low-power-dissipation state (Sleep mode). JT6N57 is woken up from Sleep mode by command input.

6. Battery Level Detector

Prohibits erroneous write to EEPROM at low power supply voltage to protect data.

If power supply voltage is abnormal, the response function indicates abnormality.

7. Parity Check Function

An even-parity check function is used for data transfer. Whether communication data are transmitted/received correctly is checked.

If data reception is abnormal, the function prohibits command reception, indicating abnormality using the response function.

8. Response Function

Whether command transmission is normal can be checked.

The response function outputs whether there is a parity error or 2-state battery level detector (BLD) error. If operation is normal, outputs 00h.

Maximum Ratings (levels are shown with GND = 0 V.)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{DD}	−0.5~6.0	V
Input voltage	V_{IN}	−0.5~V_{DD} + 0.5	V
Operating temperature	T_{opr}	−40~85	°C
Storage temperature	T_{stg}	−55~125	°C

Electrical Characteristics

DC Characteristics (unless otherwise noted, V_{DD} = 2.7~5.5 V, GND = 0 V, Ta = −40~85°C)

Parameter		Pad	Symbol	Test Condition	Min	Max	Unit
High-level input voltage		$\overline{RST}$	V_{IH}	—	V_{DD} × 0.8	V_{DD} + 0.3	V
		CLK		—	V_{DD} × 0.7	V_{DD} + 0.3	V
		I/O		—	V_{DD} × 0.7	V_{DD} + 0.3	V
Low-level input voltage		$\overline{RST}$	V_{IL}	—	−0.3	V_{DD} × 0.2	V
		CLK		—	−0.3	V_{DD} × 0.2	V
		I/O		—	−0.3	V_{DD} × 0.2	V
High-level output voltage		I/O	V_{OH}	I_{OH} = −100 μA, V_{DD} = 2.5 V	V_{DD} − 0.8	V_{DD}	V
Low-level output voltage			V_{OL}	I_{OL} = 1 mA, V_{DD} = 2.5 V	0	0.4	V
High-level input current		$\overline{RST}$	I_{IH}	V_{IN} = V_{DD} × 0.8~V_{DD}	−20	10	μA
		CLK		V_{IN} = V_{DD} × 0.7~V_{DD}	−20	10	μA
Low-level input current		$\overline{RST}$	I_{IL}	V_{IN} = GND~V_{DD} × 0.12	−50	−0.1	μA
		CLK		V_{IN} = GND~V_{DD} × 0.12	−50	−0.1	μA
Pull-up resistance		I/O	R_{IN}	—	10	30	kΩ
Battery level detection voltage		V_{DD}	BLD	—	2.10	2.65	V
Current dissipation	Normal conditions	V_{DD}	I_{DD}	V_{DD} = 5.5 V, f (CLK) = 1 MHz	—	7	mA
	Battery open check (CLK IN)			V_{DD} = 5.5 V, f (CLK) = 1 MHz	—	70	μA
	Sleep mode (CLK H STOP)			V_{DD} = 5.5 V, f (CLK) = 1 MHz	—	7	μA

AC Characteristics (unless otherwise noted, V_{DD} = 2.7~5.5 V, GND = 0 V, Ta = –40~85°C)

AC Characteristics at Byte Write/Read and PAGE Read

(values enclosed by square brackets [—] are AC characteristics at page write)

Parameter	Pad	Symbol	Test Condition	Min	Max	Unit
Clock cycle time	CLK	t_{cyc}	Figure 5	1.0 [10]	1000 [1000]	μs
Clock pulse width (high)	CLK	t_{DTYH}	Figure 5	0.35 [3.5]	Tcyc – 0.35 [tcyc – 3.5]	μs
Clock pulse width (low)	CLK	t_{DTYL}	Figure 5	0.35 [3.5]	Tcyc – 0.35 [tcyc – 3.5]	μs
Clock fall time	CLK	t_{cf}	Figure 5	—	100	ns
Clock rise time	CLK	t_{cr}	Figure 5	—	100	ns
I/O port fall time	I/O	t_f	Figure 6	—	200	ns
I/O port rise time	I/O	t_r	Figure 6	—	200	ns
Setup time: $\overline{RST}$ fall to CLK falling time	$\overline{RST}$	tRSF	Figure 7	90	—	ns
Setup time: $\overline{RST}$ rise to CLK falling time	$\overline{RST}$	tRSR	Figure 7	90	—	ns
Hold time: $\overline{RST}$ rise to CLK rising time	$\overline{RST}$	tRHD	Figure 7	50	—	ns
I/O output delay to CLK rising time	I/O	tOD	Figure 6	—	200	ns
Hold time: I/O input rise to CLK rising time	I/O	tIHR	Figure 6	200	—	ns
Setup time: I/O input rise to CLK rising time	I/O	tISR	Figure 6	200	—	ns
Hold time: I/O input fall to CLK rising time	I/O	tIHF	Figure 6	200	—	ns
Setup time: I/O input fall to CLK rising time	I/O	tISF	Figure 6	200	—	ns
EEPROM write cycle time	—	twc	—	—	8	ms
EEPROM data hold term	—	—	Ta = 85°C	10	—	years
EEPROM data re-write times (tentative)	—	—	—	10^5	—	times

AC Test Conditions

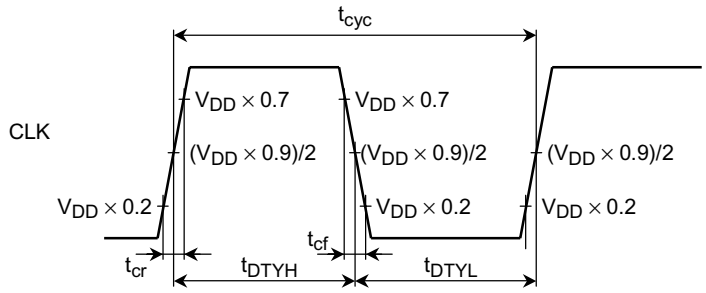
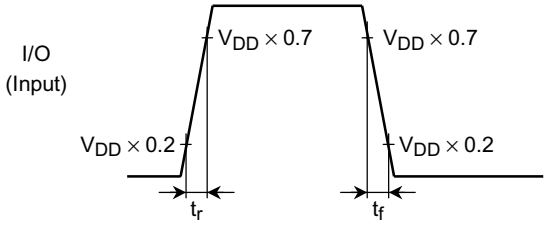


Figure 5 CLK Input Waveform



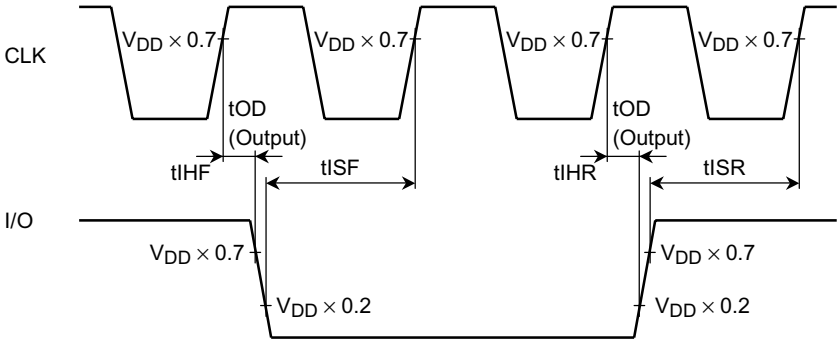


Figure 6 I/O Input Waveform

Reset Timing

To reset JT6N57, the $\overline{RST}$ pin must be Low for 3 states or longer from a CLK falling edge followed by a rising edge. After the reset signal ($\overline{RST}$) goes High, information about the LSI type is output at the seventh state following the rising edge of the next CLK signal. I/O input can start from the 35th state.

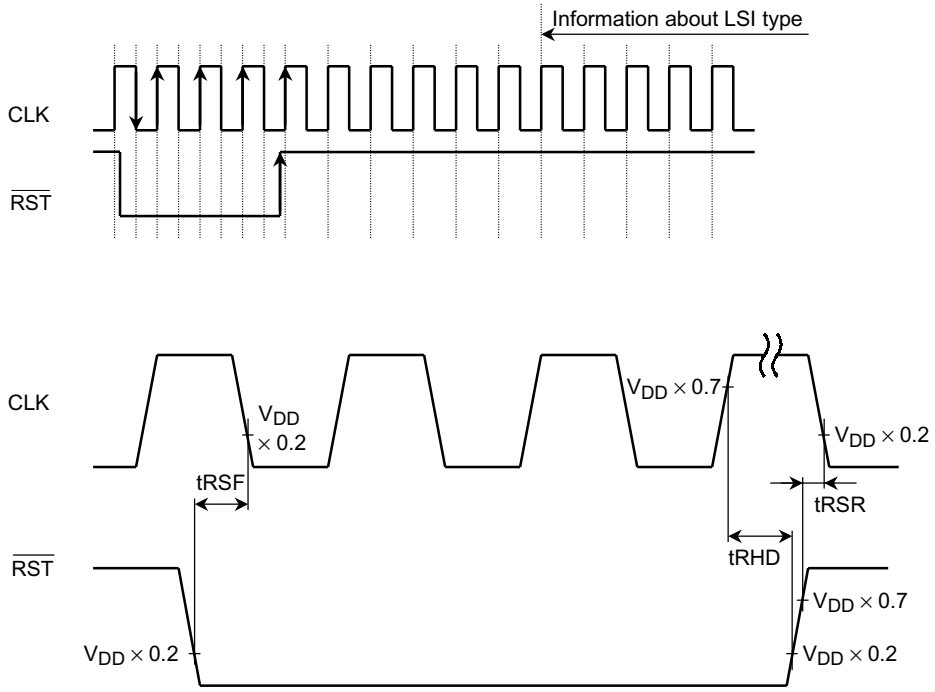


Figure 7 $\overline{RST}$ Input Waveform