TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

JTMP04020-XXXS

CMOS 4 BIT LL MICROCONTROLLER
(LL : LOW POWER CONSUMPTION & LOW VOLTAGE OPERATION MICROCONTROLLER)

JTMP04020-XXXS is a high-performance LL microcontroller developed for use in contact-type personal reader / writers.
JTMP04020-XXXS combines a 4-bit high-performance CPU, memory (work RAM, data RAM, and program ROM), LCD LL controller driver, multi-function timers, IC card power supply (3 V / 5 V switchable), IC card interface, external memory interface, and battery voltage detector circuit on a single chip.
The basic features are as follows :

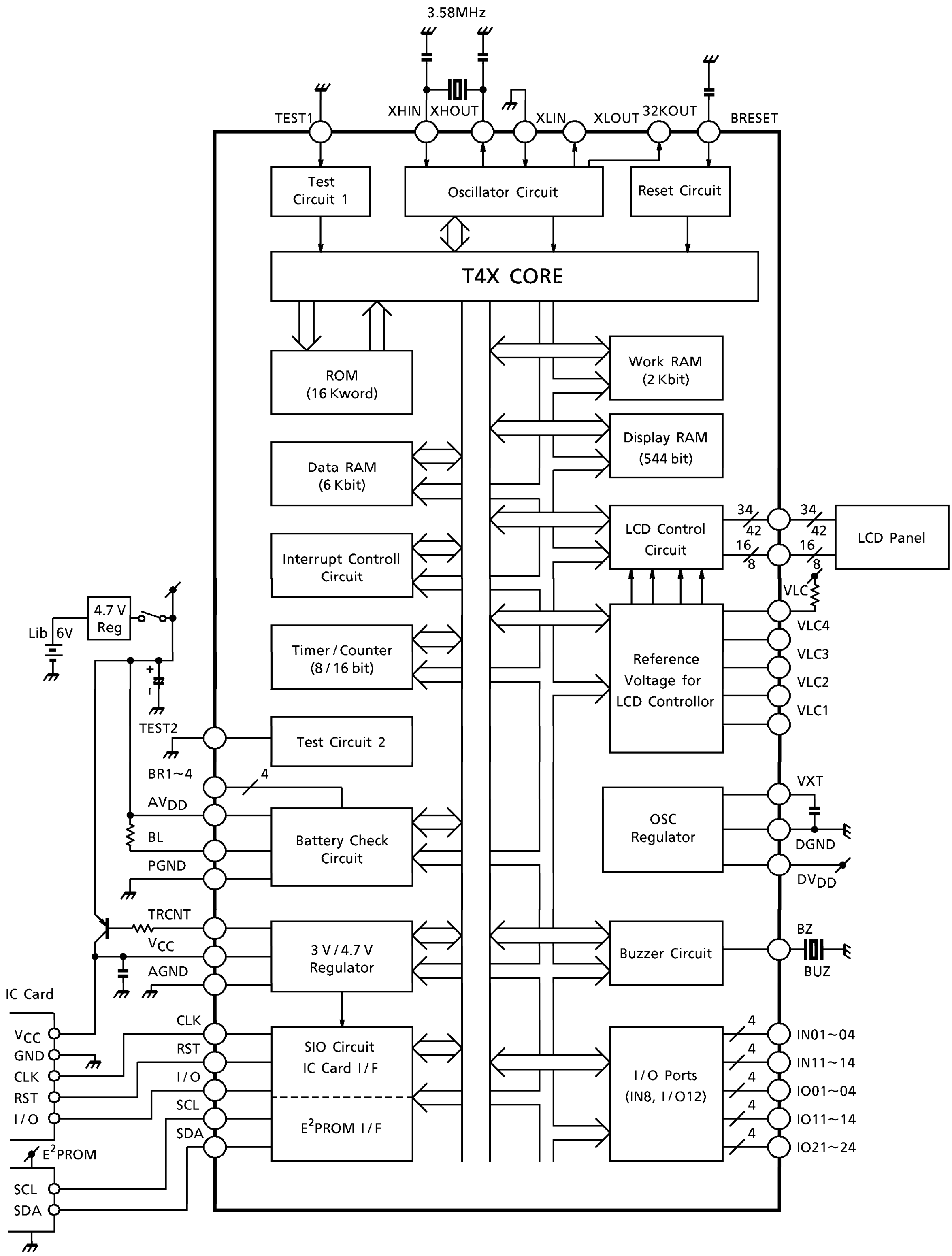
FEATURES

- Number of instructions : 56
- Minimum instruction execution time : 61 μs (at 32.768 kHz)
  57 μs (at 35 kHz)
  1 μs (at 2 MHz / 3.0 V)
  560 ns (at 3.58 MHz / 4.7 V)
- Oscillator circuit :

POWER SUPPLY VOLTAGE	HIGH SPEED	LOW SPEED
3.0 V	2.0 MHz (X'tal)	32.768 kHz (X'tal)
4.7 V	3.58 MHz (X'tal)	35 kHz (Built-in CR)

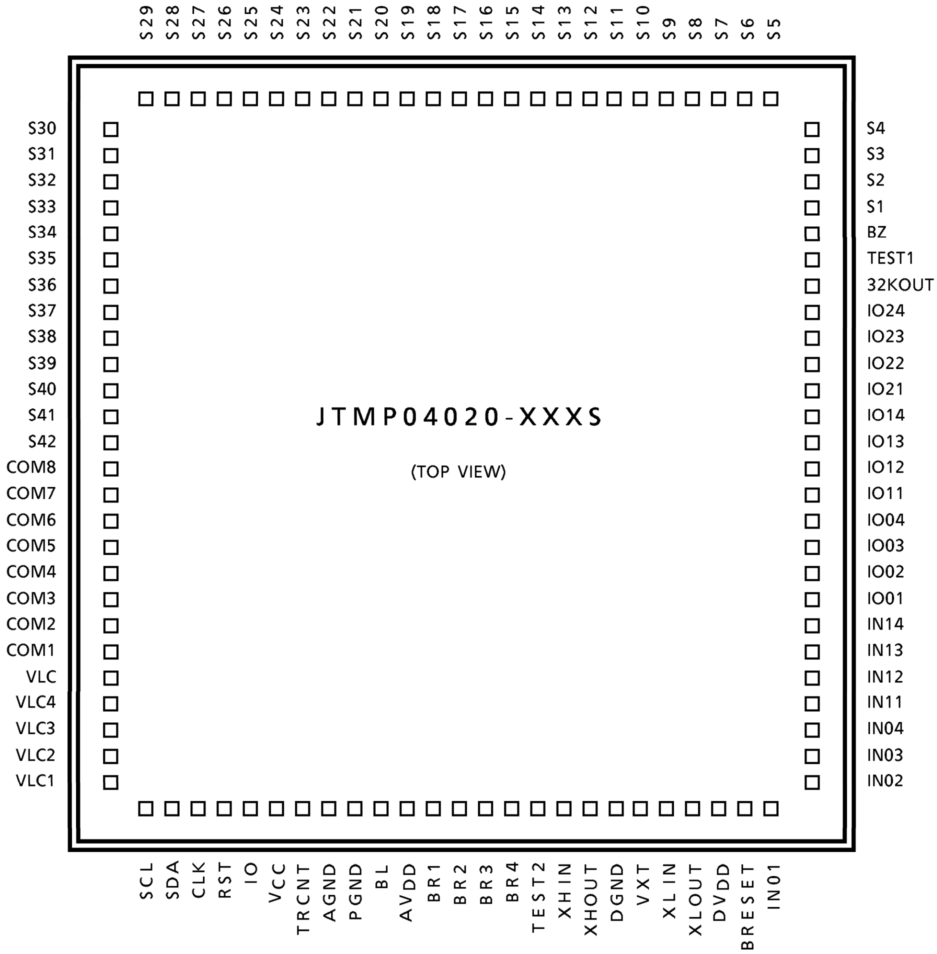
- Built-in ROM size : 16 K words (1 word = 16 bit)
- Built-in RAM size :
  - Work RAM : 512 × 4 bit
  - Data RAM : 6 Kbit
  - Display RAM : 544 bit (16 com × 34 seg)
    : 336 bit (8 com × 42 seg)
- Input pin : 8 pins (with interrupts)
- Input / output pin : 12 pins (output pins for key strobe)
- Output pin : A pin for buzzer output
- Interrupts : 4 external interrupts (input pin, IC card I / F, external memory I / F)
  3 internal interrupts (timer / counter, timing)
- Timer : 8 bit × 2 ch or 16 bit × 1 ch
  (Switchable by software)
- LCD display driver controller : 34 seg × 16 com or 42 seg × 8 com
- Watchdog timer : Timer / counter can be used as watchdog timer.
- Operating power supply voltage : 3.0 V@f = 2 MHz / 4.7 V@f = 3.58 MHz

BLOCK DIAGRAM



PAD / PIN LAYOUT

Pad Assignment



Chip size = 4.92 mm × 5.17 mm
Chip Thickness = 450 μm
Substrate voltage = DGND

Pad Coordinates

No.	PAD NAME	X POINT	Y POINT
1	SCL	– 1840	– 2446
2	SDA	– 1690	– 2446
3	CLK	– 1540	– 2446
4	RST	– 1390	– 2446
5	IO	– 1240	– 2446
6	V_{CC}	– 1090	– 2446
7	TRCNT	– 940	– 2446
8	AGND	– 789	– 2446
9	PGND	– 639	– 2446
10	BL	– 489	– 2446
11	AV_{DD}	– 339	– 2446
12	BR1	– 189	– 2446
13	BR2	– 39	– 2446
14	BR3	111	– 2446
15	BR4	261	– 2446
16	TEST2	411	– 2446
17	XHIN	561	– 2446
18	XHOUT	712	– 2446
19	DGND	862	– 2446
20	VXT	1012	– 2446
21	XLIN	1162	– 2446
22	XLOUT	1312	– 2446
23	DV_{DD}	1462	– 2446
24	BRESET	1612	– 2446
25	IN01	1762	– 2446
26	IN02	2324	– 1989
27	IN03	2324	– 1839
28	IN04	2324	– 1689
29	IN11	2324	– 1539
30	IN12	2324	– 1389
31	IN13	2324	– 1239
32	IN14	2324	– 1089
33	IO01	2324	– 938
34	IO02	2324	– 788
35	IO03	2324	– 638
36	IO04	2324	– 488
37	IO11	2324	– 338
38	IO12	2324	– 188
39	IO13	2324	– 38
40	IO14	2324	112
41	IO21	2324	262
42	IO22	2324	412
43	IO23	2324	563
44	IO24	2324	713

No.	PAD NAME	X POINT	Y POINT
45	32KOUT	2324	863
46	TEST1	2324	1013
47	BZ	2324	1163
48	S1	2324	1313
49	S2	2324	1463
50	S3	2324	1613
51	S4	2324	1763
52	S5	1708	2446
53	S6	1558	2446
54	S7	1408	2446
55	S8	1258	2446
56	S9	1108	2446
57	S10	958	2446
58	S11	807	2446
59	S12	657	2446
60	S13	507	2446
61	S14	357	2446
62	S15	207	2446
63	S16	57	2446
64	S17	– 93	2446
65	S18	– 243	2446
66	S19	– 393	2446
67	S20	– 543	2446
68	S21	– 694	2446
69	S22	– 844	2446
70	S23	– 994	2446
71	S24	– 1144	2446
72	S25	– 1294	2446
73	S26	– 1444	2446
74	S27	– 1594	2446
75	S28	– 1744	2446
76	S29	– 1894	2446
77	S30	– 2324	1778
78	S31	– 2324	1627
79	S32	– 2324	1477
80	S33	– 2324	1327
81	S34	– 2324	1177
82	COM16 / S31	– 2324	1027
83	COM15 / S36	– 2324	877
84	COM14 / S37	– 2324	727
85	COM13 / S38	– 2324	577
86	COM12 / S39	– 2324	427
87	COM11 / S40	– 2324	277
88	COM10 / S41	– 2324	126

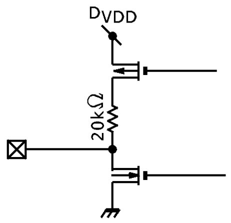
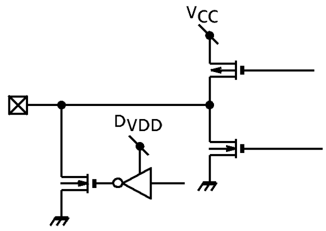
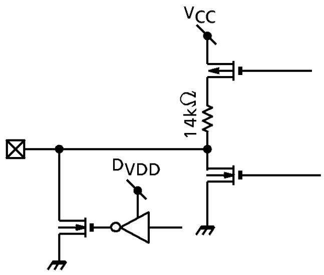
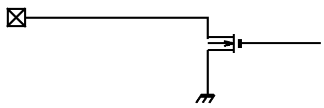
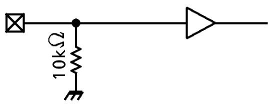
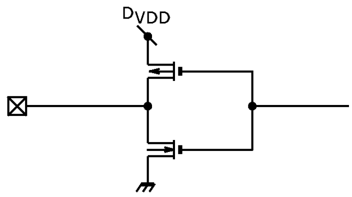
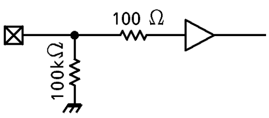
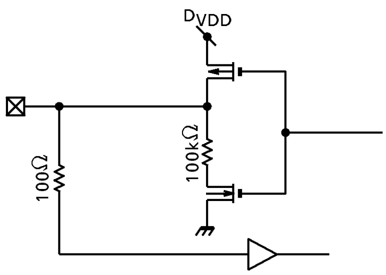
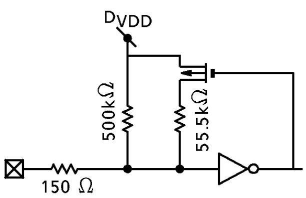
No.	PAD NAME	X POINT	Y POINT
89	COM9 / S42	− 2324	− 24
90	COM8	− 2324	− 174
91	COM7	− 2324	− 324
92	COM6	− 2324	− 474
93	COM5	− 2324	− 624
94	COM4	− 2324	− 774
95	COM3	− 2324	− 924
96	COM2	− 2324	− 1074
97	COM1	− 2324	− 1224
98	VLC	− 2324	− 1375
99	VLC4	− 2324	− 1525
100	VLC3	− 2324	− 1675
101	VLC2	− 2324	− 1825
102	VLC1	− 2324	− 1975

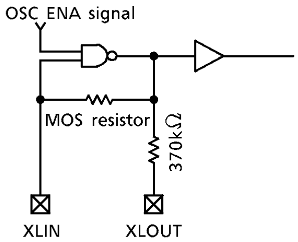
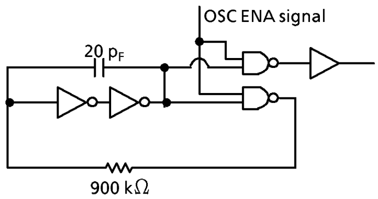
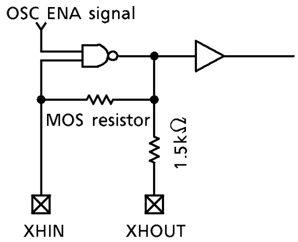
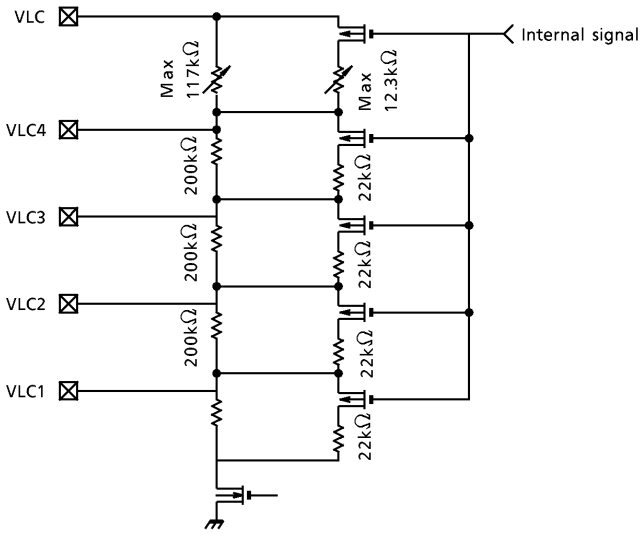
Pin Description

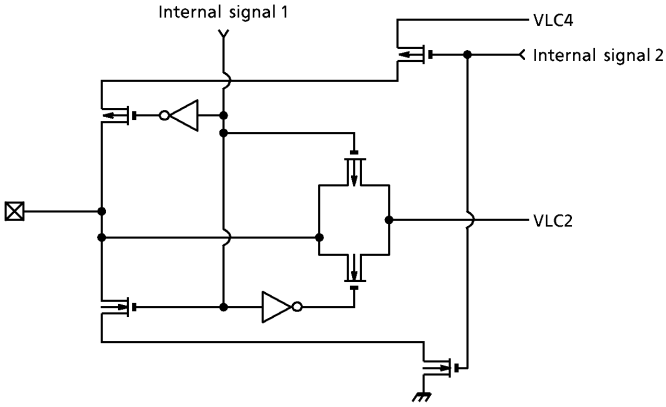
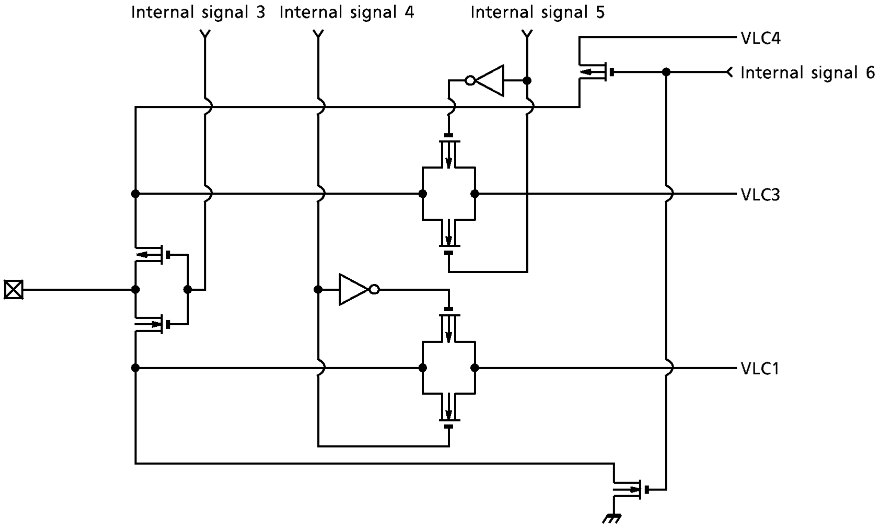
PIN NAME	FUNCTION	Remarks
DV_{DD}	Power supply voltage for logic signals (+)	
AV_{DD}	Power supply voltage for analog signals (+)	
DGND	GND for logic signals (−)	
AGND	GND for analog signals (−)	
PGND	GND for BL pin (−)	
BL	Pseudo-load control for battery voltage difference detection	Cannot be used at 3 V
BR1 to 4	Battery voltage differential detection level setting and external resistor connecting pins	Cannot be used at 3 V
TRCNT	External transistor controller	
V_{CC}	Power supply voltage for IC card	
SEG1~42 (1~34)	LCD segment outputs	
COM1~8 (1~16)	LCD common outputs	
VLC1~4	Reference voltage for LCD	
VLC	Power supply voltage for LCD (+)	
32KOUT	Low-speed oscillation frequency output	
CLK	CLK output for IC card	
I/O	Data I/O for IC card	
RST	Reset output for IC card	
SCL	CLK output for external memory	
SDA	Data I/O for external memory	
IN01~04	Input ports (with interruption)	
IN11~14	Input ports (with interruption)	
IO01~04	I/O ports	
IO11~14	I/O ports	
IO21~24	I/O ports	
XHIN~XHOUT	Crystal connection pin for high-speed oscillator	
XLIN~XLOUT	Crystal connection pin for low-speed oscillator	
BZ	Buzzer output	
BRESET	Reset input (low active)	
TEST1	Test input for logic signal	
TEST2	Test input for analog signal	

(Note) : Pay attention to the following notes when designing circuit board layout.
(1) Do not locate the high-speed and low-speed clocks line side by side.
(2) Do not locate the clock line and the large current line side by side.
(3) Do not locate lines with analog characteristics and lines with large current line side by side.
(4) Do not locate lines with analog characteristics and clock lines side by side.

Pin

Pin name	Pin configuration	Pin name	Pin configuration
SCL SDA		CLK RST	
IO		BL	
TEST1 TEST2		BZ 32KOUT	
IN01 ~ 04 IN11 ~ 14		IO01 ~ 04 IO11 ~ 14 IO21 ~ 24	
BRESET			

Pin name	Pin configuration	Pin name	Pin configuration
XLIN XLOUT	① AL option: Crystal oscillator  ② AI option: Internal CR oscillation  (As the CR oscillation is fully internal, it is not output on the pin.)	XHIN XHOUT	
VLC VLC1 to 4	 		

Pin name	Pin configuration
SEG pin	
COM pin	

MEMORY MAP

1. Program ROM

Program ROM consists of 16 bits per 1 word. Op-code and operand are executed in one word units. Program ROM consists of 4 K words per page. The internal program ROM area is 4 pages (16 K words).
This program ROM area can be used for storing constant data. In this case, it can be used in byte units (1 byte = 8 bits).

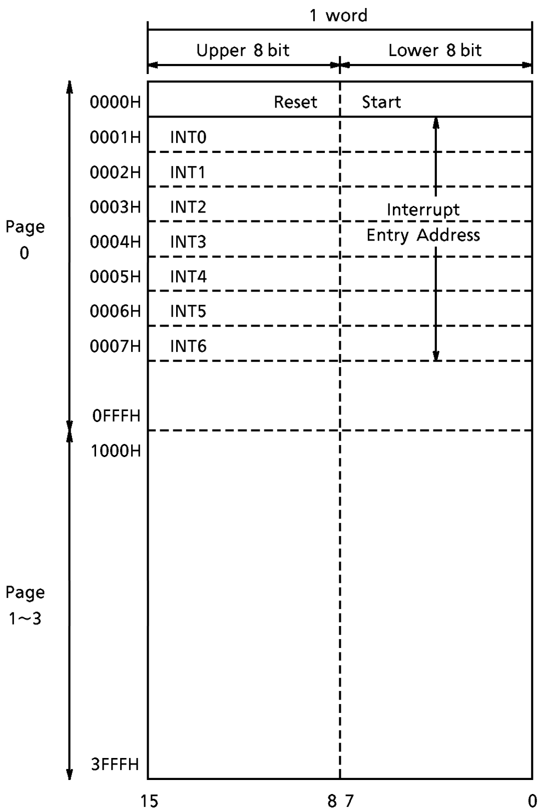


Fig.1 Program memory map

(Note) : Use the CALL instruction to write the interrupt entry address. Write NOP for unused interrupts.

```
Example :  CALL A  ; INT0
           NOP     ; INT1
           CALL B  ; INT2
           NOP     ; INT3
           NOP     ; INT4
           NOP     ; INT5
           NOP     ; INT6
```

2. Work RAM

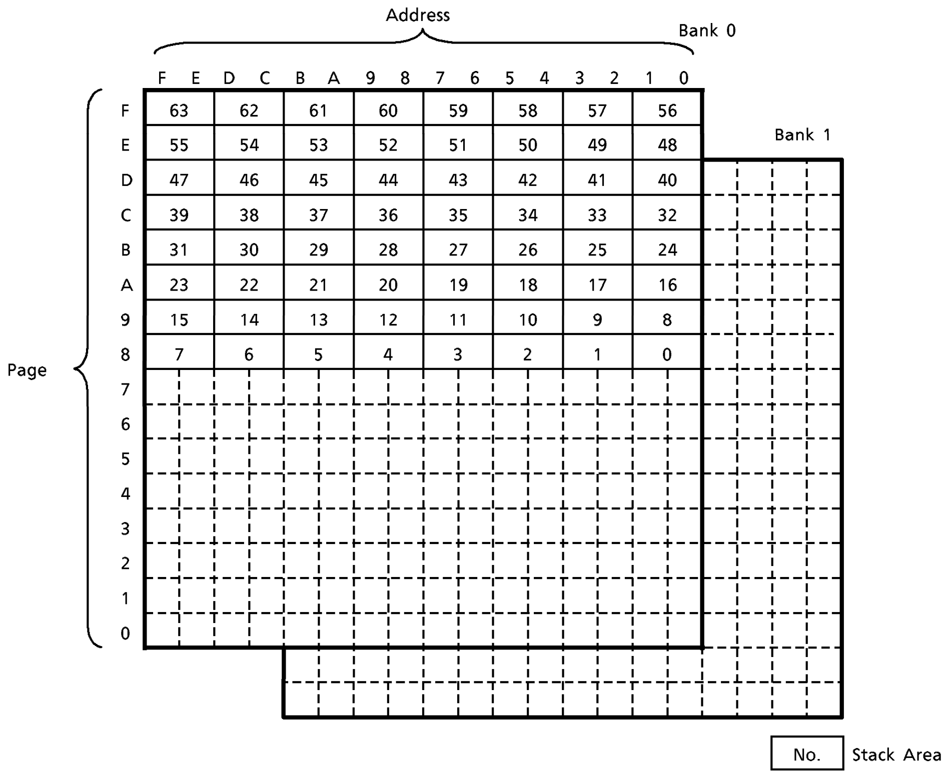
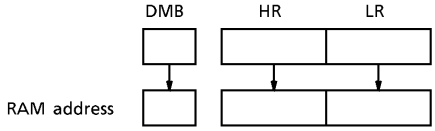


Fig.2 Work RAM

Work RAM consists of 512 × 4 bits.
R / W is performed at the address specified by bellows.

(1) Indirectly addressing mode (Fig.3 (a))

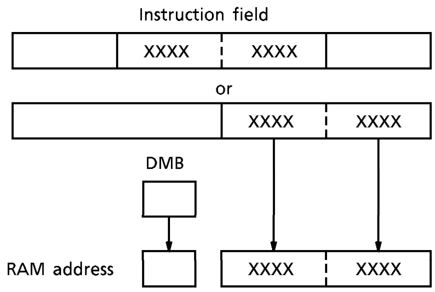
DMB in F-reg, H, L-reg specify the Work RAM address.
(DMB : bank, H-reg : page, L-reg : address)
EX. LD A, M : A ← RAM (HL)



(a) Indirectly addressing

(2) Directly addressing mode (Fig.3 (b))

Immediate data (8 bits) in instruction specify the Work RAM page and address.
Bank is specified by DMB in F-reg.
EX. LD 2CH, 0AH : RAM (2CH) ← AH

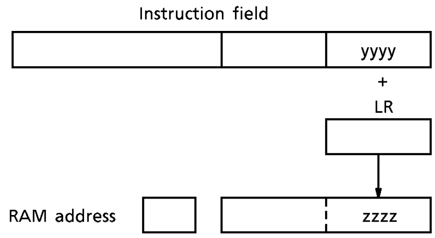


(b) Directly addressing

(3) Index addressing mode (Fig.3 (c))

Address is specified by adding 4 bits (L-reg) and the immediate data (4 bits) in instruction.

EX. LDRI 4H, 3H : RAM (HL + 4H)
← RAM (3H, L)
L ← L + 1, A ← A − 1



(c) Index addressing

Fig.3 Addressing mode

BANK 0, PAGE 8~F area can be used as Stack area.
When using the "CALL / CALLS" instruction or start the interruption routine, the data of program counter and Program memory bank are stored in Stack area.
Then, using "RET" instruction, program return according to those data.
And, using "PUSH" instruction, 8 bits data in a pair register can be stored in Stack area.
Then, using "POP" instruction, those data are returned to the register.
Maximum Stack area is 64 (0~63), and each Stack area consist of 8 bits.

Register File

PAGE (RFB)		ADDRESS	0		1		2		3		4		5		6		7	
		8BIT ADDRESS	0				2				4				6			
			LOWER4BIT		UPPER4BIT		L4BIT		H4BIT		L4BIT		H4BIT		L4BIT		H4BIT	
		R / W	READ	WRITE	READ	WRITE	READ	WRITE	READ	WRITE	READ	WRITE	READ	WRITE	READ	WRITE	READ	WRITE
0	MSB	BIT 3	F REGISTER		A REGISTER		L REGISTER		H REGISTER		E REGISTER		D REGISTER		P REGISTER		B REGISTER	
		BIT 2																
		BIT 1																
	LSB	BIT 0																
1	MSB	BIT 3	STACK POINTER (SP)		0		INT2		INT6		IOD14	IOO14	IOD24	IOO24				
		BIT 2					INT1		INT5		IOD13	IOO13	IOD23	IOO23		LVLC2		
		BIT 1					INT0		INT4		IOD12	IOO12	IOD22	IOO22		LVLC1		
	LSB	BIT 0	0				0		INT3		IOD11	IOO11	IOD21	IOO21		LVLC0		
2 (PAx)	MSB	BIT 3	IND04		IND14		CONTCLK		FCLK3		SELT		TREFLG		FSEL			RST4
		BIT 2	IND03		IND13		ENACLK		FCLK2		DTPB		RCEFLG		LOWCP			RST3
		BIT 1	IND02		IND12		IODATA	CONTIO	FCLK1		RTST		PEFLG		CPMODE2			RST2
	LSB	BIT 0	IND01		IND11		RES		FCLK0		CDST		RDEFLG		CPMODE1			RST1
3 (PBx)	MSB	BIT 3									RAR4		RAC4		RAD4		RAD8	
		BIT 2									RAR3		RAC3		RAD3		RAD7	
		BIT 1							RAB2		RAR2		RAC2		RAD2		RAD6	
	LSB	BIT 0	CE1						RAB1		RAR1		RAC1		RAD1		RAD5	
4 (PCx)	MSB	BIT 3	MCLK		IIN04		IIE04		RIO		BCOUT1		SELS3		32KOUT		BZCNT1	
		BIT 2	ESELT		IIN03		IIE03		ISIO		BCOUT0		SELS2			DRCE	BZCNT0	
		BIT 1	ESELI1		IIN02		IIE02		IICCD		SELBL		SELS1			DON	P2	
	LSB	BIT 0	ESELI0		IIN01		IIE01		IOIE0		SELBC		SELS0			DSTA	P1	
5 (PDx)	MSB	BIT 3	TI4		1.7 / 3.4			TIR4	TIE4		DRR4				DRD4		DRD8	
		BIT 2	TI3		6.8 / 13.5			TIR3	TIE3		DRR3		DRC3		DRD3		DRD7	
		BIT 1	TI2		27 / 55			TIR2	TIE2		DRR2		DRC2		DRD2		DRD6	
	LSB	BIT 0	TI1		218 / 437			TIR1	TIE1		DRR1		DRC1		DRD1		DRD5	
6 (PEx)	MSB	BIT 3	TCR14	SET14	TCR18	SET18	MRIO		TC1EN		REQT1		SELSIO		IOD04	IOO04	2 / 4K	
		BIT 2	TCR13	SET13	TCR17	SET17	CKS13			TC1R	REQT0		PWCD		IOD03	IOO03	BZ3	
		BIT 1	TCR12	SET12	TCR16	SET16	CKS12		CMPEN1		TCI1E		ENA5V / 3V		IOD02	IOO02	BZ2	
	LSB	BIT 0	TCR11	SET11	TCR15	SET15	CKS11		WDT1			TCI1R	BITACK		IOD01	IOO01	BZ1	
7 (PFx)	MSB	BIT 3	TCR24	SET24	TCR28	SET28	TCPS		TC2EN		LD1		EXMMODE1		SID7		SID3	
		BIT 2	TCR23	SET23	TCR27	SET27	CKS23			TC2R	LD0		EXMMODE0		SID6		SID2	
		BIT 1	TCR22	SET22	TCR26	SET26	CKS22		CMPEN2		TCI2E		EXMRW		SID5		SID1	
	LSB	BIT 0	TCR21	SET21	TCR25	SET25	CKS21		SELCLK			TCI2R	EXMSTA		SID4		SID0	

(Note) : Blank columns are indeterminate.

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3. Data RAM

JTMP04020-XXXS has 6 K bits Data RAM (256 AD × 3 bank × 8 bit), and addressing and data read / write is done by Register file, as follows.
When the data is read from Data RAM / written in Data RAM, CE1 (PB0-bit0) is needed to set 1.
(R30 : Register file Page 3, AD0)

	MSB 3	2	1	0 LSB
PB0	—	—	—	CE1

Addressing is decided by RAB1~2 (R33-bit0, 1), RAC1~4 (R35), RAR1~4 (R34)

		MSB 3	2	1	0 LSB
BANK	R33	—	—	RAB2	RAB1
ROW	R34	RAR4	RAR3	RAR2	RAR1
COLUMN	R35	RAC4	RAC3	RAC2	RAC1

Data is read / written by 8 bits which is set in RAD1~8 (PB6, PB7).

	MSB 3	2	1	0 LSB
PB7	RAD8	RAD7	RAD6	RAD5
PB6	RAD4	RAD3	RAD2	RAD1

(Note) : When "HALT" instruction is excuted for the next instruction of transference the data to Data RAM, the data of Data RAM is broken. Also, data may be destroyed if the HALT instruction is executed while CE1 is set to 1. Therefore, be sure to set CE1 to 0 before executing the HALT instruction.
RAD1 to 8 (R36, R37) are valid for only 8-bit transfer instructions.
4-bit transfer instructions do not have any effect (NOP).
(No operation at a write.
Data may be corrupted because the bus data are written to work RAM at a read.)

Data RAM

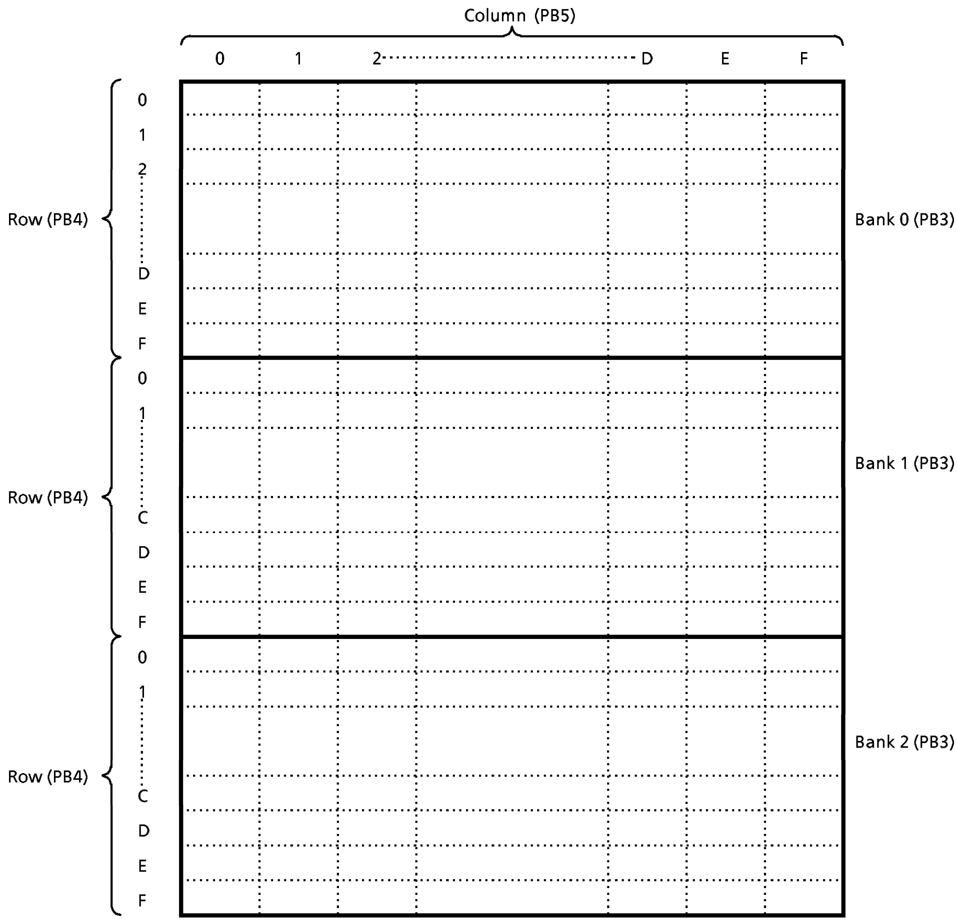


Fig.4 Data RAM

4. Display RAM

JTMP04020-XXXS has Display RAM, and addressing and data read / write is decided by Register file, as follows.
When the data is read from / written into Display RAM, DRCE (R46-bit2) is needed to be 1.

	MSB 3	2	1	0 LSB
PC6	(32KOUT)	DRCE	DON	DST

Addressing is decided by DRR1~4 (PD4), DRC1~3 (PD5-bit0, 1, 2) (LSB is DRR1, and MSB is DRC3)

	MSB 3	2	1	0 LSB
PD5	—	DRC3	DRC2	DRC1
PD4	DRR4	DRR3	DRR2	DRR1

The DRD1 to DRD8 (PD6, PD7) data are written to / read from Display RAM.
Data is read / written by 8 bits.

	MSB 3	2	1	0 LSB
PD7	DRD8	DRD7	DRD6	DRD5
PD6	DRD4	DRD3	DRD2	DRD1

(Note 1) : When "HALT" instruction is executed for the next instruction of the transference the data to Display RAM, the data of Display RAM is broken.
When "HALT" instruction is executed during DRCE is 1, the data of Display RAM is broken.
Therefore, be sure to set DRCE to 0 before executing the HALT instruction.
DRD1 to 8 (PD6, PD7) are valid for only 8-bit transfer instructions.
4-bit transfer instructions do not have any effect (NOP).

	DRD 8	DRD 7	DRD 6	DRD 5	DRD 4	DRD 3	DRD 2	DRD 1	
00H	COM8	COM7	COM6	COM5	COM4	COM3	COM2	COM1	→ S_1
01H									→ S_2
02H									→ S_3
2AH	1	1	1	1	1	1	1	1	
	1	1	1	1	1	1	1	1	
3FH	1	1	1	1	1	1	1	1	
40H	COM16	COM15	COM14	COM13	COM12	COM11	COM10	COM9	→ S_1
41H									→ S_2
60H									→ S_{33}
61H									→ S_{34}
62H	1	1	1	1	1	1	1	1	
	1	1	1	1	1	1	1	1	
	1	1	1	1	1	1	1	1	
7FH	1	1	1	1	1	1	1	1	

Fig.5 Display RAM

(Note 2) : The display RAM map area designated as "1" in Figure 4 is accessible by tools, that area cannot be used by this product.

REGISTER FILE

Register files consist of (1) general-purpose registers, (2) system registers, and (3) peripheral I / O registers.

1. Flag Register : F-Register (PAGE / AD = 0 / 0)

F-Register

	MSB 3	2	1	0 LSB
R00	DMB	(0)	ZF	CF

CF : Carry Flag
ZF : Zero Flag
(0) : Not use
DMB : Work RAM Bank

2. Accumulater Register : A-Register (PAGE / AD = 0 / 1)
3. H.L Register (PAGE / AD = 0 / 3~2)

   H.L Register are used for Work RAM address setting with DMB.

H-Register

	MSB 3	2	1	0 LSB
R03	HR3	HR2	HR1	HR0

Work RAM page

L-Register

	MSB 3	2	1	0 LSB
R02	LR3	LR2	LR1	LR0

Work RAM Address

4. Bank Register (PAGE / AD = 0 / 7)

   B-Register is used for ROM Page.

	MSB 3	2	1	0 LSB
R07	3	2	1	0

0000 = Page 0
0001 = Page 1
0010 = Page 2
0011 = Page 3

5. D-Register, E-Register, P-Register

   There are general purpose registers. (PAGE / AD = 0 / 5, 0 / 4, 0 / 6)
   When using ROM as Data Table Function, B, P, D, E-Register are used for ROM address setting. (Data table function : user can use ROM area for store the constant, and can access those constant by LDBL and LDBH instruction.)

PERIPHERAL CIRCUIT

Each peripheral circuits can be accessed (Read / Write / Circuit setting) by Register files.

1. Oscillator Block

	MSB 3	2	1	0 LSB
PA6	FSEL	LOWCP	CPMODE2	CPMODE1

The CPU clock is generated by the asynchronous oscillator switching circuit which has low-speed and high-speed clock oscillator circuit.
This block also provides the clock for the timer circuit and LCD driver.
Oscillation mode is controlled by Register files "CPMODE1" and "CPMODE2" (PAGE / AD = 2 / 6), as follows.

CPMODE 2	CPMODE 1	Low-speed OSC	High-speed OSC	SYSTEM CP	MODE name
0	0	OFF	OFF	OFF	(CPM0)
0	1	ON	OFF	Low speed	(CPM1)
1	0	OFF	ON	High speed	(CPM2)
1	1	ON	ON	High speed	(CPM3)

CPMODE 1, 2 are initially 1 (CPM3).
"LOWCP" is the display clock control bit. When "LOWCP" is set to 1, Low OSC clock is supplied to LCD circuit. "LOWCP" is initially "0". Even if LOWCP is set to 1, clock cannot be occupied to display circuit during Low-speed OSC stopped, and display cannot be shown.
Low-speed OSC circuit can select X'tal or internal CR oscillation by Mask option.
High-speed OSC circuit can select X'tal or external CR oscillation by Mask option.
Setting a register to CPM1 and executing a HALT instruction sets the mode to Halt (system CP off, high-speed oscillator off, low-speed oscillator on). Setting a register to CPM0 and executing a HALT instruction sets the mode to Stop (system CP off, high-speed oscillator and low-speed oscillators off).
Even if, mode is changed to MODE 0 from MODE 1 / 2 / 3, there are no changing until use "HALT" instruction.
The High-speed / low-speed OSC circuit has WARM UP function. The low-speed oscillation does not have enough warm-up time, therefore when the oscillation is started, software need to make warming up time enoughly.
When the System CP is changed between Low and High (CPM1 → CPM2 / 3, CPM2 → CPM1), changing System CP waits to finish the warming up time.
Until the system CP is changed, instructions are executed with the previous system CP.

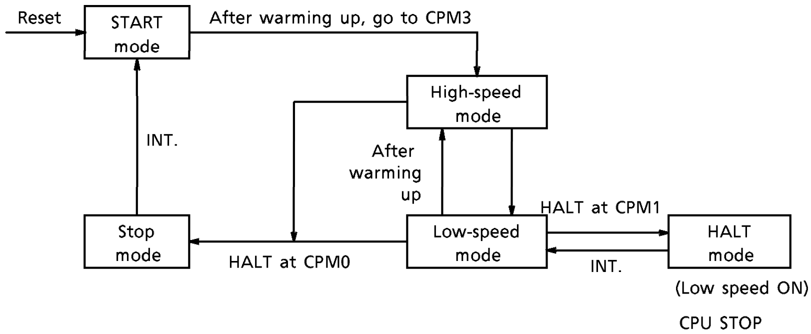


Fig.6 Mode status

JTMP04020-XXXS has 21 bits Divider.
(When using a 3.58 MHz crystal as the high-speed oscillator, the frequency divider supplies 1.79 MHz to 1.79 Hz.) The clock supplied to the frequency divider for bit 7 and onwards can be forcibly switched. Setting FSEL = 1 supplies a $fH/2^6$ clock (regardless of CP mode). Setting FSEL = 0 supplies a clock according to the CP mode. (When the low-speed oscillator is ON, 32 kHz is supplied.) The initial value of FSEL is 0.
The reset for this Divider circuit is done by Register file RST1~4 (R27W).

	MSB 3	2	1	0 LSB
PA7W	RST4	RST3	RST2	RST1

RST1 : Binary counter 1~6 (3.58 M~56 kHz) reset
RST2 : Binary counter 7~12 (28 k~896 Hz) reset
RST3 : Binary counter 13~17 (448~28 Hz) reset
RST4 : Binary counter 18~21 (14~1.75 Hz) reset
(when using 3.58 MHz crystal)

(Note 1) : Do not set System CP to low speed when the Low-speed OSC is not in operation or before stable.

(Note 2) : Do not set System CP to high speed when the High-speed OSC is not in operation or before stable.

(Note 3) : And, when Low-speed OSC is on, low-speed frequency is supplied to 7th bit Divider circuit and onwards (when use 3.58 MHz crystal and low-speed oscillator with 32 kHz crystal for High-speed OSC and the mode is CPM3, 1.79 MHz~56 kHz are made from 3.58 MHz crystal, 16 kHz~1 Hz are made from 32 kHz crystal oscillator. And when the mode is CPM2, all frequency are made from 3.58 MHz crystal. Therefore if the mode change between CPM1 and CPM2 or CPM2 and CPM3, the frequency which is supplied by Binary counter 7~21 shift the timing).

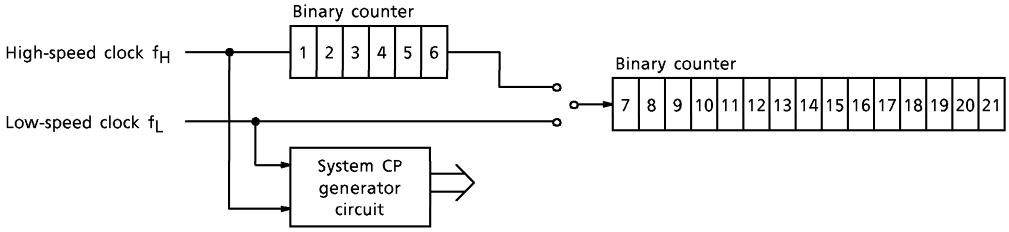


Fig.7 Divider circuit

Example 1

START mode (After warming up, program start at address 0000.)
↓
CPM3 (High / Low speed ON, SYSCP = High, LOWCP OFF)
↓ LD 26O, 7H
CPM3 (High / Low speed ON, SYSCP = High, LOWCP ON)
↓ LD 26O, 4H
CPM0 (High / Low speed ON, SYSCP = High, LOWCP ON)
↓ HALT
STOP mode (High / Low-speed OSC, STOP, SYSCP OFF, LOWCP OFF)

When an interruption occurs, the mode is changed to START mode and program start at the address which is decided by each interruption (refer to Fig.6).

Example 2

START mode (After warming up, program start at address 0000.)
↓
CPM3 (High / Low speed ON, SYSCP = High, LOWCP OFF)
↓ LD 26O, 5H
CPM1 (Low speed ON, SYSCP = Low, LOWCP ON)
↓ HALT
HALT mode (High-speed OSC OFF, Low-speed OSC ON, SYSCP OFF, LOWCP ON)

When an interruption occurs, the mode is changed to slow mode (CPM1) and program start at the address which is decided by each interruption (refer to Fig.6).

Example 3

START mode (After warming up, program start at address 0000.)

↓

CPM3 (High / Low speed ON, SYSCP = High, LOWCP OFF)

↓ LD 26O, 7H

CPM3 (High / Low speed ON, SYSCP = High, LOWCP ON)

↓ LD 26O, 4H

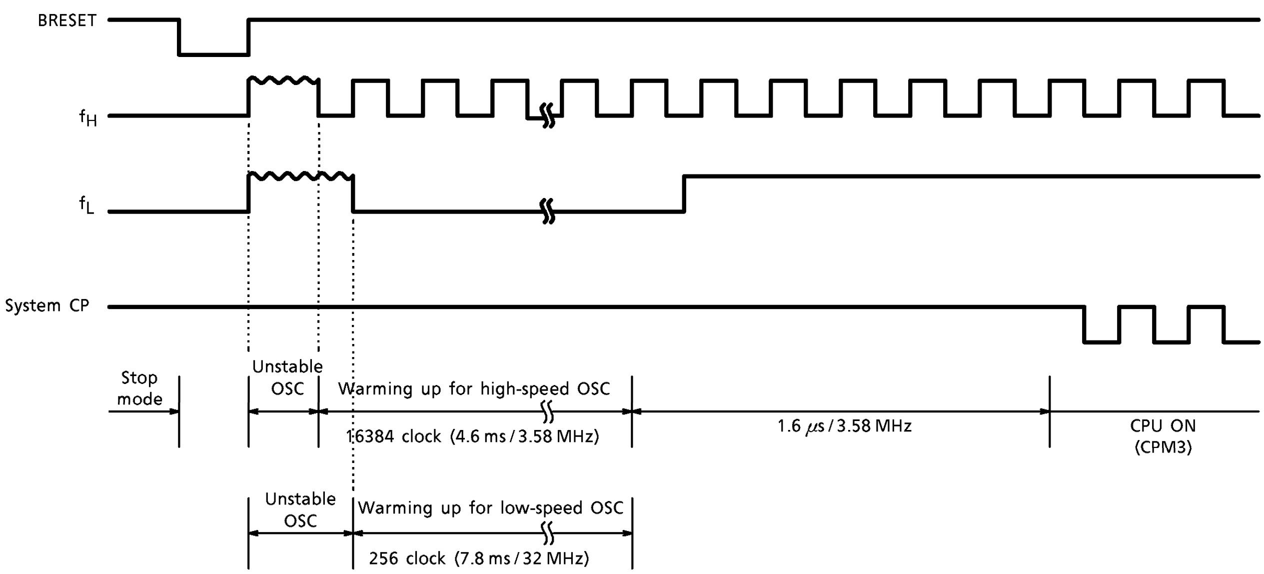
CPM0 (High / Low speed ON, SYSCP = High, LOWCP ON)

(There are no change after shift to CPM0.)

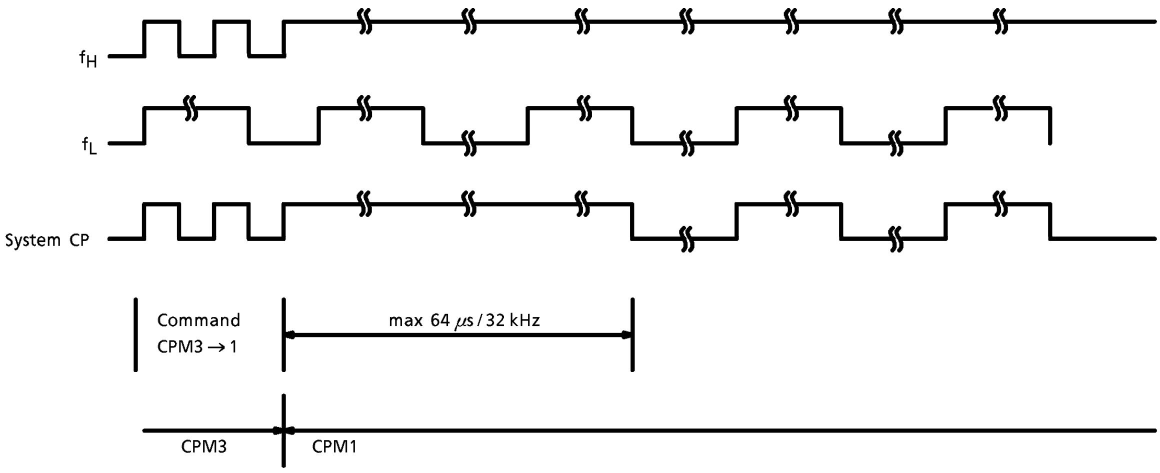
↓ LD 26O, 7H

CPM3 (High / Low speed ON, SYSCP = High, LOWCP ON)

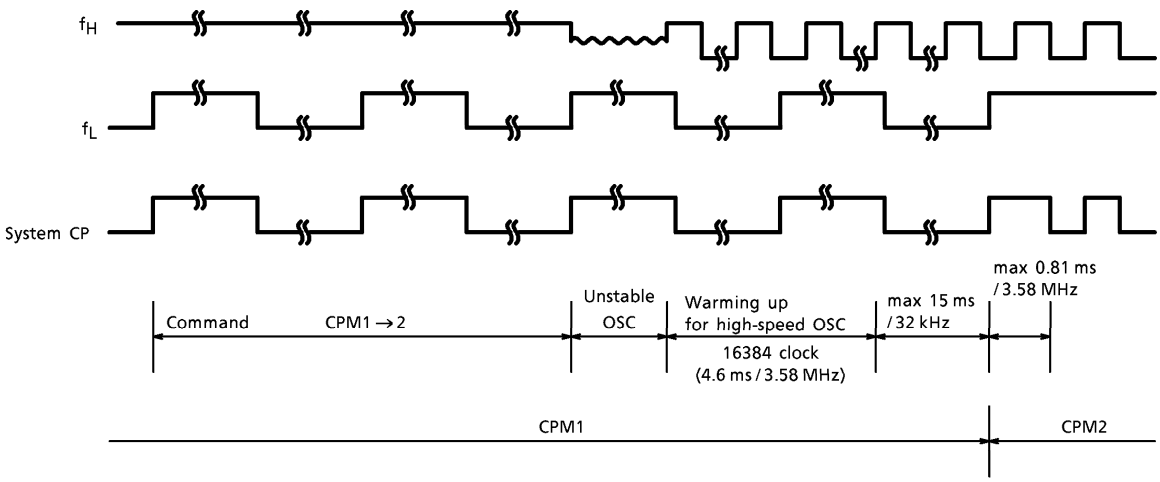
Example 4 (After reset)



Example 5 (CPM3 → 1)



Example 6 (CPM1 → 2)



(Note) : Warm-up is not provided for low-speed RC oscillations by mask options.

2. Interruption Block

Interruption is supplied by IN01~04, IN11~14, Timer / Counter, Timing, IC card I / F and external memory I / F.

(Interruption Priority)

Interruption priority can be selected by Register file P1 (PC7-bit0) and P2 (PC7-bit1).
P1 and P2 are initially 0.

(Note) : Note that once interrupt priority is set in register files P1 and P2, the priority is protected.

	MSB 3	2	1	0 LSB
PC7	(BZCNT1)	(BZCNT0)	P2	P1

P2	P1	INT0	INT1	INT2	INT3	INT4	INT5	INT6
0	0	IIN0	IIN1	TIN	IICCD	ISIO	TCIN1	TCIN2
0	1	IIN1	IIN0	TIN	IICCD	ISIO	TCIN1	TCIN2
1	0	TIN	IIN0	IIN1	IICCD	ISIO	TCIN1	TCIN2
1	1	TCIN1	IIN0	IIN1	TIN	IICCD	ISIO	TCIN2

(Higher) ←—— Priority ——→ (Lower)

(IIN0 : IN01~04, IIN1 : IN11~14, TIN : TIMING
TCIN1 / 2 : TIMER / COUNTER1/ 2,
IICCD : ICCARDIF, ISIO : SIOIF)

(Interruption enable / disable)

Each interruption (IIN0, IN1, TIN, TCIN1, TCIN2, IICCD, ISIO) is decided enable / disable as follows.

IIN0	:	IIE01~04	(PC2-BIT0~3)
IIN1	:	IOIE0	(PC3-BIT0)
TIN	:	TIE1~4	(PD3-BIT0~3)
TCIN1	:	TCI1E	(PE4-BIT1)
TCIN2	:	TCI2E	(PF4-BIT1)
IICCD	:	IICCD	(PC3-BIT1)
ISIO	:	ISIO	(PC3-BIT2)

After deciding priority by P1, P2, each interruption is decided enable / disable by INT0~6.
Disable the unnecessary interrupts in your application by initial settings of IIE01~04, IOIE0, TIE1-4 and TCI1E / 2E.
INT0~6 are initially 0 (disable)

	MSB 3	2	1	0 LSB
R12	INT2	INT1	INT0	(0)
R13	INT6	INT5	INT4	INT3

INT0~6 = 0 : INT0~6 disable
= 1 : INT0~6 enable

(Interrupt reset)

After assertion of an interrupt is detected, reset the interrupt following the procedures described below.
First reset the interrupt latch by disabling the interrupt (input interrupts IN01 to IN04, timing interrupts TI1 to TI4, timer / counter interrupts TCI1 and TCI2) using the corresponding register file (IN01 to IN04 : PC2 (IIE01 to IIE04)*2, IN11 to IN14 : PC3 (IOIE0)*2, TI1 to TI4 : PD3 (TIE1 to TIE4)*1, TCI1 : PE4 (TCI1E)*1, TCI2 : PF4 (TCI2E)*1, IICCD : PC3 (IICCD)*1, ISIO : PC3 (ISIO)*1). Next, reset the interrupt latch circuit for the core by disabling / enabling the interrupt using register file R12 or R13. (Enable the interrupt again by a transfer instruction to R12 or R13 if necessary.)

*1 : Regarding INT Latch of TIN, TCIN1, TCIN2, It is able to reset each Latch at both case of enabling disabling each resistor file (TIE1 to 4, TCI1E, TCI2E). It is also able to reset each INT Latch by setting each resistor file for reset (TIR1 to 4, TCI1R, TCI2R).

*2 : Regarding IIN0, IIN1, IICCD, ISIO, It is able to reset each INT Latch only when disabling each resistor file (IIE01 to 04, IOIE0, IICCD, ISIO).

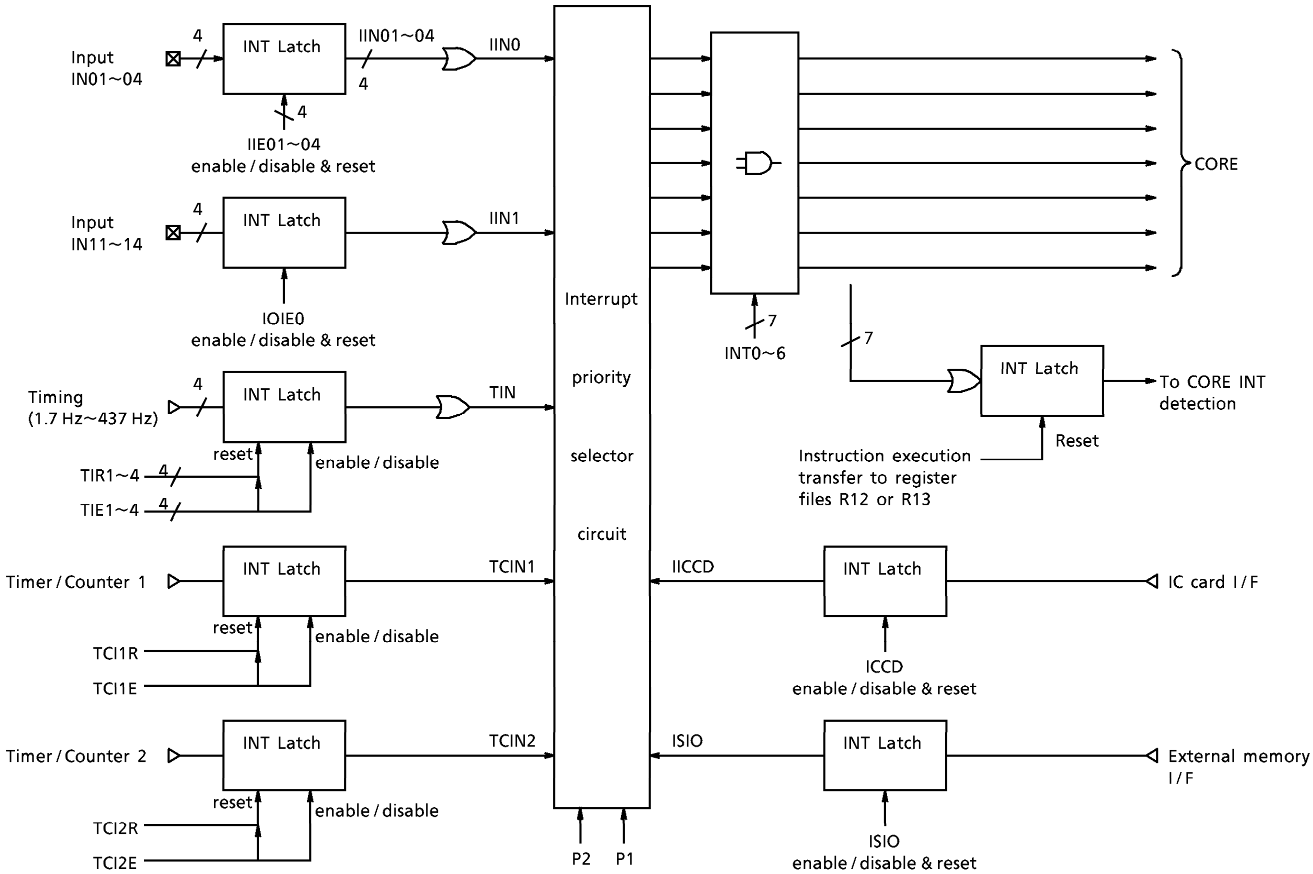


Fig.8 Interruption circuit block

2-1. Input Interruption

(Interruption enable / disable)

	MSB 3	2	1	0 LSB
PC2	IIE04	IIE03	IIE02	IIE01

IIE01 = 0 : IN01 Interruption disable
= 1 : IN01 Interruption enable
IIE02 = 0 : IN02 Interruption disable
= 1 : IN02 Interruption enable
IIE03 = 0 : IN03 Interruption disable
= 1 : IN03 Interruption enable
IIE04 = 0 : IN04 Interruption disable
= 1 : IN04 Interruption enable

IIE01~04 are initially 0 (IN01~04 Interruption disable).

	MSB 3	2	1	0 LSB
PC3	(RIO)	(ISIO)	(IICCD)	IOIE0

IOIE0 = 0 : IN11~14 Interruption disable
= 1 : IN11~14 Interruption enable

IOIE0 is initially 0 (disable).
Interruption enable / disable bit can use as interruption reset.
When the interruption occurs and after recognizing the interruption, it can be resetted by setting IIE01~04 or IOIE0.

(Interruption Data Read)

Interruption Data of IN01~04 can be read by Register file IIN01~04 (PC1R).

	MSB 3	2	1	0 LSB
PC1R	IIN0	IIN03	IIN02	IIN01

Example

LD 42O, 0FH (enable interruption IN01~04)
IN01 interruption occurs.
↓ program goes to the address which is decided by each interruption
LD M, 41O (read IN01~04 interruption)
recognize which interruption is occurred.
↓ (recognize IN01 interruption is occurred.)
LD 42O, 0EH (reset IN01 interruption)
↓
LD 12O, 0FH (enable INT0~2)
↓
LD 13O, 0FH (enable INT3~6)
↓
LD 42O, 0FH (enable IN01~04 interruption)

2-2. Timing Interruption

(Timing Interruption selecting)

Where bit 7 of the 21-bit frequency divider (used to set the input clock) is set to output 3.58 MHz / 2^6 from bit 6 (refer to Fig.7).
The value in parentheses ( ) shows the case where f_L (32 kHz) is set as the input clock of bit 7.
Timing Interruptions are selectable by Register file PD1 as following. PD1 is initially 0H.

	MSB 3	2	1	0 LSB
PD1	1.7 / 3.4	6.8 / 13.5	27 / 55	218 / 437
	(1) / (2)	(4) / (8)	(16) / (32)	(128) / (256)

218 (128) / 437 (256)	= 0	: 218 (128) Hz	INT. select
	= 1	: 437 (256) Hz	INT. select
27 (16) / 55 (32)	= 0	: 27 (16) Hz	INT. select
	= 1	: 55 (32) Hz	INT. select
6.8 (4) / 13.5 (8)	= 0	: 6.8 (4) Hz	INT. select
	= 1	: 13.5 (8) Hz	INT. select
1.7 (1) / 3.4 (2)	= 0	: 1.7 (1) Hz	INT. select
	= 1	: 3.4 (2) Hz	INT. select

(Timing Interruption enable / disable)

Selected Timing Interruption can be controlled enable / disable by Register file TIE1~4 (PD3).
TIE1~4 are initially 0 (disable).
Where bit 7 of the 21-bit frequency divider (used to set the input clock) is set to output 3.58 MHz / 2^6 from bit 6. The value in parentheses ( ) shows the case where f_L (32 kHz) is set as the input clock.

	MSB 3	2	1	0 LSB
PD3	TIE4	TIE3	TIE2	TIE1

TIE1	= 0	: 1.7 (1) Hz or 3.4 (2) Hz	INT. disable
	= 1	: 1.7 (1) Hz or 3.4 (2) Hz	INT. enable
TIE2	= 0	: 6.8 (4) Hz or 13.5 (8) Hz	INT. disable
	= 1	: 6.8 (4) Hz or 13.5 (8) Hz	INT. enable
TIE3	= 0	: 27 (16) Hz or 55 (32) Hz	INT. disable
	= 1	: 27 (16) Hz or 55 (32) Hz	INT. enable
TIE4	= 0	: 218 (128) Hz or 437 (256) Hz	INT. disable
	= 1	: 218 (128) Hz or 437 (256) Hz	INT. enable

(Timing Interruption Reset)

The timing Interruption for the selected timing interruption is reset by register files TIR1 to 4 (PD2W).
TIR1~4 is initially 0. The value in parentheses ( ) shows the case where f_{BCCK} = 32 kHz is set as the input clock (refer to Fig.7).

	MSB 3	2	1	0 LSB
PD2W	TIR4	TIR3	TIR2	TIR1

TIR1 = 1 : 1.7 (1) Hz or 3.4 (2) Hz Interruption reset
TIR2 = 1 : 6.8 (4) Hz or 13.5 (8) Hz Interruption reset
TIR3 = 1 : 27 (16) Hz or 55 (32) Hz Interruption reset
TIR4 = 1 : 218 (128) Hz or 437 (256) Hz Interruption reset

(Timing Interruption Read)

Selected Timing Interruption can be read by Register file TI1~4 (PD0R).
The value in parentheses ( ) shows the case where f_{BCCK} = 32 kHz is set as the input clock.

	MSB 3	2	1	0 LSB
PD0R	TI4	TI3	TI2	TI1

TI1 = 1 : Interruption data of 1.7 (1) Hz or 3.4 (2) Hz
TI2 = 1 : Interruption data of 6.8 (4) Hz or 13.5 (8) Hz
TI3 = 1 : Interruption data of 27 (16) Hz or 55 (32) Hz
TI4 = 1 : Interruption data of 218 (128) Hz or 437 (256) Hz

(Interruption Edge Selection)
TIN Interruption can be selected the reading point (_↑‾ or ‾↓_) by Register file ESELT (PC0-bit 2).
ESTLT is initially 0 (rising EDGE).

	MSB 3	2	1	0 LSB
PC0	(MCLK)	ESELT	(ESELI1)	(ESELI0)

ESELT = 0 Interruption at rising Edge of Timing INT.
= 1 Interruption at down Edge of Timing INT.

Example
LD 51O, 01H (437 Hz, 27 Hz, 6.8 Hz, 1.7 Hz select)
↓
LD 53O, 07H (437 Hz disable, 27 Hz, 6.8 Hz, 1.7 Hz select)
↓ When the 1.7 Hz interruption occurs.
LD M, 50O (read timing interruption)
↓ Recognize 1.7 Hz interruption.
LD 52O, 01H (reset 1.7 Hz interruption)

(Note) : Since a mode transition CPM1 / 3 ↔ CPM2 causes the timing of the binary counters 7-21 to change, timing interrupts also have their timings shifts.

2-3. 8 bits / 16 bits Timer Counter Interruption

When Timer / Counter1, 2 overflow or coincide with setting Time / Count, each Interruption occurs.

	MSB 3	2	1	0 LSB
PE4	(REQT1)	(REQT0)	TCI1E	TCI1R

	MSB 3	2	1	0 LSB
PF4	(LD1)	(LD0)	TCI2E	TCI2R

TCI1E / TCI2E = 1 : Timer / Counter1, 2 Interruption enable
= 0 : Timer / Counter1, 2 Interruption disable
TCI1R / TCI2R = 1 : Timer / Counter1, 2 Interruption reset

TCI1E, TCI2E and TCI2R are initially 0 (disable).

2-4. IC card interface interrupt

An interrupt is triggered at the termination of transmission / reception, or when a parity error occurs at reception.

	MSB 3	2	1	0 LSB
PC3	(RIO)	(ISIO)	IICCD	(IOIE0)

IICCD = 0 : Disables IC card interface interrupt.
= 1 : Enables IC card interface interrupt.

The IICCD initial value is 0 (disable).

2-5. External memory interface interrupt

An interrupt is triggered at the termination of transmission / reception.

	MSB 3	2	1	0 LSB
PC3	(RIO)	ISIO	(IICCD)	(IOIE0)

ISIO = 0 : Disables serial interface interrupt.
= 1 : Enables serial interface interrupt.

The ISIO initial value is 0 (disable).

3. Timer / Counter

The Timer / Counter circuit can use as 8 bit × 2 channel or 16 bit × 1 channel Timer / Counter. And there Time / Counter can be used as general purpose Timer / Counter, Watch Dog Timer, or Multi Interruption Timer.
8 bits / 16 bits can be switched by Register file TCPS (PF2-bit3). And input frequency also can be choosed by Register CKS11~13 (PE2-bit0, 1, 2) and CKS21~23 (PF2 -bit0, 1, 2), as follows.

	MSB 3	2	1	0 LSB
PE2	(MRIO)	CKS13	CKS12	CKS11

	MSB 3	2	1	0 LSB
PF2	TCPS	CKS23	CKS22	CKS21

CKS11	CKS12	CKS13	Input Frequency for Timer Counter1 (f_H = 3.58 MHz, f_L = 32 kHz) The value in parentheses ( ) shows the case where low-speed OSC is selected as f_{BCK} clock.			
0	0	0	$f_H / 2^{21}$	$(f_L / 2^{15})$	1.7 Hz	(1.0 s)
1	0	0	$f_H / 2^{12}$	$(f_L / 2^{6})$	874 Hz	(2.0 ms)
0	1	0	$f_H / 2^{8}$	$(f_L / 2^{2})$	14 kHz	(125 μs)
1	1	0	$f_H / 2^{3}$		448 kHz	
—	—	1	OFF			

CKS21	CKS22	CKS23	Input Frequency for Timer Counter2 (f_H = 3.58 MHz, f_L = 32 kHz)			
0	0	0	$f_H / 2^{15}$	$(f_L / 2^{9})$	109 Hz	(16 ms)
1	0	0	$f_H / 2^{9}$	$(f_L / 2^{3})$	7 kHz	(250 μs)
0	1	0	$f_H / 2^{5}$		112 kHz	
1	1	0	$f_H / 2^{2}$		895 kHz	
—	—	1	OFF			

TCPS = 0 : 8 bit × 2 channel Timer / Counter
= 1 : 16 bit × 1 channel Timer / Counter

(When Timer / Counter is used as 16 bits timer, TIMER2 is used as lower bits.
And CKS11~13 are ignored. Input Frequency is decided by CKS21~23.)

CKS11~13, CKS21~23, TCPS are initially 0.

(Timer / Counter1 : 1Hz, Timer / Counter2 : 109 (64) Hz, 8 bit × 2 channel)
The value in parentheses ( ) shows the case where f_{BCCK} = 32 kHz.

(Note) : 448 kHz of Timer / Counter1, 895 kHz, 112 kHz of Timer / Counter2 can be used when High-speed OSC is on.

Timer function can be selected by Register file WDT1 (PE3-bit0) and CMPEN1 (PE3-bit1), 2 (PF3-bit1).
Timer / Counter1 can be used as Watch Dog Timer.
And Input Frequency can be controlled by Register file TC1EN (PE3-bit3) and TC2EN (PF3-bit3).
Timer / Counter is resetted by Register file TC1R (PE3-bit2), TC2R (PF3-bit2).

	MSB 3	2	1	0 LSB
PE3	TC1EN	TC1R	CMPEN1	WDT1
	R / W	W	R / W	R / W

	MSB 3	2	1	0 LSB
PF3	TC2EN	TC2R	CMPEN2	(SELCLK)
	R / W	W	R / W	R / W

Set timer/counter 1 using PE3.
Set timer/counter 2 using PF3.
The initial value for both PE3 and PF3 is all bits set to 0.

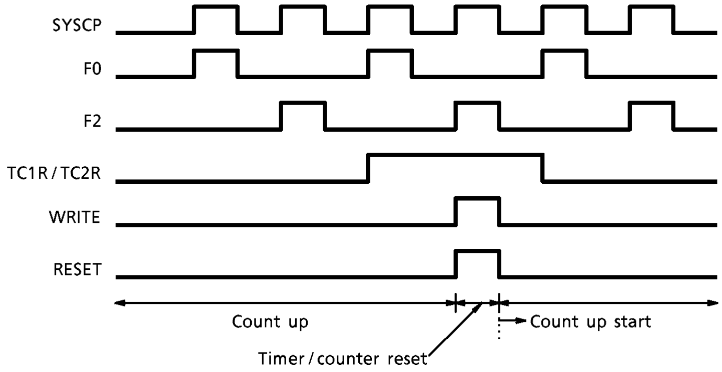
PE3

WDT1	= 0 :	Functions as an 8-bit timer / counter.
	= 1 :	Functions as a watchdog timer.
CMPEN1	= 0 :	When the timer / counter 1 overflows, an interrupt occurs. (Note that when WDT1 = 1, the whole system is reset.)
	= 1 :	When TCR11 to TCR18 match SET11 to SET18, an interrupt occurs. (Note that when WDT1 = 1, the whole system is reset.)
TC1R	= 1 :	Timer / Counter1 reset (Counter clear) Restart counting after the reset. (The timing is shown below.)
TC1EN	= 0 :	Timer / Counter1 Input Frequency disable
	= 1 :	Timer / Counter1 Input Frequency enable

PF3

CMPEN2	= 0 :	When Timer / Counter2 overflows, an interrupt occurs.
	= 1 :	When TCR21 to TCR28 match SET21 to SET28, an interrupt occurs.
TC2R	= 1 :	Timer / Counter2 reset (Counter clear) Restart counting after the reset. (The timing is shown below.)
TC2EN	= 0 :	Timer / Counter2 Input Frequency disable
	= 1 :	Timer / Counter2 Input Frequency enable

Timing chart for timer / counter 1 / 2 reset



Timer / Counter1, 2 data can read from Register file TCR11～18 and TCR21～28.

	MSB 3	2	1	0 LSB
PE0R	TCR14	TCR13	TCR12	TCR11
PE1R	TCR18	TCR17	TCR16	TCR15
PF0R	TCR24	TCR23	TCR22	TCR21
PF1R	TCR28	TCR27	TCR26	TCR25

Timer / Counter1, 2 Comparison data is set by Register file SET11～18 and SET21～28.

	MSB 3	2	1	0 LSB
PE0W	SET14	SET13	SET12	SET11
PE1W	SET18	SET17	SET16	SET15
PF0W	SET24	SET23	SET22	SET21
PF1W	SET28	SET27	SET26	SET25

SET11～18 and SET21～28 are initially 0.

(Note 1) : When generating an interrupt for the timer / counter by comparing it with the setup value (SET11-18, SET21-28) or resetting the system, set the setup values in register files SET11-18 and SET21-28 before enabling CMPEN1 and 2.

(Note 2) : When generating an interrupt by a 16-bit timer by comparing it with the setup value, enable all of CMPEN1, CMPEN2, TC1EN, and TC2EN using instructions.

(Note 3) : Since the setup values and timer / counter values both are 0 after initialization, an interrupt is generated or the system is reset immediately when CMPEN1 is enabled.

(Note 4) : Since a mode transition CPM1 / 3 ↔ CPM2 causes the timing of the binary counters 7-21 to change, the timer / counters also have their timings shifts.

(Note 5) : Do not change the timer / counter from 8 bits to 16 bits in the middle of operation after the timer / counter has started counting, because such a change could cause the data to be destroyed.

4. I / O PORT (Refer to Fig.9)

JTMP04020-XXXS has 8 input ports and 12 I / O ports.
8 input ports have Interruption.

4.1 INPUT (IN01~04)

Each input data can be read by Register file IND01~IND04.

	MSB 3	2	1	0 LSB
PA0R	IND04	IND03	IND02	IND01

Each input Interruption function can be set enable / disable by Register file IIE01~04.

	MSB 3	2	1	0 LSB
PC2	IIE04	IIE03	IIE02	IIE01

IIE01~04 = 0 : IN01~IN04 each Interruption disable
= 1 : IN01~IN04 each Interruption enable

(Note) : IIE01 to IIE04 interrupt disable / enables are register files that are effective when rising-edge interrupts are selected.
When level interrupts are selected, interrupts are disabled / enabled by the data input from ports. In this case, therefore, interrupts cannot be disabled / enabled by the register files.

Interruption data can be read by Register file IIN01~04.

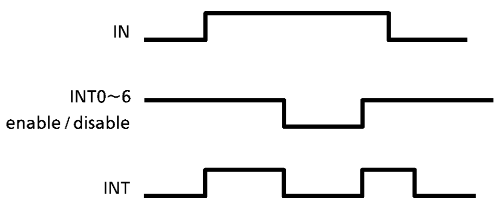
	MSB 3	2	1	0 LSB
PC1R	IIN04	IIN03	IIN02	IIN01

(Note) : Interrupt data IN11 to IN14 cannot be read out. Only the data input from ports can be read out. (Refer to Fig.8.)
Interrupt timings (rising edge / level) can be selected using register file ESELI0.

	MSB 3	2	1	0 LSB
PC0	(MCLK)	(ESELT)	(ESELI1)	ESELI0

ESELI = 0 IN01~04 : Interruption at rising edge of input INT.
= 1 IN01~04 : High level of input INT .

Input level-triggered interrupts are possible when ESELI0 = 1. In this case, if interrupts have been enabled by register files INT0~6, the interrupt remain asserted while the input level is high.



Input ports (IN11~IN14)

The input data can be read out via register files IND11~IND14.

	MSB 3	2	1	0 LSB
PA1R	IND14	IND13	IND12	IND11

IN11 to IN14 have an interrupt facility, so that interrupts can be disabled / enabled by register file IOIE0. (Four interrupt sources are collectively disabled / enabled by IOIE0.)

	MSB 3	2	1	0 LSB
PC3	(RIO)	(ISIO)	(IICCD)	IOIE0

IOIE0 = 0 : IN11~IN14 are disabled.
= 1 : IN11~IN14 are enabled.

(Note) : The IN11~IN14 interrupt disable / enables are the register files that are effective when rising-edge interrupts are selected.
When level interrupts are selected, interrupts are disabled / enabled by the data input from ports. In this case, therefore, interrupts cannot be disabled / enabled by the register files.
The interrupt data IN11~IN14 cannot be read out. Only the data input from ports can be read out. (Refer to Fig.8.)

Interrupt timings of IN11~14 (rising edge / level) can be selected using register file ESELI1.

	MSB 3	2	1	0 LSB
PC0	(MCLK)	(ESELT)	ESELI1	(ESELI0)

ESELI1 = 0 : IN11~IN14 are rising edge-triggered.
= 1 : IN11~IN14 are level-triggered.

Input level-triggered interrupts are possible when ESELI1 = 1. In this case, if interrupts have been enabled by register files INT0~6, the interrupt remain asserted while the input level is high.

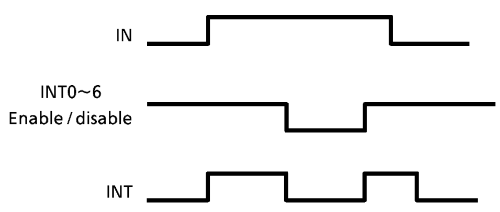


Fig.9 Level-triggered interrupts

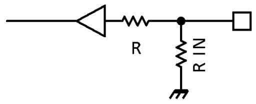
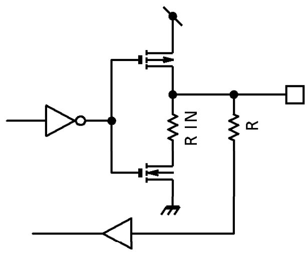
4-2. I / O ports (IO01~IO04, IO11~IO14, IO21~IO24)

Each input data can be read by following Register file, when using input port.

	MSB 3	2	1	0 LSB
R14R	IOD1	IOD13	IOD12	IOD11
R15R	IOD2	IOD23	IOD22	IOD21
PE6R	IOD0	IOD03	IOD02	IOD01

When using each input / output port for output, the output data can be set using the register file shown below.

	MSB 3	2	1	0 LSB
R14W	IOO14	IOO13	IOO12	IOO11
R15W	IOO24	IOO23	IOO22	IOO21
PE6W	IOO04	IOO03	IOO02	IOO01

	Input / Output Circuit
IN01~IN04 IN11~IN14	
IO01~IO04 IO11~IO14 IO21~IO24	

RIN : Internal pull-down resistor
Typ. = 100 kΩ
R : Input protective resistor
Typ. = 100 Ω

Fig.10 Structure of input / output port

At initialization, Nch of this port is set to ON and the port is set to a 100 kΩ pull-down input (low output). When using this port as an input pin, be sure to set the output registers (R14W to R15W, RE6W) to 0.

5. Buzzer Circuit

Buzzer sound can be selected by Register file BZ1, BZ2, BZ3 and 3.5 k (2 k) / 7 k (4 k). The value in parentheses ( ) shows the case where bit 7 of the 21-bit frequency divider is set to a low-speed clock.

	MSB 3	2	1	0 LSB
PE7	3.5k / 7k (2k / 4k)	BZ3	BZ2	BZ1

3.5 k (2 k) / 7 k (4 k) = 0 Basic frequency 3.5 kHz (2 kHz)
= 1 Basic frequency 7 kHz (4 kHz)
The initial value is 0.

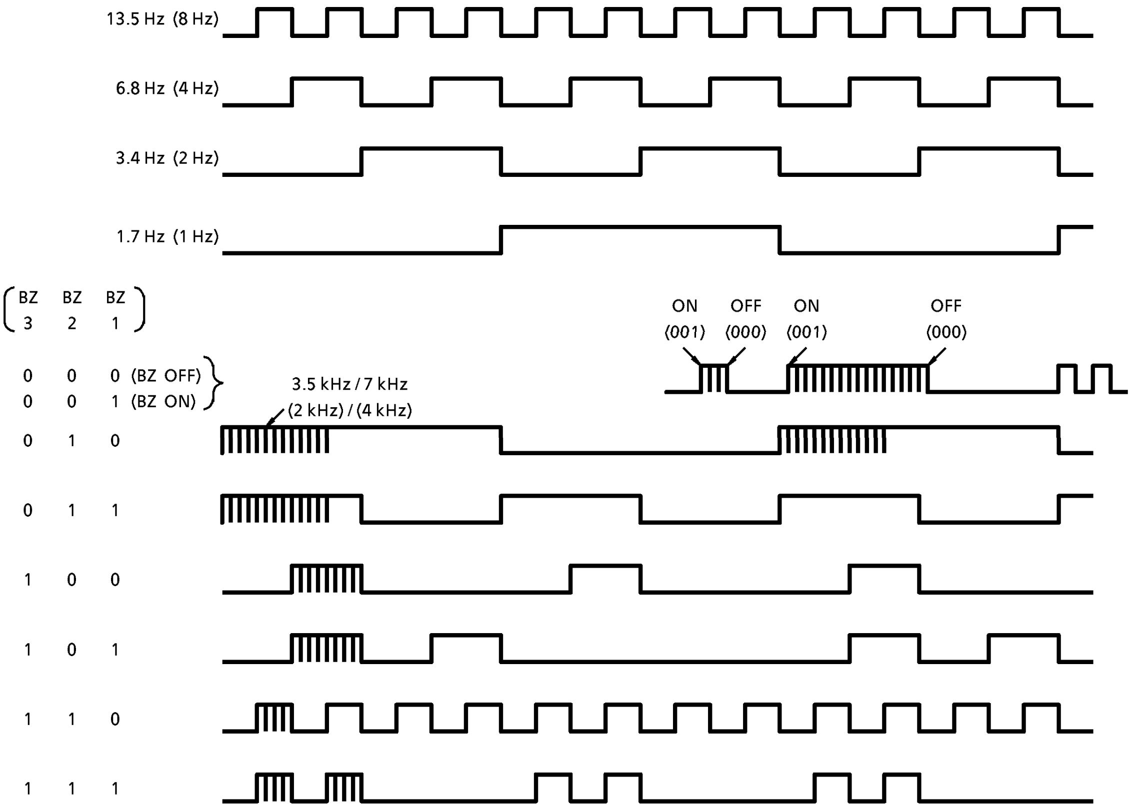


Fig.11 Buzzer sound

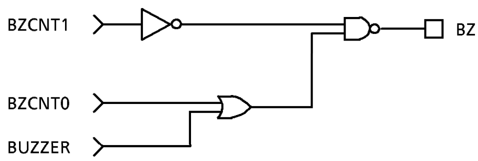
BZ sound can be made by software using (000), (001) setting, as above.
When the Register file R67 is set the above ((BZ3, BZ2, BZ1) = (010)~(111)), each BZ sound is continuously released setting (BZ3, BZ2, BZ1) to (000).

The buzzer output pin can be forcibly fixed to any level.

	MSB 3	2	1	0 LSB
PC7	BZCNT1	BZCNT0	(P2)	(P0)

Initial value = 0

BZCNT1	BZCNT0	
0	0	No forced control
0	1	Forced low output
1	0	Forced high output



6. LCD Circuit

The LCD driver circuit has common signals and segment signals to drive, 1 / 8 or 1 / 16 duty, 1 / 4 bias LCD.

Duty can be set to 1 / 8 or 1 / 16 by mask option.

Duty	Frame Frequency	COMMON	SEGMENT
1 / 8	97.5 Hz	COM1~COM8	S1~S42
1 / 16	97.5 Hz	COM1~COM16	S1~S34

The LCD driver circuit is controlled by Register file both DSTA and DON, and Display RAM is enable on DRCE = 1.

	MSB 3	2	1	0 LSB
PC6	(32KOUT)	DRCE	DON	DSTA

The initial value is 0.

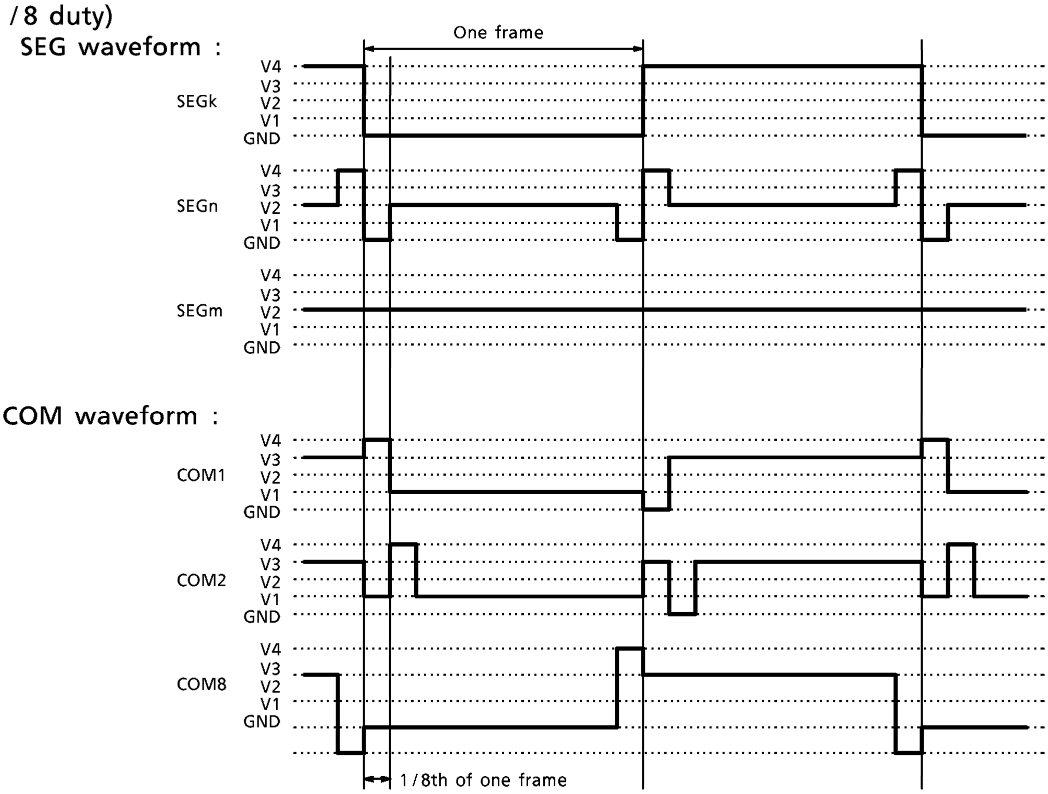
DSTA = 0 : All of COMMON and SEGMENT are fixed DGND level.
= 1 : enable normal Display
DON = 0 : Quadrupler OFF
= 1 : Quadrupler ON
DRCE = 1 : Display RAM enable

(Note 1) : Display signals from segment and common are mode by the clock which come from low- speed oscillation. Even though the high-speed oscillator may be operating no display is output unless the low-speed oscillator is operating.

(Note 2) : Register file DON and DSTA are read to Display Driver circuit by the clock which is made by LOWCP.
When the LOWCP is needed OFF it is needs max. 103 ms after changing the data of DON and DSTA.

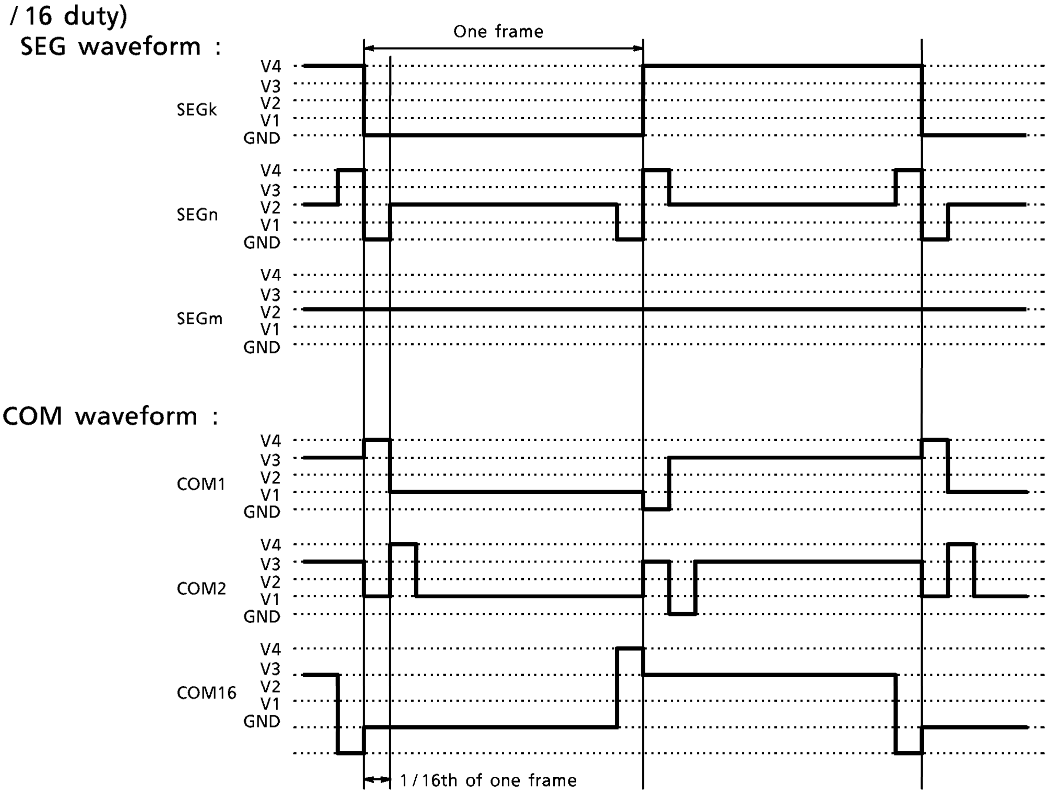
LCD SDE / COM waveform

(1 / 8 duty)



(*) SEGk : All on
SEGn : COM1 and COM8 on
SEGm : All off

(1 / 16 duty)



(*) SEGk : All on
SEGn : COM1 and COM16 on
SEGm : All off

LCD contrast control

The LCD regulator VLC4 level can be adjusted to one of seven levels.

	MSB 3	2	1	0 LSB
R16W	—	LVLC2	LVLC1	LVLC0
		0	0	0

Initial value = 0

LVLC2	LVLC1	LVLC0	LVC4 level (@VLC = 4.7 V)
0	0	0	—
0	0	1	4.7 V
0	1	0	4.6 V
0	1	1	4.5 V
1	0	0	4.4 V
1	0	1	4.3 V
1	1	0	4.2 V
1	1	1	4.1 V

(Note 1) : Note that register R16 cannot be read.

(Note 2) : When register R16 is set to 0 and the display is turned ON, the LCD does not output the normal waveform.

Pin 32KOUT circuit

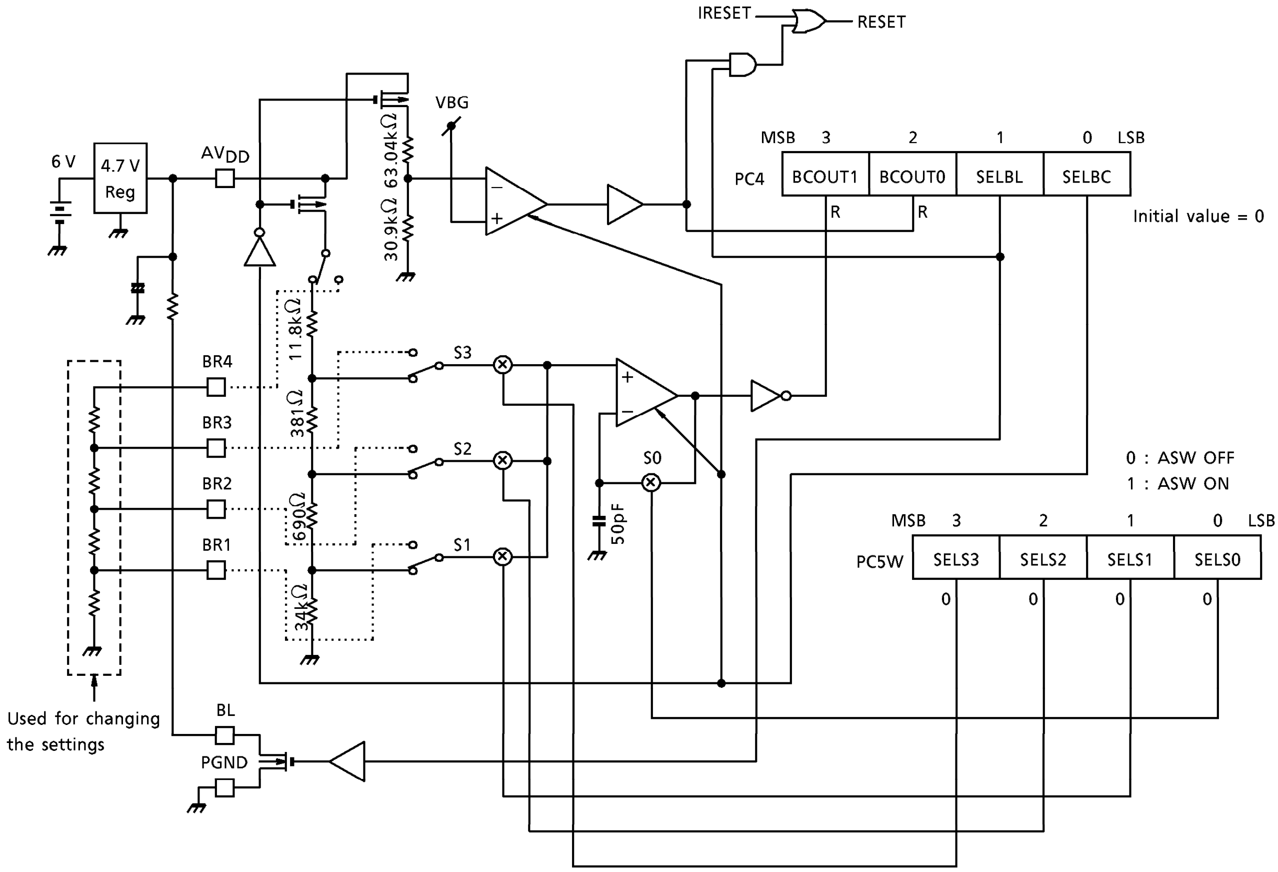
This pin can output low-speed oscillation.

	MSB 3	2	1	0 LSB
PC6	32KOUT	(DRCE)	(DON)	(DSTA)

Initial value = 1

32KOUT = 0 : Fixed to low level
= 1 : Outputs low-speed oscillation

7. Battery Check Circuit



The above diagram shows the structure of the battery check circuit.

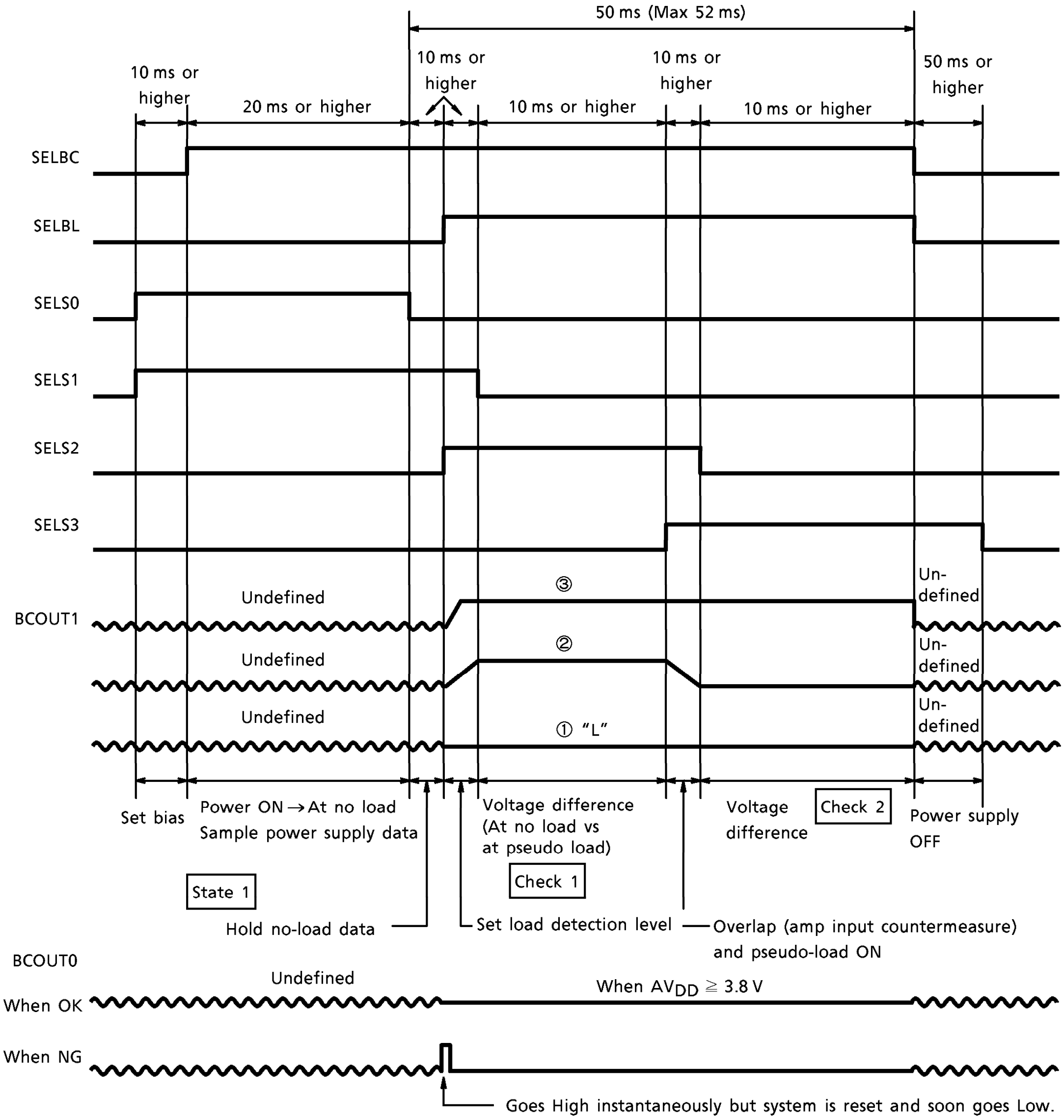
≪Description of Operation≫

- Outline

At IC card communication the battery check circuit can identify three levels of battery voltage difference between no load and pseudo load by checking the relative value using BCOUT1. These levels are : up to 100 mV, 100 to 150 mV, and 150 mV and higher. This function is useful for checking the battery capacity before communication starts. In addition, absolutevalue detection (BCOUT0) can also be performed at the level of AVDD = 3.8 V (design standard 3.2 to 4.35 V).

If BCOUT0 = 0, battery OK.
If BCOUT0 = 1, battery NG.

- Operating timing



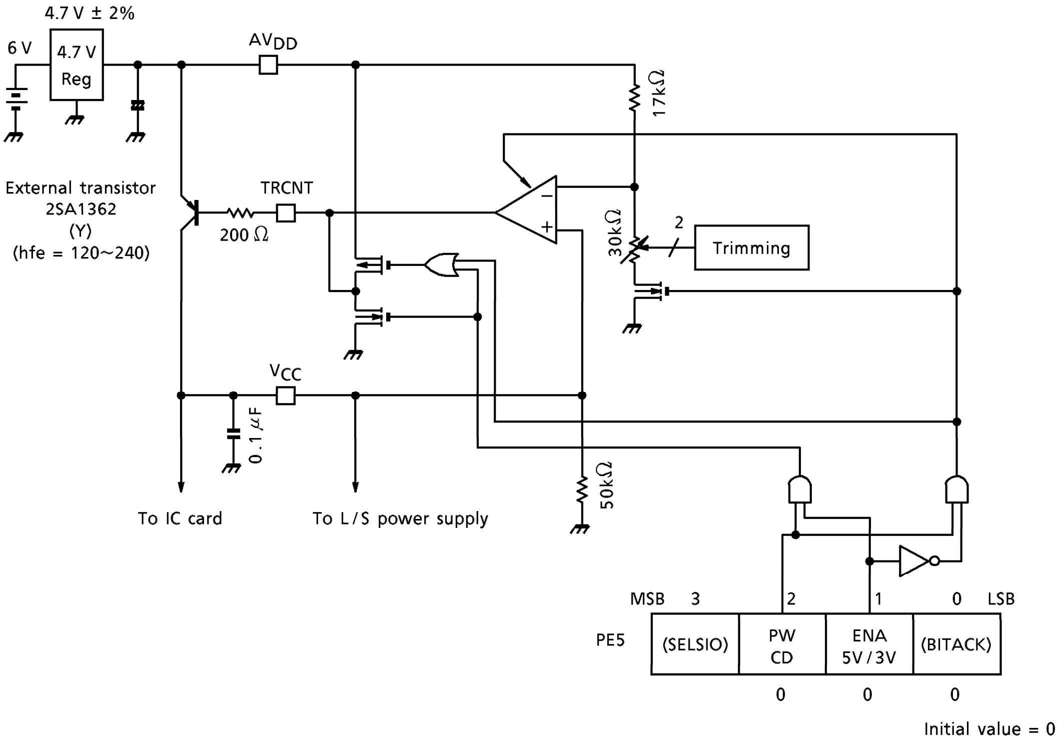
Monitoring BCOUT1 and identifying as below (relative check)

Check 1	Check 2	OVERALL RESULT	STATE
0	0	When pseudo current is loaded, no power supply voltage fluctuation (up to 100 mV). (The battery can be used for IC card communication.)	①
1	0	When pseudo current is loaded, the power supply voltage fluctuates slightly (100 mV to 150 mV). (Battery change required.)	②
1	1	When pseudo current is loaded, the power supply voltage fluctuates significantly. (150 mV or higher). (The battery cannot be used for IC card communication.)	③

The Check 1 and 2 times can be set as desired, but the total time must not exceed 50 ms.

(Note) : After 20 ms of State 1, during absolute value detection, the value can be read from BCOUT0 when no load is applied (SELBL = 0). However, when a load is applied (SELBL = 1), the system is reset and the value cannot be read.

8. 3 V / 4.7 V Regulator



Operating States

PWCD	ENA5V / 3V	TRCNT	V_{CC}
0	*	4.7 V	0 V
1	0	External transistor base control using a 3 V regulator	3 V
	1	0 V	4.7 V

(*) : indicates can be set to 0 or 1.

ENA5V / 3V = 0 : 3 V supported (PWCD = 1)

ENA5V / 3V = 1 : 4.7 V supported (PWCD = 1)

As shown in the above table, the 3 V / 4.7 V regulator can be controlled by adjusting ENA5V / 3V and PWCD.

(Note 1) : Write a program to change to 4.7 V communication if no reply is received to an initial 3 V communication.

(Note 2) : When writing the program, note that the MSB (SELSIO) and LSB (BITACK) are physically different bits.

9. IC Card Interface

The IC card interface supports the T = 0, T = 1 transmit / receive protocol based on JIS regulations. (This interface cannot be used at the same time as the external memory interface circuit described later.)
IC card communication is supported only in CPM2 and CPM3 modes. (Only when SYSCP is set as a high-speed clock.)

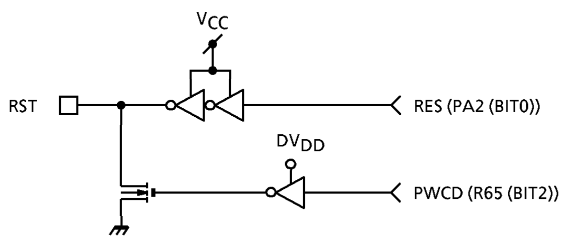
The power supply to the IC card is controlled by the 3 V / 4.7 V regulator described above (using register file PE5).
The 3 V or 4.7 V is supplied to the IC card from the VCC pin. (See the application circuit, including the external transistor).

① RST : This pin outputs reset requests to the IC card. Control the pin using register file RES.

	MSB 3	2	1		0 LSB
PA2	(CONTCLK)	(ENACLK)	(IODATA)	(CONTIO)	RES

Initial value = 0

The RST pin is a CMOS output.



(Note) : When V_{CC} is OFF, the RST pin outputs a Low signal.

② CLK : This pin outputs a clock to the IC card. Control the pin using register files SELCLK, ENACLK, and CONTCLK.

	MSB 3	2	1	0 LSB
PF3	(TC2EN)	(TC2R)	(CMPEN2)	SELCLK

Initial value = 0

Clock output is determined (f_{CLK} is selected) by setting SELCLK = 0 for 3.58 MHz (f_H) or SELCLK = 1 for 1.79 MHz (f_H / 2).

	MSB 3	2	1		0 LSB
PA2	CONTCLK	ENACLK	(IODATA)	(CONTIO)	(RES)

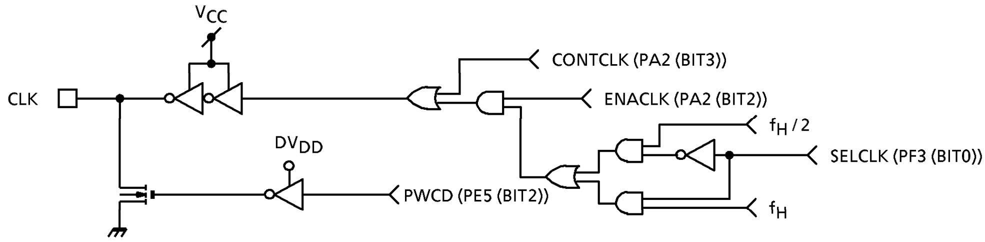
Initial value = 0

Output is enabled / disabled using ENACLK and CONTCLK.

CONTCLK	ENACLK	CLK OUTPUT
0	0	Forced low output
0	1	Output the selected CLK (f_{CLK})
1	0	Forced high output

(Note) : When V_{CC} is off, CLK pin outputs a Low signal.
(*) : When CONTCLK = 1, the CLK pin functions as a forced high output regardless of the ENACLK signal.

The CLK pin is a CMOS output.



③ I / O : This pin transmits/receives data to/from the IC card.
The IC card interface circuit also functions as the external memory interface circuit. Initially, select either IC card interface or external memory interface communication. Use the following register file (PE5) for the selection.

	MSB 3	2	1	0 LSB
PE5	SELSIO	(PWCD)	(ENA5V / 3V)	(BITACK)

Initial value = 0

SELSIO = 0 selects IC Card Communication mode. SELSIO = 1 selects External Memory Communication mode.

	MSB 3	2	1	0 LSB
PA2	(CONTCLK)	ENACLK	IODATA ⋮ CONTIO	(RES)

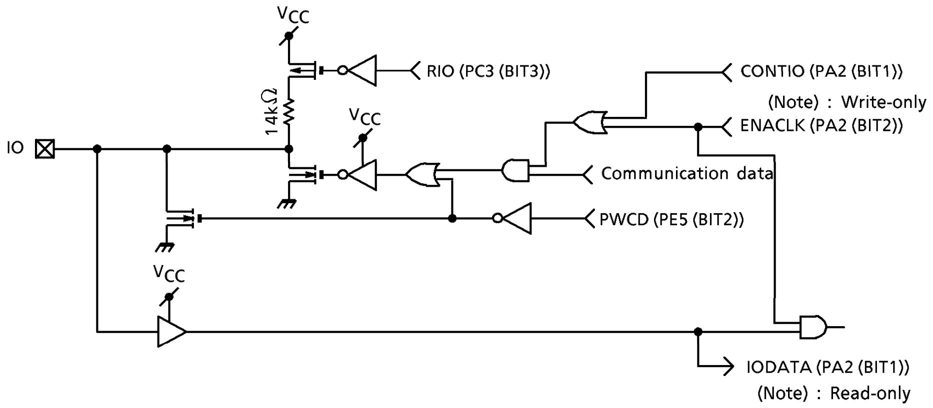
Initial value = 0

ENACLK	CONTIO	I / O OUTPUT
0	0	Forced low output
0	1	Forced high output
1	1	Output data of communication register

Bit 1 of PA2 is used as CONTIO when writing the I / O pin control setting and also as IODATA when reading the I/O pin status.

(Note 1) : When V_{CC} is OFF, the I / O pin outputs a Low signal.
(Note 2) : Before turning V_{CC} ON, first set ENACLK (bit 2 of PA2) and CONTIO (bit 1 of PA2).
(Note 3) : When ENACLK = 1, the I / O pin outputs the data in the communications register regardless of the CONTIO signal.

The I/O pin is an Nch open drain output (with programmable pull-up resistor). The I/O pin input is a CMOS inverter input.



Control the IC card data transfer clock (fCDSCK) using the following register file.

	MSB 3	2	1	0 LSB
PA3	FCLK3	FCLK2	FCLK1	FCLK0

Initial value = 0

FCLK3	FCLK2	FCLK1	FCLK0	Transfer clock (f_{CDSCK})
0	0	0	0	$f_{CLK} \times \frac{1}{186 \times 2}$ (1/372)
0	0	0	1	$f_{CLK} \times \frac{1}{186 \times 3}$ (1/558)
0	0	1	0	$f_{CLK} \times \frac{1}{186 \times 4}$ (1/744)
0	0	1	1	$f_{CLK} \times \frac{1}{186 \times 6}$ (1/1116)
0	1	0	0	$f_{CLK} \times \frac{1}{186 \times 8}$ (1/1488)
0	1	0	1	$f_{CLK} \times \frac{1}{186 \times 10}$ (1/1860)
1	0	0	0	$f_{CLK} \times \frac{1}{256 \times 2}$ (1/512)
1	0	0	1	$f_{CLK} \times \frac{1}{256 \times 3}$ (1/768)
1	0	1	0	$f_{CLK} \times \frac{1}{256 \times 4}$ (1/1024)
1	0	1	1	$f_{CLK} \times \frac{1}{256 \times 6}$ (1/1536)
1	1	0	0	$f_{CLK} \times \frac{1}{256 \times 8}$ (1/2048)

(Note) : The clock is supplied from the high-speed oscillator.

The following shows the interfaces in IC Card Communication mode and External Memory Communication mode.

		SELSIO		
		0	1	
			V_{CC} output state	V_{CC} OFF state
IC card interface	CLK	Controllable by PA2	Controllable by PA2	Low output
	RST	Controllable by PA2	Controllable by PA2	Low output
	I/O	IC card communication	High output (pulled-up)	Low output
External memory interface	SCL	Hiz output	External memory communication	External memory communication
	SDA	Hiz output	External memory communication	External memory communication

The following IC card control register controls the IC card transmission/reception.
SELT switches between T = 0 (resend request) and T = 1 (no resend request).

	MSB 3	2	1	0 LSB
PA4	SELT	(DTPB)	(RTST)	(CDST)

Initial value = 0

The following register file stores information on whether the transmit / receive data have even or odd parity. (Used for parity check by hardware at transmission / reception.)

	MSB 3	2	1	0 LSB
PA4	(SELT)	DTPB	(RTST)	(CDST)

Initial value = 0

DTPB = 0 indicates even parity. DTPB = 1 indicates odd parity. CDST controls the data transmission.

	MSB 3	2	1	0 LSB
PA4	(SELT)	(DTPB)	(RTST)	CDST

Initial value = 0

When CDST = 0, transmission stops. When CDST = 1, transmission starts (is in progress). The lower four bits of the transfer data are read from / written to SIO data register 1. The upper four bits of the transfer data are read from/written to SIO register 2.

(Note): After start of transmission:
Because CDST is controlled by hardware data write by software is disabled except when transmission is forcibly stopped.

The following shows the writing of the transmit data and the reading of the receive data.

	MSB 3	2	1	0 LSB	
PF6	SID7	SID6	SID5	SID4	SIO register 2
PF7	SID3	SID2	SID1	SID0	SIO register 1

Initial value = 0

(Note) : The upper 4 bits of transfer data should be captured into PF6 and the lower 4 bits of transfer data should be captured into PF7. Thus any attempt of byte-accessing this register (i.e. attempt to capture all the 8 bits of transfer data at a time) would result in incorrect order of the upper and lower 4 bits.

The parity in the transmit data is checked by hardware and determined.

(Note) : The transmit data support MSB-first communication only.

Retries by resend requests when T = 0 (resend request) can be forcibly stopped.

	MSB 3	2	1	0 LSB
PA4	(SELT)	(DTPB)	RTST	(CDST)

Initial value = 0

When RTST = 0, communication is enabled. When RTST = 1, communication is forcibly stopped.

At transmission

Writing 1 to RTST at data transmission forcibly stops the transmissionand sets the device to a WAIT state.
That is, the next transmission can start even if all the data of the specified length are not sent. At that time, RTST is cleared to 0 by hardware.

At reception

Writing 1 to RTST at data reception forcibly ends Receive mode and sets the device to a wait. That is, the next communication can start even if the specified transmit length is not yet complete. In this case, RTST is set to 0 by hardware.

LD0, LD1 of register PF4 select the transfer length for both reception and transmission.

PF4	MSB 3	2	1	0 LSB
	LD1	LD0	(TCI2E)	(TCI2R)

Initialized to 0

The following describes the various signal output times by transfer length at both reception and transmission.
(For details on output timing, see the IC card interface timing chart on Page 51 and 53.)

At transmission

Check at the 11 etu point to see whether a resend request signal is sent from the card as a result of a data transmission when T = 0 (indicates a resend request).

The following table shows the transmission format by transfer length.

LD1	LD0	Transmit length	T = 0: Character protection time	T = 0: Resend request check point	T = 0: Transmission complete interrupt point	T = 1: Character protection time	T = 1: Transmission complete interrupt point
0	0	13 etu	3.0 etu	11.0 etu	12.5 etu	3.0 etu	12.5 etu
0	1	12 etu	2.0 etu	11.0 etu	11.5 etu	2.0 etu	11.5 etu
1	0	11 etu	1.0 etu	—	10.5 etu	1.0 etu	10.5 etu

(Note 1) : Parity bits are set for transmission every time resend is requested.

(Note 2) : When 11 etu is selected, set SELT (PA4, (bit 3)) to 1 (T = 1). That is, when SELT = 1, do not set LD1 to 1.

At reception

The resend request output time by the data reception side when T = 0 (indicates a resend request) can be selected among four types from 0 to 2 etu in 0.5-etu steps (depending on the transfer length).

PE4	MSB 3	2	1	0 LSB
	REQT1	REQT0	(TCI1E)	(TCI1R)
	R/W	R/W	R/W	R

Initial value = 0

REQT1	REQT0	Resend request output time: Transfer length = 12 etu	Resend request output time: Transfer length = 13 etu
0	0	0 etu	0 etu
0	1	1.0 etu	1.0 etu
1	0	1.0 etu	1.5 etu
1	1	1.0 etu	2.0 etu

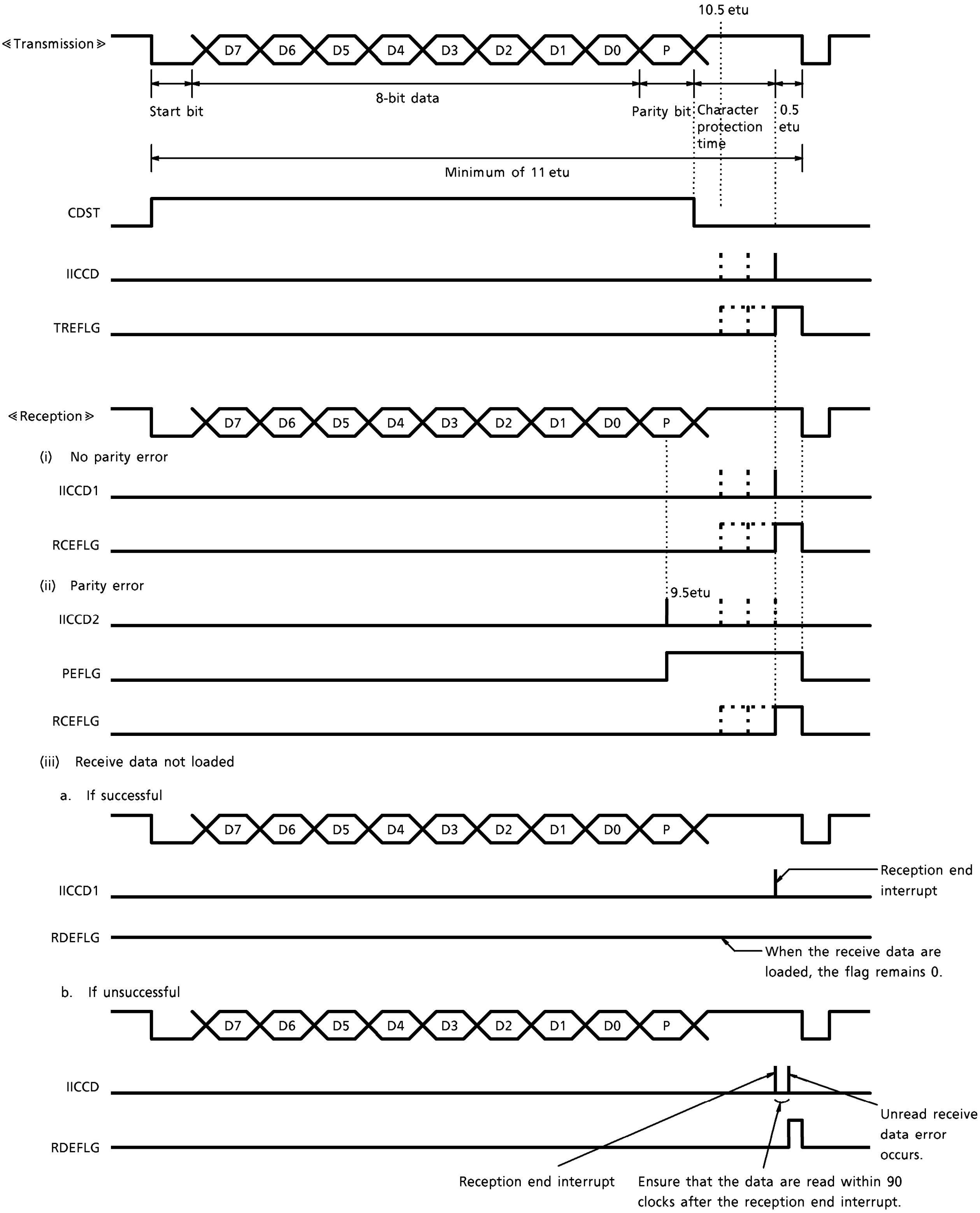
The following table shows the reception format by transfer length.

LD1	LD0	Transmit length	T				
			0			1	
			Character protection time	Resend request signal output time	Reception complete interrupt point	Character protection time	Reception complete interrupt point
0	0	13 etu	3.0 etu	0 to 2.0 etu (0 to 2 etu selectable)	12.5 etu	3.0 etu	12.5 etu
0	1	12 etu	2.0 etu	0 etu or 1.0 etu (0 or 1 etu selectable)	11.5 etu	2.0 etu	11.5 etu
1	0	11 etu	1.0 etu	—	10.5 etu	1.0 etu	10.5 etu

(Note 1) : When T = 0, the resend request signal output time can be adjusted only when 13 etu is selected as the transfer length.

(Note 2) : When 11 etu is selected, set SELT (PA4, (bit 3)) to 1 (T = 1).
That is, when SELT = 1, do not set LD1 to 1.

T = 1


10.5 etu
≪Transmission≫
D7 D6 D5 D4 D3 D2 D1 D0 P
Start bit
8-bit data
Parity bit
Character protection time
0.5 etu
Minimum of 11 etu
CDST
IICCD
TREFLG
≪Reception≫
(i) No parity error
IICCD1
RCEFLG
(ii) Parity error
9.5etu
IICCD2
PEFLG
RCEFLG
(iii) Receive data not loaded
a. If successful
IICCD1
Reception end interrupt
RDEFLG
When the receive data are loaded, the flag remains 0.
b. If unsuccessful
IICCD
RDEFLG
Unread receive data error occurs.
Reception end interrupt
Ensure that the data are read within 90 clocks after the reception end interrupt.

At transmission : At the completion of transmission (on confirmation of the STOP bit at 0.5 etu before the specified transmit length) an interrupt occurs. This sets the transmission end flag TREFLG. This flag is initialized (cleared to 0) on the falling edge of the start bit. The data should be processed within 0.5 etu. The resended from card is set to automatic resend. Count number of resends by program.

At reception : An interrupt source is not known when one of the following interrupts occurs. Therefore, identify the source by reading register PA5:

* When a parity error (at the 9.5 etu point) interrupt occurs <PEFLG>
* When a reception end interrupt (on confirmation of the STOP bit at 0.5 etu before the specified receive length) occurs <RCEFLG>
* When an interrupt occurs As the write source is unknown when an interrupt occurs, read the PA5 register to confirm the write source. (the next data reception started before the received data were read). <RDEFLG>

	MSB 3	2	1	0 LSB
PA5	TREFLG	RCEFLG	PEFLG	RDEFLG

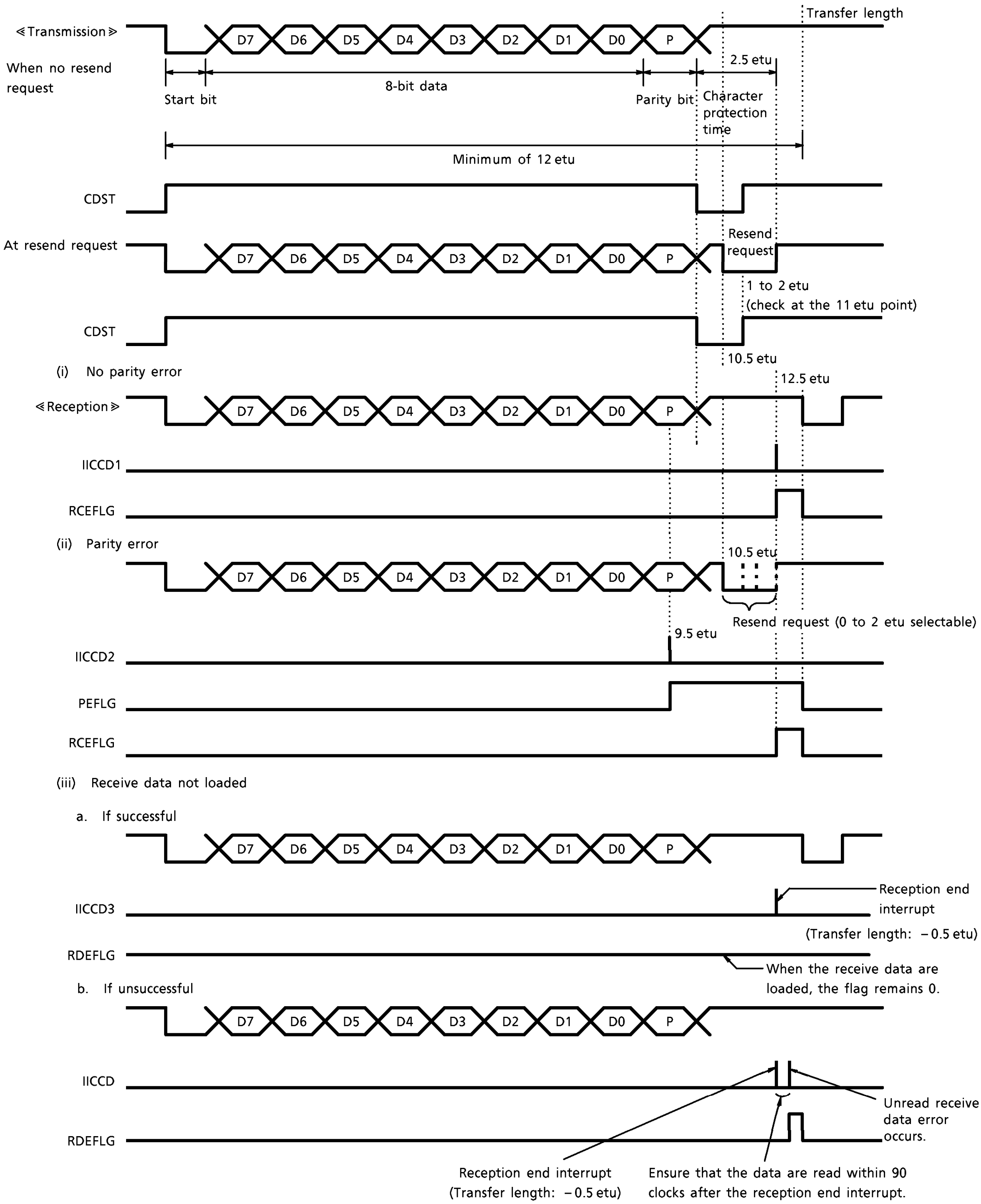
Initial value = 0

Even if 0 is written to initialize register PA5, the TREFLG, the RCEFLG, the PEFLG, and the RDEFLG flags retain the previous data up to the end of the communication. Accordingly, initialize this register only after the completion of the communication.

As interrupts from the IC card interface occur at the end of transmission, at the end of reception, at the occurrence of a parity error, or when reception data are not fully loaded, first confirm the interrupt then confirm the cause of the interrupt using the flag corresponding to the interrupt.

T = 0

At transmission, detects whether there is a resend request within 11 etu. If a request is detected, the same data are resent after a minimum of 12 etu. The resend can be forcibly stopped by setting bit RTST of register file PA4 to high.



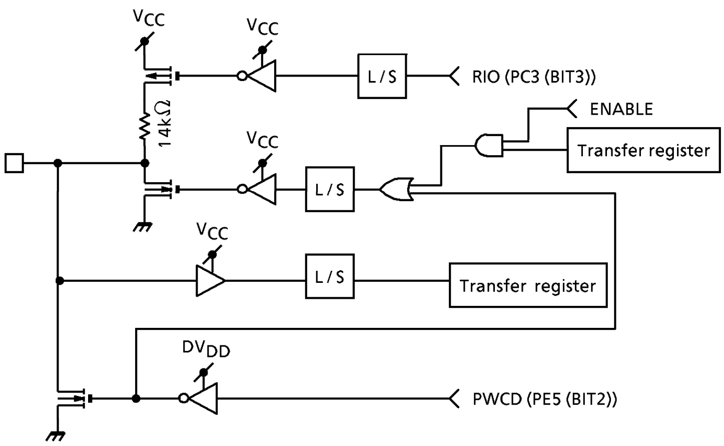
As interrupts from the IC card interface occur at the end of transmission, at the end of reception, at the occurrence of a parity error, or when receive data are not fully loaded, first confirm the interrupt then confirm the cause of the interrupt using the flag corresponding to the interrupt.

	MSB 3	2	1	0 LSB
PA5	TREFLG	RCEFLG	PEFLG	RDEFLG

Initial value = 0

Even if 0 is written to initialize register PA5, the TREFLG, the RCEFLG, the PEFLG, and the RDEFLG flags retain their previous data up to the end of the communication. Accordingly, initialize this register only after the end of the communication.
When a parity error occurs (at 9.5 etu), the resend request is output after 10.5 etu. (Register file PE4 determines the request time.)
When an interrupt is triggered by a card communications flag (TREFLG, RCEFLG, PEFLG, or RDEFLG), reading register file PA5 clears the interrupt signal to 0. (Even though the communication completes, the interrupt signal is not cleared to 0.)

The following shows the I/O pin circuit configuration.



Control the programmable pull-up resistors using the following register file.

	MSB 3	2	1	0 LSB
PC3	RIO	(ISIO)	(IICCD)	(IOIE0)

Initial value = 1

When RIO = 0, pull-up resistors are OFF. When RIO = 1, pull-up resistors are ON.
The I / O pin's initial state is high output with pull-up resistors, waiting for input.

10. External Memory Interface

This interface supports a two-lead external memory interface. The following register file is used for serial data control.
When this interface is in use, the IC card interface cannot be used.
External memory communications are supported only in CPM2 and CPM3 modes. (Only when SYSCP is set as a high-speed clock.)

	MSB 3	2	1	0 LSB
PA3	(FCLK3)	FCLK2	FCLK1	FCLK0

Initial value = 0

Set SELSIO to 1 (External Memory Communication mode).
(PE5-BIT3)

Select the transfer speed using FCLK0 to 2.

FCLK2	FCLK1	FCLK0	Transfer clock
1	0	1	$f_H / 32$
1	1	0	$f_H / 64$

(Note) : The clock output requires a high-speed oscillator.

	MSB 3	2	1	0 LSB
PF5	(EXMMODE1)	(EXMMODE0)	(EXMRW)	EXMSTA

Initial value = 0

When EXMSTA = 0, transfer stops. When EXMSTA = 1, transfer starts (is in progress).
Select the transfer mode using EXMMODE1 and 0 as follows:

	MSB 3	2	1	0 LSB
PF5	EXMMODE1	EXMMODE0	(EXMRW)	(EXMSTA)

Initial value = 0

EXMMODE1	EXMMODE0	Transfer mode
0	0	Start
0	1	Normal
1	0	Stop
1	1	No mode selected (8-bit transfer)

The following register file determines transmission or reception for communication with the external memory interface.

	MSB 3	2	1	0 LSB
PF5	(EXMMODE1)	(EXMMODE0)	EXMRW	(EXMSTA)

Initial value = 0

EXMRW = 0 : Trasmission
EXMRW = 1 : Reception

The lower four bits of the transfer data are read from / written to SIO register 1. The upper four bits of the transfer data are read from / written to SIO register 2.

SIO register 2

	MSB 3	2	1	0 LSB
PF6	SID7	SID6	SID5	SID4

Initial value = 0

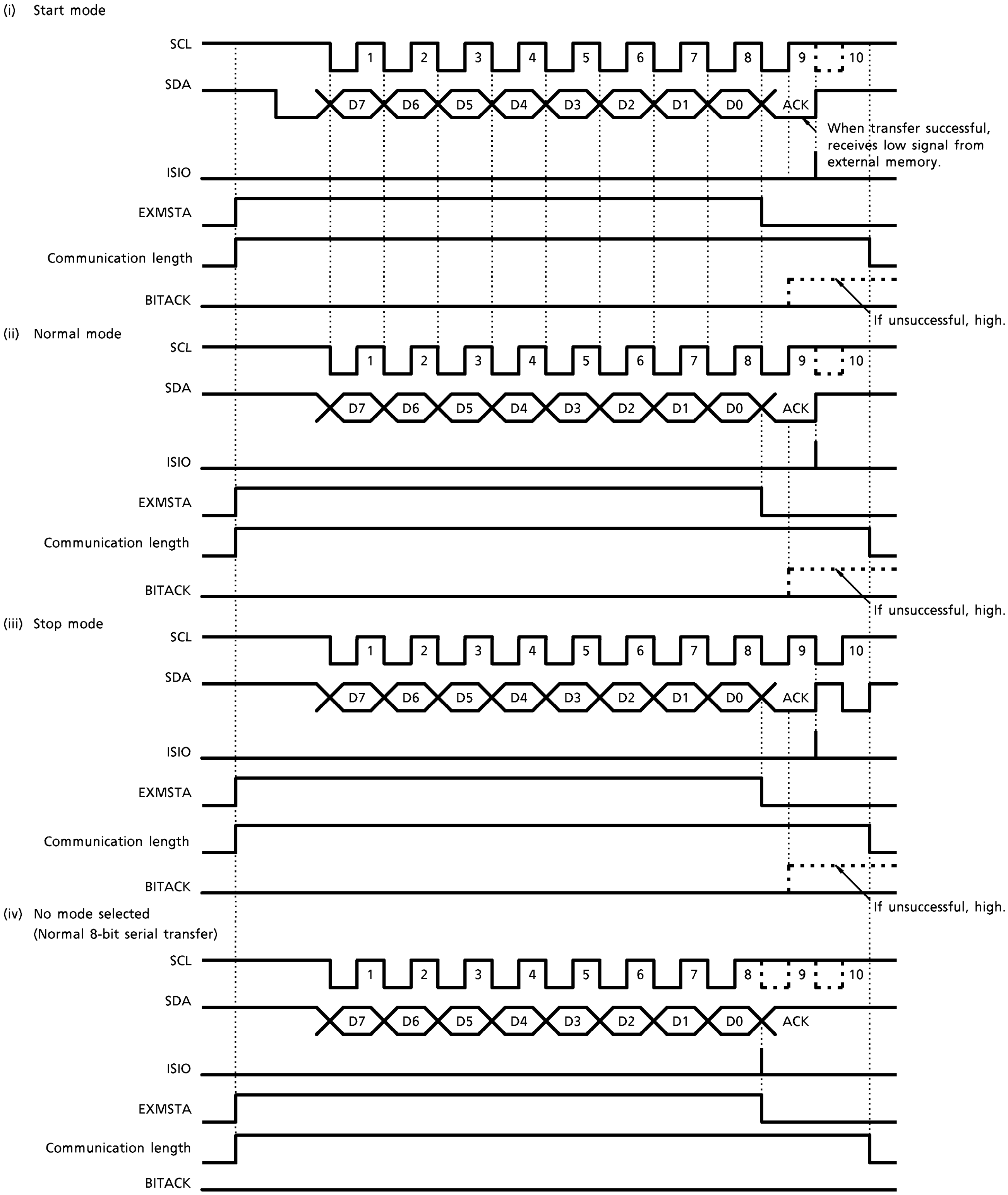
SIO register 1

	MSB 3	2	1	0 LSB
PF7	SID3	SID2	SID1	SID0

Initial value = 0

(Note) : The upper 4 bits of transfer data should be captured into PF6 and the lower 4 bits of transfer data should be captured into PF7. Thus any attempt of byte-accessing this register (i.e. attempt to capture all the 8 bits of transfer data at a time) would result in incorrect order of the upper and lower 4 bits.

External memory data transfer timing



(Note 1) : In continuous communication, execute when the communication is complete.
(Note 2) : Load the (iv) receive data one clock after an interrupt.

ISIO is reset by the processing of an interrupt. As the completion of an external memory transfer generates an interrupt, use BITACK to check whether communication was successful. If BITACK = 0, the communication was successful. If BITACK = 1, the communication was unsuccessful. When EXMSTA = 1, BITACK is reset. When normal 8-bit serial transfer is selected, BITACK remains 0.

BITACK can be read with the following register file.

	MSB 3	2	1	0 LSB
PE5	(SELSIO)	(PWCD)	(ENA5V / 3V)	BITACK

Initial value = 0

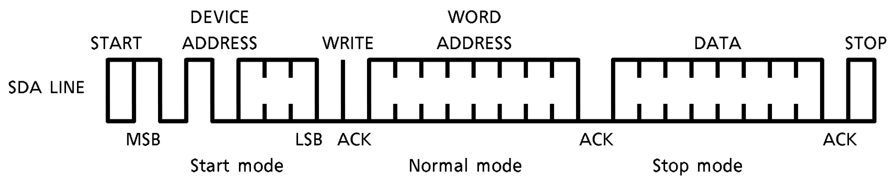
BITACK = 0, communication successful.
BITACK = 1, communication unsuccessful.

External memory communication method

Use the following method to communicate with the external memory.
Note that when a read is completed, this IC does not send an ACK signal to external memory.
"DEVICE ADDRESS" below indicates the signal used to specify external memory to be accessed.
"WORD ADDRESS" indicates the specified external memory ROM address.

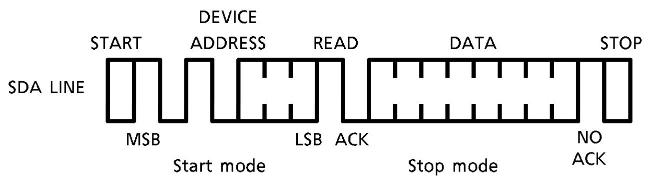
(1) Writing method

(i) Byte writing

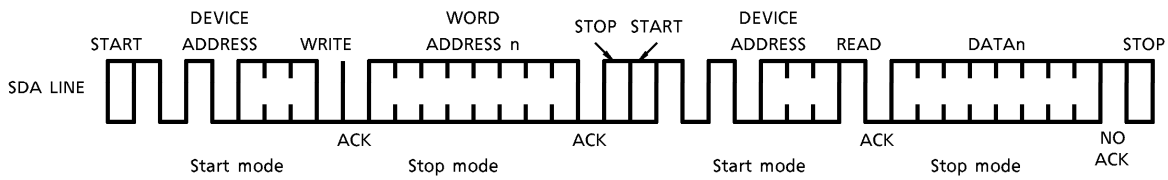


(2) Reading method

(i) How to read the current address

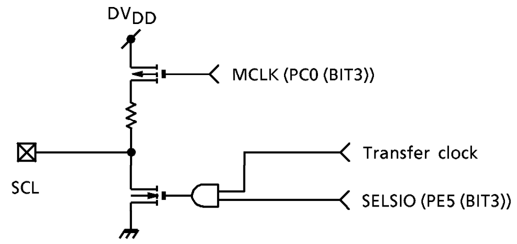


(ii) Random read method



The following shows the circuit configuration for the external memory interface block.

≪External memory interface≫
CLOCK pin



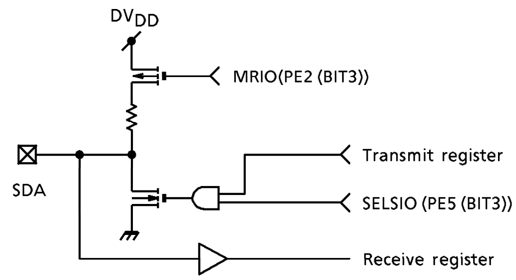
Control the pull-up resistor of the external memory interface clock pin using the following register.

	MSB 3	2	1	0 LSB
PC0	MCLK	(ESELT)	(ESELT1)	(ESELT0)

Initial value = 0

MCLK = 0 : Pull-up resistor ON.
MCLK = 1 : Pull-up resistor OFF.

Data transmit / receive pin



	MSB 3	2	1	0 LSB
PE2	MRIO	(CKS13)	(CKS12)	(CKS11)

Initial value = 0

MRIO = 0 : Pull-up resistor ON.
MRIO = 1 : Pull-up resistor OFF.

OUTLINE OF SPECIFICATIONS

(1) Outline

Product number	JTMP04020-XXXS (PI)	
Application	Contact-type IC card reader	
Structure	SDT-0.6 2AL	
Power supply voltage	4.7-V version	3-V version
Configuration / Functions	LCD driver, voltage differential detector circuit, IC card power supply control circuit, IC card interface, E^2PROM interface	LCD driver, IC card power supply control circuit, IC card interface, E^2PROM interface
Number of pins	102 (excluding trimming fuse)	←
Power supply system	DVDD: Power supply for logic AVDD: Power supply for analog DGND: GND for logic AGND: GND for analog PGND: GND for BL pin	←
ROM	16 Kword	←
DATA RAM	6 Kbit	←
WORK RAM	2 Kbit	←
DISPLAY RAM	544 bit (16 com × 34 seg) 336 bit (8 com × 42 seg)	←
Oscillator circuit	High-speed oscillation: 3.58 MHz Low-speed oscillation : 35 kHz (CR), 32 kHz (crystal)	High-speed oscillation: 2 MHz, 32 kHz (crystal)
Regulator	1.8-V regulator (for low-speed oscillation)	←
IO ports	Input ports: 8, input/output ports: 12 Buzzer output port: 1	←
LCD driver	16 com x 34 seg or 8 com × 42 seg Bleeder resistance External LCD power supply required	←
Voltage differential detector circuit	Built-in capacitor: 2 levels (Detection level determined by external or internal resistance.) Detects Δ 100 mV or Δ150 mV	Not usable
IC card power supply control circuit	External transistors, capacitors. 3 V / 4.7 V switching control circuit Precision: within ± 5%	External transistors, capacitors. Precision: within ± 5%
IC card interface	CLK, RST, I / O	←
E^2PROM interface	SCL, SDA	←

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	−0.3~6.0	V
Input Voltage	V_{IN}	V_{DD} + 0.3~GND − 0.3	V
Operating Temperature	T_{opr}	0~40	°C
Storage Temperature	T_{stg}	−55~125	°C

(2) Mask options

	Power supply voltage	Duty	Segment	High-speed oscillator	Low-speed oscillator	Battery check BR pin	Remarks
A4580	3.0 (V), 4.7 (V)	1 / 8	42	X'tal	X'tal	External resistor cannot be connected	Planned
A45F0	3.0 (V), 4.7 (V)	1 / 16	34	X'tal	X'tal	External resistor cannot be connected	Planned
A4582	4.7 (V)	1 / 8	42	X'tal	CR	External resistor cannot be connected	—
A45F2	4.7 (V)	1 / 16	34	X'tal	CR	External resistor cannot be connected	Planned
A4680	3.0 (V), 4.7 (V)	1 / 8	42	X'tal	X'tal	External resistor can be connected, Planned	Planned
A46F0	3.0 (V), 4.7 (V)	1 / 16	34	X'tal	X'tal	External resistor can be connected, Planned	Planned
A4682	4.7 (V)	1 / 8	42	X'tal	CR	External resistor can be connected, Planned	Planned
A46F2	4.7 (V)	1 / 16	34	X'tal	CR	External resistor can be connected, Planned	Planned

* : In the above mask options, when the low-speed oscillator is controlled by CR (A4582, A45F2, A4682, A46F2), the IC cannot be used with a 3.0-V power supply.

(3) Electrical Characteristics

Maximum ratings (Ta = 25°C)

Parameter	Symbol	Rating	Unit
Power supply voltage	V_{DD}	−0.3 ~ 6.0	V
Input voltage	V_{IN}	V_{DD} + 0.3 ~ GND −0.3	V
Operating temperature	T_{opr}	0 ~ 40	°C
Storage temperature	T_{stg}	−55 ~ 125	°C

Test Specifications (Ta = 25°C, unless otherwise specified, DV_{DD} = AV_{DD} = VLC = 3.0 V)

Parameter	Conditions	Symbol	Min	Typ.	Max	Unit
For power supply						
Power supply voltage 1	No AVDD load	$V_{DD}1$	2.94	3.0	3.06	V
Power supply voltage 2	No AVDD load	$V_{DD}2$	4.6	4.7	4.8	V
Power supply voltage 3 (Note 1)	AVDD load = 50 mA	$V_{DD}3$	4.4	4.7	4.8	V
Oscillator						
High-speed oscillation frequency 1	DV_{DD} = 3.0 V, external 2.0 MHz crystal	HICP1	—	2.0	—	MHz
High-speed oscillation frequency 2	DV_{DD} = 4.7 V, external 3.58 MHz crystal	HICP2	—	3.58	—	MHz
Low-speed oscillation frequency 1	Internal CR (when DV_{DD} = 4.7 V only)	LOWCP1	20	35	60	kHz
Low-speed oscillation frequency 2	External 32-kHz crystal	LOWCP2	—	32.768	—	kHz
SCL (1)						
Low-level output current	V_{OL} = 0.5 V	I_{OL}, SCL	2.0	—		mA
Pull-up resistor		R, SCL	12	20	28	kΩ
SDA (2)						
High-level input voltage		V_{IH}, SDA	DV_{DD} ×0.8	—	DV_{DD}	V
Low-level input voltage		V_{IL}, SDA	0	—	DV_{DD} ×0.2	V
Low-level output current	V_{OL} = 0.5 V	I_{OL}, SDA	2.0	—	—	mA
Pull-up resistor		R, SDA	12	20	28	kΩ
CLK (3)						
High-level output current	V_{OH} = 2.5 V, VCC on (PE5, bit 2 = 1)	I_{OH}, CLK	—	—	−4.0	mA
Low-level output current 1	V_{OL} = 0.5 V, VCC on (PE5, bit 2 = 1)	I_{OL}, CLK1	5.0	—	—	mA
Low-level output current 2	V_{OL} = 0.5 V, VCC off (PE5, bit 2 = 0)	I_{OL}, CLK2	100	—	—	μA
Clock duty	Deviation from 50% duty (based on clock H level) fclk = 3.58 / 1.79 MHz	CLK, DUTY	−5	—	5	%

(*) : At 4.7 V, connect DVDD to AVDD to VLC.
At 3.0 V, connect DVDD to AVDD. Apply 4.7 V to VLC using an external booster circuit.

(Note) : When AVDD load = 50 mA, card communication cannot be performed.

Test Specifications (Ta = 25°C; unless otherwise specified: $DV_{DD} = AV_{DD}$ = VLC = 3.0 V)

Parameter	Conditions	Symbol	Min	Typ.	Max	Unit
RST (4)						
High-level output current	V_{OH} = 2.5 V, VCC on (PE5, bit 2 = 1)	I_{OH}, RST		—	− 4.0	mA
Low-level output current 1	V_{OL} = 0.5 V, VCC on (PE5, bit 2 = 1)	I_{OL}, RST1	5.0	—	—	mA
Low-level output current 2	V_{OL} = 0.5 V, VCC off (PE5, bit 2 = 0)	I_{OL}, RST2	100	—	—	μA
IO (5)						
High-level input voltage	V_{CC} = 3 / 4.7 V	V_{IH}, IO	V_{CC} × 0.8	—	V_{CC}	V
Low-level input voltage	V_{CC} = 3 / 4.7 V	V_{IL}, IO	0	—	V_{CC} × 0.2	V
Low-level output current 1	V_{OL} = 0.5 V, V_{CC} on (PE5, bit 2 = 1)	I_{OL}, IO1	5.0	—	—	mA
Low-level output current 2	V_{OL} = 0.5 V, V_{CC} off (PE5, bit 2 = 0)	I_{OL}, IO2	100	—	—	μA
Pull-up resistor		R, IO	8.4	14	19.6	kΩ
V_{CC} (6)						
Output Voltage	V_{CC} = 3.0 V, no load	V_{CC1}	2.85	3.0	3.15	V
Pull-down resistor		R, V_{CC}	30	50	70	kΩ
TRCNT (7)						
High-level output current	V_{OH} = 2.5 V, V_{CC} off (PE5, bit 2 = 0)	I_{OH}, TRCNT	—	—	− 0.5	mA
Low-level output current	V_{OL} = 0.5 V, V_{CC} on (PE5, bit 2 = 1)	I_{OL}, TRCNT	1.0	—	—	mA
BL (10)						
Low-level output current	Only when DV_{DD} = 4.7 V, V_{OL} = 1.0 V (PC4, bit 1 = 1)	I_{OL}, BL	50	—	—	mA
Off-leak current	V_{OUT} = 4.0 V (PC4, bit 1 = 0)	LEAK, BL	− 2	—	2	μA
Power supply Voltage detection 1	VDET1 = VSH − VSH1	VDET1	80	100	120	mV
Power supply Voltage detection 2	VDET2 = VSH − VSH2	VDET2	120	150	180	mV
Sample time	C0 = 50 pF (design target)	TSPL	20	—	—	mS
Hold time	C0 = 50 pF (design target)	THOLD	—	—	52	mS
TEST2 (16)						
High-level input Voltage		V_{IH}, TEST2	DV_{DD} × 0.8	—	DV_{DD}	V
Low-level input Voltage		V_{IL}, TEST2	0	—	V_{DD} × 0.2	V
Pull-down resistor		R, TEST2	6	10	14	kΩ
VXT (20)						
Low-voltage output Voltage		VVXT	—	1.92	—	V

Test Specifications (Ta = 25°C; unless otherwise specified: $DV_{DD} = AV_{DD}$ = VLC = 3.0 V)

Parameter	Conditions	Symbol	Min	Typ.	Max	Unit
BRESET (24)						
High-level input Voltage		V_{IH}, BRESET	DV_{DD} × 0.8	—	DV_{DD}	V
Low-level input Voltage		V_{IL}, BRESET	0	—	DV_{DD} × 0.2	V
Pull-up resistor (high resistance)	At reset	R, BRESET1	300	500	700	kΩ
Pull-up resistor (low resistance)	Except at reset	R, BRESET2	30	50	70	kΩ
IN01 (25), IN02 (26), IN03 (27), IN04 (28) IN11 (29), IN12 (30), IN13 (31), IN14 (32)						
High-level input Voltage		V_{IH}, IN01	DV_{DD} × 0.8	—	DV_{DD}	V
Low-level input Voltage		V_{IL}, IN01	0	—	DV_{DD} × 0.2	V
Pull-down resistor		R, IN01	60	100	140	kΩ
IO01 (33), IO02 (34), IO03 (35), IO04 (36) IO11 (37), IO12 (38), IO13 (39), IO14 (40) IO21 (41), IO22 (42), IO23 (43), IO24 (44)						
High-level input Voltage		V_{IH}, IO01	DV_{DD} × 0.8	—	DV_{DD}	V
Low-level input Voltage		V_{IL}, IO01	0	—	DV_{DD} × 0.2	V
High-level output current	V_{OH} = 2.5 V	I_{OH}, IO01	—	—	– 1.0	mA
Pull-down resistor		R, IO01	60	100	140	kΩ
KOUT (45)						
High-level output current	V_{OH} = 2.5 V	V_{OH}, 32KOUT	—	—	– 1.0	mA
Low-level output current	V_{OL} = 0.5 V	V_{OL}, 32KOUT	1.0	—	—	mA
TEST1 (46)						
High-level input Voltage		V_{IH}, TEST1	DV_{DD} × 0.8	—	DV_{DD}	V
Low-level input Voltage		V_{IL}, TEST1	0	—	DV_{DD} × 0.2	V
Pull-down resistor		R, TEST1	6	10	14	kΩ
BZ (47)						
High-level output Voltage	V_{OH} = 2.5 V	I_{OH}, BZ	—	—	– 1.0	mA
Low-level output Voltage	V_{OL} = 0.5 V	I_{OL}, BZ	1.0	—	—	mA

Test Specifications (Ta = 25°C; unless otherwise specified: $DV_{DD} = AV_{DD}$ = VLC = 4.7 V)

Parameter	Conditions	Symbol	Min	Typ.	Max	Unit
VLC (98), VLC4 (99), LVC3 (100), VLC2 (101), VLC1 (102)						
Liquid crystal display power supply Voltage (Note 1)	VLC = 4.7 V	VVLC	DV_{DD}	4.7	4.8	V
Liquid crystal display reference Voltage 1	VLC = 4.7 V, VVLC4 = 4.5 V (R16W"3")	LLVC1	1.069	1.125	1.181	V
Liquid crystal display reference Voltage 2	VLC = 4.7 V, VVLC4 = 4.5 V (R16W"3")	VVLC2	2.138	2.250	2.363	V
Liquid crystal display reference Voltage 3	VLC = 4.7 V, VVLC4 = 4.5 V (R16W"3")	VVLC3	3.206	3.375	3.544	V
Liquid crystal display reference Voltage 4	VLC = 4.7V, VVLC4 = 4.5V (R16W"3")	VVLC4	4.275	4.500	4.725	V
Frame frequency	fL = 32 kHz	Fframe	—	95.7	—	Hz

(Note) : To ensure display quality, Toshiba recommend setting the liquid crystal display power supply Voltage at 4.7 ± 0.1 V.

Test Specifications (Ta = 25°C; unless otherwise specified: $DV_{DD} = AV_{DD}$ = VLC = 4.7 V)

Parameter		Conditions	Symbol	Min	Typ.	Max	Unit
High-speed crystal …X'tal low-speed crystal …X'tal	Current dissipation 1	(CMP3) 3.58 MHz, no load, 4.7-V regulator on, LCD lit at card communication	IDDOP1	—	1.3	6.0	mA
	Current dissipation 2	(CMP3) 3.58 MHz, no load, 4.7-V regulator ON, LCD not lit at card communication	IDDOP2	—	1.3	6.0	mA
	Current dissipation 3	(CMP1) 32 kHz, no load, Slow mode, LCD lit	ISLOW1	—	29	70	μA
	Current dissipation 4	(CMP1) 32 kHz, no load, Slow mode, LCD not lit	ISLOW2	—	16	40	μA
	Current dissipation 5	(CMP1) 32 kHz, no load, Halt mode, LCD lit	IQD1	—	22	50	μA
	Current dissipation 6	(CMP1) 32 kHz, no load, Halt mode, LCD not lit	IQD2	—	9	25	μA
	Current dissipation 7	(CMP0) Stop mode	ISTOP	—	1.0	3.0	μA
High-speed crystal …X'tal low-speed crystal …CR	Current dissipation 1	(CMP3) 3.58 MHz, no load, 4.7-V regulator on, LCD lit at card communication	IDDOP1	—	1.3	6.0	mA
	Current dissipation 2	(CMP3) 3.58 MHz, no load, 4.7-V regulator on, LCD not lit at card communication	IDDOP2	—	1.3	6.0	mA
	Current dissipation 3	(CMP1) 32 kHz, no load, Slow mode, LCD lit	ISLOW1	—	29	70	μA
	Current dissipation 4	(CMP1) 32 kHz, no load, Slow mode, LCD not lit	ISLOW2	—	16	40	μA
	Current dissipation 5	(CMP1) 32 kHz, no load, Halt mode, LCD lit	IQD1	—	22	50	μA
	Current dissipation 6	(CMP1) 32 kHz, no load, Halt mode, LCD not lit	IQD2	—	9	25	μA
	Current dissipation 7	(CMP0) Stop mode	ISTOP	—	1.0	3.0	μA

(Note) : For the low-speed crystal Version, Toshiba will produce a fluctuation sample and determine the final specifications when the user requests a sample.

APPLICATION CIRCUIT