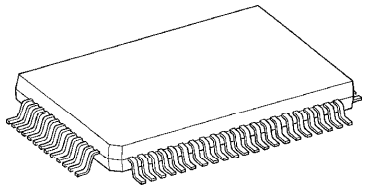
TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

T7988, JT7988Y-AS

T7988, JT7988Y-AS SINGLE-CHIP CMOS LSI FOR LCD CALCULATORS

The T7988, JT7988Y-AS is single-chip microcomputer for 10-digit + 2-digit scientific calculator.
T7988, JT7988Y-AS is the complete single-chip CMOS LSI for electronic calculator with 10 digits, 67 functions, 3 expression and hexadecimal, octal and binary, statistic calculation, fractional number calculation, and logic operation with the following features.



QFP67-P-1420-0.80

Weight : 1.20g (Typ.)

FEATURES

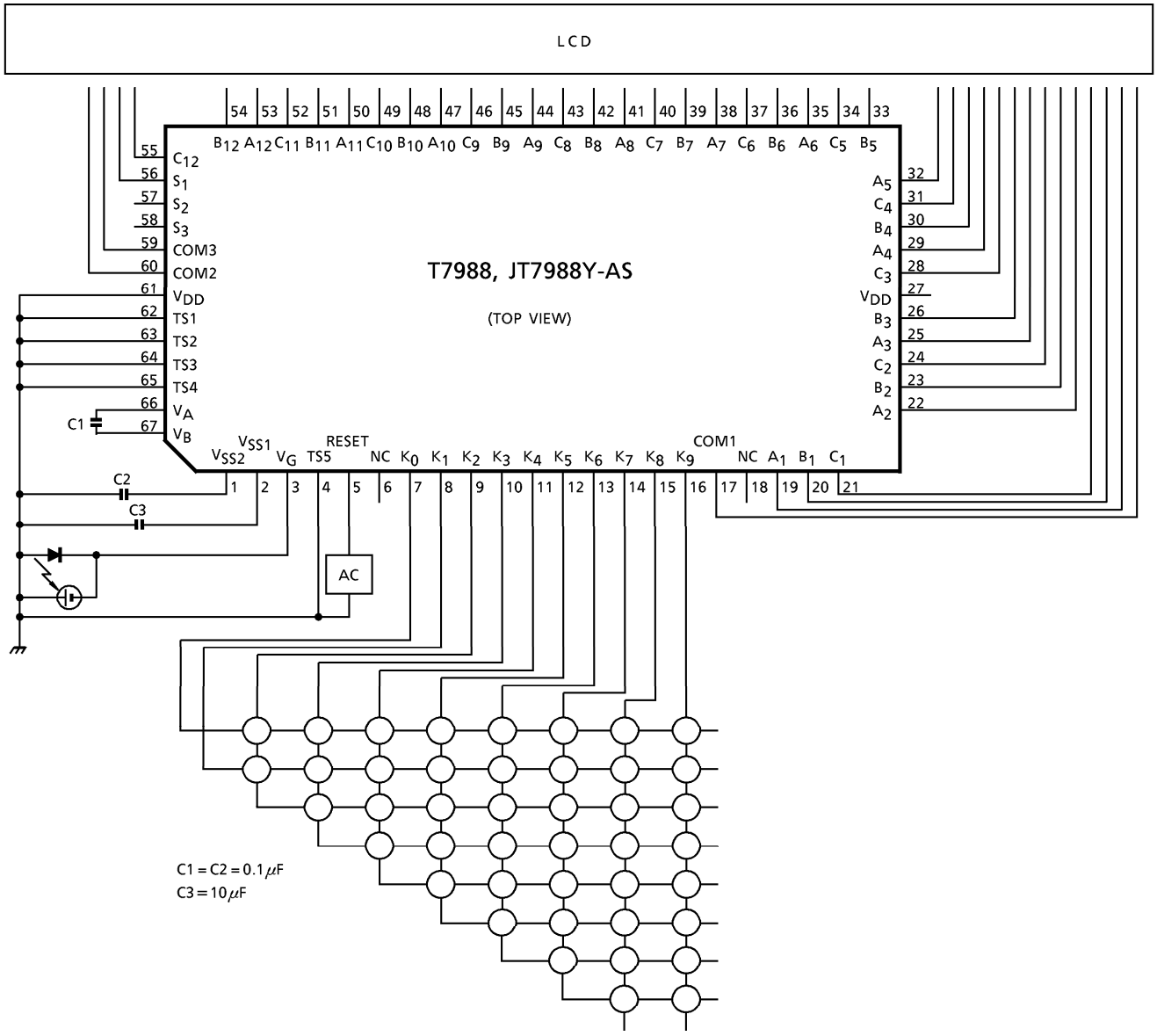
- 12-digit display plus 2-digit code at the right margin.
  - Scientific and engineering display.
    Mantissa 10 digits plus exponent 2 digits plus negative code 2 digits.
  - Other than above
    Mantissa 10 digits plus negative code 1 digit.
- 13 kinds of special display

M	Memory	HEX	Hexadecimal mode
–	Mantissa and exponent Minus	SD	Statistic calculation mode
E	Error	DEG	Degree
INV	Inverse	RAD	Radian
HYP	Hyperbolic	GRAD	Gradian
BIN	Binary mode	( )	Parenthesis calculation
OCT	Octal mode		

- The minus sign of the mantissa is floating minus.
- The arithmetic key operation in clouding Y^x or $\sqrt[x]{Y}$ has same sequence as mathematical equation. 6 pending operations are allowed and ( ) are up to continuous 15 levels.
- Fractional number calculation.
- It is possible to convert mutually between decimal, binary, octal and hexadecimal, and the 4 operations in arithmetic in binary, octal and hexadecimal.

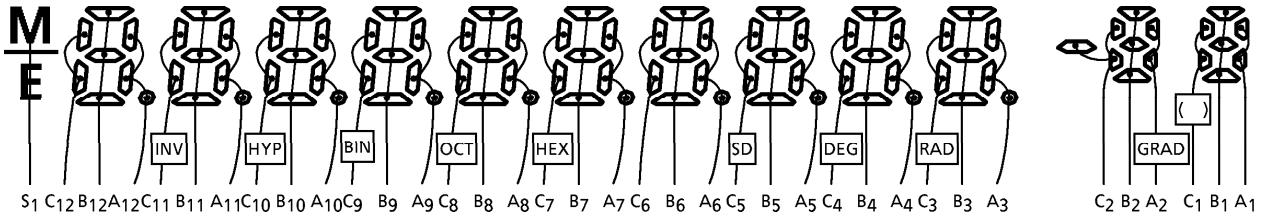
- One independent accumulating memory.
- It is possible to convert or fix the display number system by FLO (Floating) , SCI (Scientific) or ENG (Engineering) key.
- It is possible to specify decimal part digits (0~9) by FIX key.
- Direct drive for FEM LCD (1 / 2 prebias, 1 / 3 duty) .
- Automatic power on clear.
- Low-power consumption. V_G = – 1.5V single power supply.
- The 67-pin flat package is used.

SYSTEM BLOCK DIAGRAM

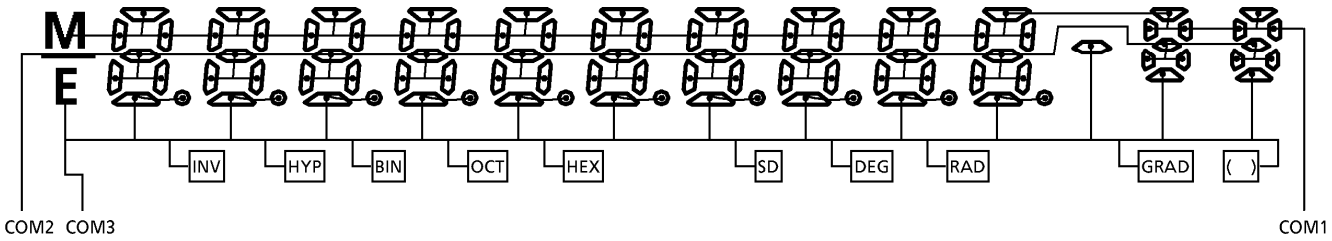


CONNECTION OF LCD

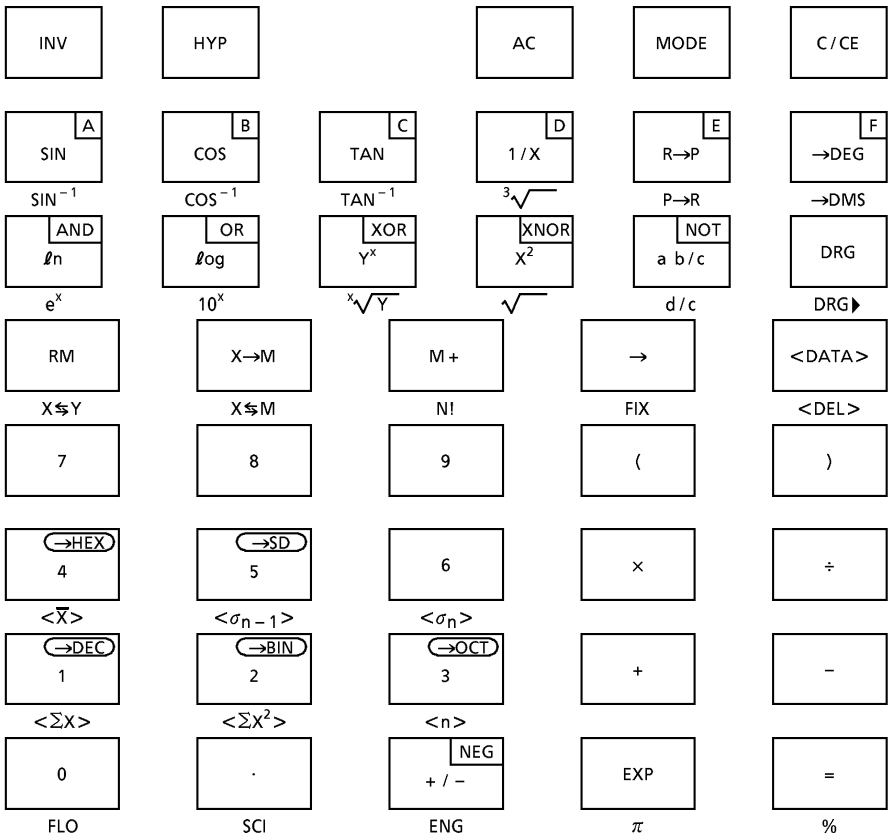
SEGMENT



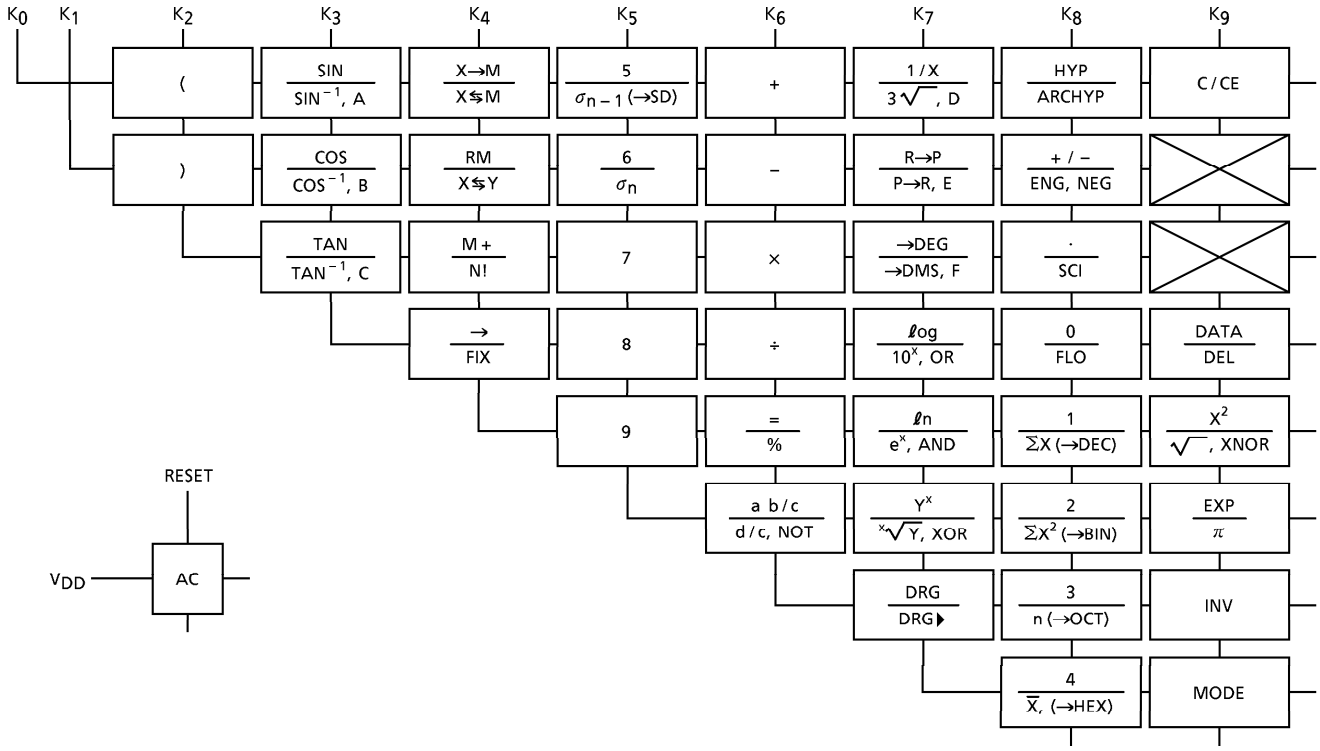
COMMON



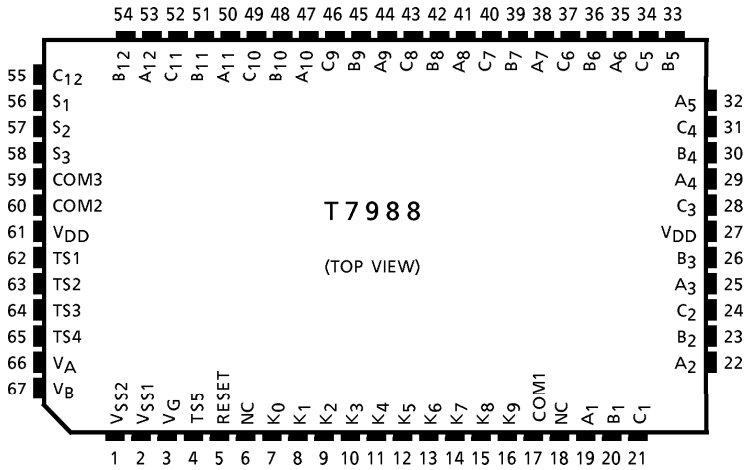
SET KEY LAYOUT (Example)



KEY CONNECTION



PIN ASSIGNMENT



SPECIFICATION OF CALCULATOR

Speed of calculation

Key on 10ms Key off 33.8ms $f\phi WAIT = 9kHz$, $f\phi op = 24kHz$

The calculation speed doesn't include the key on or off time.

ITEM	OPERATION			CALCULATION SPEED (ms)
Number	DEC		5	26
		5	5	25
	HEX		A	26
		A	A	25
Function	DEC	5	+	69
		5	×	73
	HEX	A	−	172
		A	÷	176
4 operation	DEC	1 + 2	+	97
		1 0 0 0 0 0 0 0 0 0 − 1	−	104
		5 × 9	×	104
		5 5 5 5 5 × 9 9 9 9 9	×	120
		5 ÷ 9	÷	157
		5 5 5 5 5 ÷ 9 9 9 9 9	÷	193
	HEX	A B C + D E F	+	291
		A B C − D E F	−	479
		A B C × D E F	×	334
		A B C ÷ D E F	÷	324
Y^x, $\sqrt[x]{Y}$		3 Y^x 4	=	842
		3 $\sqrt[x]{Y}$ 4	=	872
SIN	DEG	3 0	SIN	798
	RAD	π ÷ 6 =	SIN	764
	GRAD	1 0 0 ÷ 3 =	SIN	1161
COS	DEG	6 0	COS	809
	RAD	π ÷ 3 =	COS	1031
	GRAD	200 ÷ 3 =	COS	1176
TAN	DEG	4 5	TAN	386
	RAD	π ÷ 4 =	TAN	143
	GRAD	5 0	TAN	154
SIN^{-1}	DEG	0 . 5	SIN^{-1}	836
	RAD	0 . 5	SIN^{-1}	653
	GRAD	0 . 5	SIN^{-1}	825
COS^{-1}	DEG	0 . 5	COS^{-1}	1069
	RAD	0 . 5	COS^{-1}	762
	GRAD	0 . 5	COS^{-1}	1057
TAN^{-1}	DEG	1	TAN^{-1}	237
	RAD	1	TAN^{-1}	147
	GRAD	1	TAN^{-1}	236
Ln		2 0	ln	160
Log		2 0	ℓog	332

ITEM	OPERATION			CALCULATION SPEED (ms)
e^x		2 0	e^x	315
10^x		1. 2 3	10^x	380
		1 0	10^x	137
X!		6 9	N!	970
HYP		3 hyp	SIN	623
		3 hyp	COS	627
		3 hyp	TAN	766
ARC HYP		3 hyp^{-1}	SIN	607
		3 hyp^{-1}	COS	677
		0.5 hyp^{-1}	TAN	574
X^2		2 0	X^2	64
$\sqrt{}$		2 0	$\sqrt{}$	217
1/X		2 0	1/X	80
$\sqrt[3]{}$		2 0	$\sqrt[3]{}$	604
Mutual Conversion	DEC	1 2 3	→BIN	118
		1 2 3 4 5	→OCT	134
		1 2 3 4 5	→HEX	120
	BIN	1 0 1 0 1	→DEC	93
	OCT	1 2 3 4 5	→DEC	112
	HEX	A B C D E	→DEC	181
→DEG		1.2 3 4 5	→DEG	265
→DMS		1.2 3 4 5	→DMS	304
R→P	DEG	$\sqrt[3]{}$ X⇆Y 1	R→P	920
	RAD	$\sqrt[3]{}$ X⇆Y 1	R→P	723
	GRAD	$\sqrt[3]{}$ X⇆Y 1	R→P	919
P→R	DEG	2 X⇆Y 3 0	P→R	1543
	RAD	2 X⇆Y 30 DRG▶	P→R	1461
	GRAD	2 X⇆Y 30 DRG▶ DRG▶	P→R	2089
→RAD	DEG	3 6 0	DRG▶	147
→GRAD	RAD	2 × π =	DRG▶	100
→DEG	GRAD	4 0 0	DRG▶	71
Memory		1 2 3	X→M	47
		1 2 3 X→M	M+	65
		1 2 3 X→M	RM	41
		1 2 3 X→M	X⇆M	54
%		1 2 3 + 4 5 6	%	86
		1 2 3 − 4 5 6	%	86
		1 2 3 × 4 5 6	%	56
		1 2 3 ÷ 4 5 6	%	56
Exchange		1 2 3 + 4 5 6	X⇆Y	52
Shift		1 2 3	→	27

ITEM	OPERATION			CALCULATION SPEED (ms)
Statistic Calculation	1 DATA 2 DATA 3 DATA …… 8 DATA 9		DATA	125
	The above-mentioned data		n	56
			$\overline{X}$	74
			ΣX	51
			ΣX^2	52
			σ_{n-1}	300
			σ_n	347
Logic operation	HEX	A B C AND D E F	=	603
		A B C OR D E F	=	650
		A B C XOR D E F	=	568
		A B C XNOR D E F	=	961
		A B C	NOT	394
NEG	HEX	A B C	NEG	375
Fractional number calculation	Function	2 ab/c 3 6 ab/c 2 3 4	−	249
		2 ab/c 3 6 ab/c 2 3 4	÷	253
	4-operation	2 _ 36 ⌟ 234 + 3 _ 45 ⌟ 345	=	536
		2 _ 36 ⌟ 234 − 3 _ 45 ⌟ 345	=	512
		2 _ 36 ⌟ 234 × 3 _ 45 ⌟ 345	=	498
		2 _ 36 ⌟ 234 ÷ 3 _ 45 ⌟ 345	=	562

OPERATION RANGE AND ACCURACY

FUNCTION	ANGLE UNIT	OPERATION RANGE	UNDER FLOW AREA	NORMAL ACCURACY
SIN X	DEG	$0 \leqq \|X\| \leqq 4.499999999 \times 10^{10}$	$0 \leqq \|X\| \leqq 5.729577951 \times 10^{-98}$	±1 in 10th significant digit
	RAD	$0 \leqq \|X\| \leqq 785398163.3$	—	
	GRAD	$0 \leqq \|X\| \leqq 4.999999999 \times 10^{10}$	$0 \leqq \|X\| \leqq 6.366197723 \times 10^{-98}$	
COS X	DEG	$0 \leqq \|X\| \leqq 4.500000008 \times 10^{10}$	—	
	RAD	$0 \leqq \|X\| \leqq 785398164.9$	—	
	GRAD	$0 \leqq \|X\| \leqq 5.000000009 \times 10^{10}$	—	
TAN X	DEG	SAME AS SINX except for $\|X\| = (2n-1) \cdot 90$	SAME AS SINX	
	RAD	SAME AS SINX except for $\|X\| = (2n-1) \cdot \pi / 2$	SAME AS SINX	
	GRAD	SAME AS SINX except for $\|X\| = (2n-1) \cdot 100$	SAME AS SINX	
$SIN^{-1}X$	DEG	$0 \leqq \|X\| \leqq 1$	$0 \leqq \|X\| \leqq 1.570796326 \times 10^{-99}$	
	RAD	$0 \leqq \|X\| \leqq 1$	—	
	GRAD	$0 \leqq \|X\| \leqq 1$	$0 \leqq \|X\| \leqq 1.570796326 \times 10^{-99}$	
$COS^{-1}X$	DEG	SAME AS $SIN^{-1}X$	—	
	RAD	SAME AS $SIN^{-1}X$	—	
	GRAD	SAME AS $SIN^{-1}X$	—	
$TAN^{-1}X$	DEG	$0 \leqq \|X\| \leqq 9.999999999 \times 10^{99}$	SAME AS $SIN^{-1}X$	
	RAD	$0 \leqq \|X\| \leqq 9.999999999 \times 10^{99}$	—	
	GRAD	$0 \leqq \|X\| \leqq 9.999999999 \times 10^{99}$	SAME AS $SIN^{-1}X$	

FUNCTION	OPERATION RANGE	UNDER FLOW AREA	NORMAL ACCURACY
LN X	$0<X$	—	±1 in 10th significant digit
LOG X	$0<X$	—	
e^X	$-9.999999999\times10^{99}$ $\leqq X\leqq 230.2585092$	$-9.999999999\times10^{99}$ $\leqq X\leqq -227.9559243$	
10^X	$-9.999999999\times10^{99}$ $\leqq X\leqq 99.99999999$	$-9.999999999\times10^{99}$ $\leqq X\leqq -99.00000001$	
X!	$0\leqq X\leqq 69$ (INTEGER)	—	
$\frac{1}{X}$	1×10^{-99} $\leqq \lvert X\rvert \leqq 9.999999999\times10^{99}$	1.000000001×10^{99} $\leqq \lvert X\rvert \leqq 9.999999999\times10^{99}$	
X^2	$0\leqq \lvert X\rvert \leqq 9.999999999\times10^{49}$	$\leqq \lvert X\rvert \leqq 3.162277660\times10^{-50}$	
$\sqrt{X}$	$0\leqq X\leqq 9.999999999\times10^{99}$	—	
$\sqrt[3]{X}$	$0\leqq \lvert X\rvert \leqq 9.999999999\times10^{99}$	—	
DMS→DEG	$0\leqq \lvert X\rvert \leqq 9.999999999\times10^{9}$	—	
DEG→DMS	$0\leqq \lvert X\rvert \leqq 9999999.999$	$0\leqq \lvert X\rvert \leqq 1.388888888\times10^{-6}$	±1 in least significant digit
SINH X	$0\leqq \lvert X\rvert \leqq 230.2585092$	—	±1 in 10th significant digit
COSH X	$0\leqq \lvert X\rvert \leqq 230.2585092$	—	
TANH X	$0\leqq \lvert X\rvert \leqq 9.999999999\times10^{99}$	—	
$SINH^{-1}X$	$0\leqq \lvert X\rvert \leqq 4.999999999\times10^{99}$	—	
$COSH^{-1}X$	$1\leqq X\leqq 4.999999999\times10^{99}$	—	
$TANH^{-1}X$	$0\leqq \lvert X\rvert \leqq 9.999999999\times10^{-1}$	—	
R→P ($xy\rightarrow\gamma\theta$)	$\lvert x\rvert, \lvert y\rvert \leqq 9.999999999\times10^{49}$ $(x^2+y^2)\leqq 9.999999999\times10^{99}$ $\frac{Y}{X}$; SAME AS $TAN^{-1}X$	$\frac{Y}{X}$; SAME AS $TAN^{-1}X$	±1 in 10th significant digit
P→R ($\gamma\theta\rightarrow xy$)	$0\leqq\gamma\leqq 9.999999999\times10^{99}$ θ ; SAME AS SIN X, COS X	θ ; SAME AS SIN X, COS X	
DEG→RAD	$0\leqq \lvert X\rvert \leqq 9.999999999\times10^{99}$	$0\leqq \lvert X\rvert \leqq 5.729577951\times10^{-98}$	
RAD→GRAD	$0\leqq \lvert X\rvert \leqq 1.570796326\times10^{98}$	—	
GRAD→DEG	$0\leqq \lvert X\rvert \leqq 9.999999999\times10^{99}$	$0\leqq \lvert X\rvert \leqq 1.111111111\times10^{-99}$	
Y^X	$-9.999999999\times10^{99}$ $\leqq X\cdot LN\ \lvert Y\rvert \leqq 230.2585092$	$-9.999999999\times10^{99}$ $\leqq X\cdot LN\ \lvert Y\rvert \leqq -227.9559243$	±1 in 10th significant digit
	(1) $Y>0$ ··· The above-mentioned operation range. (2) $Y<0$ ··· X (Integer) or, 1 / X (Odd, $X\neq 0$) ··· The above-mentioned operation range. (3) $Y=0$ ··· $0<X$		

FUNCTION	OPERATION RANGE	UNDER FLOW AREA	NORMAL ACCURACY
$\sqrt[X]{Y}$	$-9.999999999\times10^{99}$ $\leqq \frac{1}{X}\cdot LN\ \|Y\| \leqq 230.2585092$	$-9.999999999\times10^{99}$ $\leqq \frac{1}{X}\cdot LN\ \|Y\| \leqq -227.95593243$	±1 in 10th significant digit
	(1) Y>0…The above-mentioned operation range. (2) Y<0…X (Odd) or 1/X (Integer, X≠0) …The above-mentioned operation range. (3) Y=0…0<X		
→DEC	Operation range The following operation range after the conversion. 0≦|X|≦9999999999		—
→BIN	The following operation range after the conversion. 1000000000≦X≦1111111111 0≦X≦ 111111111		—
→OCT	The following operation range after the conversion. 4000000000≦X≦7777777777 0≦X≦3777777777		—
→HEX	The following operation range after the conversion. FDABF41CO1≦X≦FFFFFFFFFF 0≦X≦2540BE3FF		—
AND OR XOR XNOR	BIN ; 1000000000≦X≦1111111111 0≦X≦ 111111111 OCT ; 4000000000≦X≦7777777777 0≦X≦3777777777 HEX ; The following operation range after the operation. FDABF41CO1≦X≦FFFFFFFFFF 0≦X≦2540BE3FF		—
NOT	BIN ; SAME AS AND OCT ; SAME AS AND HEX ; FDABF41CO1≦X≦FFFFFFFFFF 0≦X≦2540BE3FE		—
NEG	BIN ; 1000000001≦X≦1111111111 0≦X≦ 111111111 OCT ; 4000000001≦X≦7777777777 0≦X≦3777777777 HEX ; FDABF41CO1≦X≦FFFFFFFFFF 0≦X≦2540BE3FF		—

FUNCTION		OPERATION RANGE	NORMAL ACCURACY
Statistic	DATA DEL	$\|x\| \leqq 9.999999999 \times 10^{49}$ $\|\Sigma x\| \leqq 9.999999999 \times 10^{99}$ $\Sigma x^2 \leqq 9.999999999 \times 10^{99}$ $0 \leqq n \leqq 9999999999.$ n = Integer	±1 in 10th significant digit
	$\bar{x}$	$n \neq 0$	
	σ_{n-1}	$n \neq 1,\ n \neq 0$ $0 \leqq \frac{\Sigma X^2 - \{(\Sigma X)^2 / n\}}{n-1} \leqq 9.999999999 \times 10^{99}$	
	σ_n	$n \neq 0$ $0 \leqq \frac{\Sigma X^2 - \{(\Sigma X)^2 / n\}}{n} \leqq 9.999999999 \times 10^{99}$	

MAXIMUM RATINGS (Ta = 25°C)

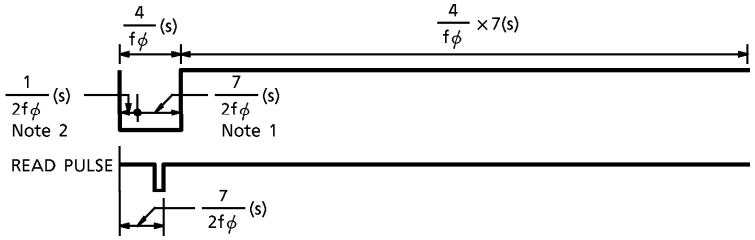
CHARACTERISTICS	SYMBOL	RATING	UNIT
Supply Voltage	V_G	+0.3~−2.2	V
Input Voltage	V_{IN}	+0.3~V_G−0.3	V
Operating Temperature	T_{opr}	0~40	°C
Storage Temperature	T_{stg}	−55~125	°C

ELECTRICAL CHARACTERISTICS (V_G = −1.5V ± 0.2V, V_{SS2} = −3.0 ± 0.4V, V_{DD} = 0V, Ta = 25°C)

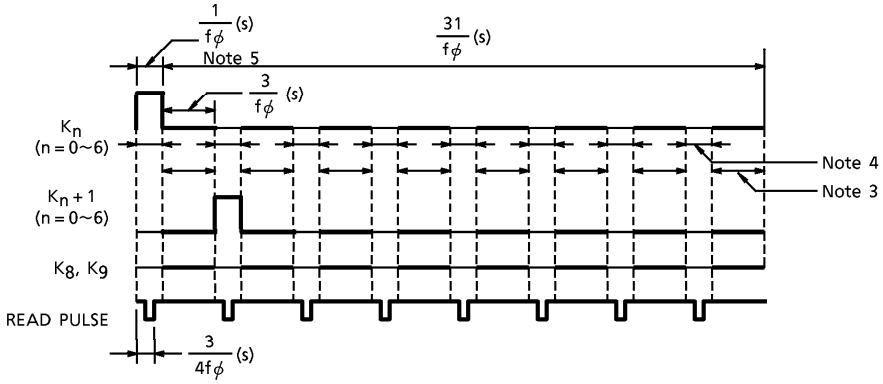
CHARACTERISTICS	SYMBOL	TEST CIR-CUIT	PIN NAME	TEST CONDITION	MIN	TYP.	MAX	UNIT
Operating Voltage	V_G	—	—	—	−1.2	−1.5	−2.0	V
Supply Current (I)	I_{DD} WAIT	—	—	V_G = −1.5V, wait	—	2.0	3.0	μA
Supply Current (II)	I_{DD} OP	—	—	V_G = −1.2V, operate	—	4.5	7.0	μA
Oscillating Frequency (I)	$F\phi$ WAIT	—	—	V_G = −1.5V, wait	5.4	9.0	12.6	kHz
Oscillating Frequency (II)	$F\phi$ OP	—	—	V_G = −1.5V, operate	14.4	24.0	33.6	kHz
Frame Frequency	f_F	—	—	V_G = −1.5V, wait	56.3	93.8	131.3	Hz
"1" Input Voltage	V_{IH}	—	K_2~K_9 RESET	—	V_G +0.4	—	V_G	V
"0" Input Voltage	V_{IL}	—	K_2~K_9 RESET	—	V_{DD}	—	−0.4	V
"1" Output Voltage	V_{OH} (I)	—	SEGMENT COM1~3	—	V_{SS2} +0.2	—	V_{SS2}	V
"0" Output Voltage	V_{OL} (I)	—	SEGMENT COM1~3	—	V_{DD}	—	−0.2	V

CHARACTERISTICS	SYMBOL	TEST CIR-CUIT	PIN NAME	TEST CONDITION	MIN	TYP.	MAX	UNIT
"M" Output Voltage	V_{OM}	—	COM1~3	—	V_{SS1} +0.2	—	V_{SS1} −0.2	V
"1" Output Voltage	V_{OH} (II)	—	K_0~K_9 RESET	—	V_{SS1} +0.2	—	V_{SS1}	V
"0" Output Voltage	V_{OL} (II)	—	K_0~K_9 RESET	—	V_{DD}	—	−0.2	V
"1" Output Resistance	R_{OH}	—	SEGMENT COM1~3	$V_{OUT} = V_{SS2} + 0.5V$	—	—	70	kΩ
"0" Output Resistance	R_{OL}	—	SEGMENT COM1~3	$V_{OUT} = -0.5V$	—	—	70	kΩ
RESET Pull Up Resistance (I)	R_{RESETH} (I)	—	RESET	$V_{OUT} = 0V$ (Note 1)	156	260	364	kΩ
RESET Pull Up Resistance (II)	R_{RESETH} (II)	—	RESET	$V_{OUT} = 0V$ (Note 2)	18	75	300	kΩ
Key Pull Up Resistance (I)	R_{KEYH} (I)	—	K_0~K_9	$V_{OUT} = V_G + 0.5V$ (Note 3)	—	—	500	kΩ
Key Pull Up Resistance (II)	R_{KEYH}	—	K_0~K_9	$V_{OUT} = 0V$ (Note 4)	60	300	1500	kΩ
Key RESET Pull Down Resistance	R_{KEYL} RESETL	—	K_0~K_9 RESET	$V_{OUT} = -0.5V$ (Note 5)	—	—	25	kΩ

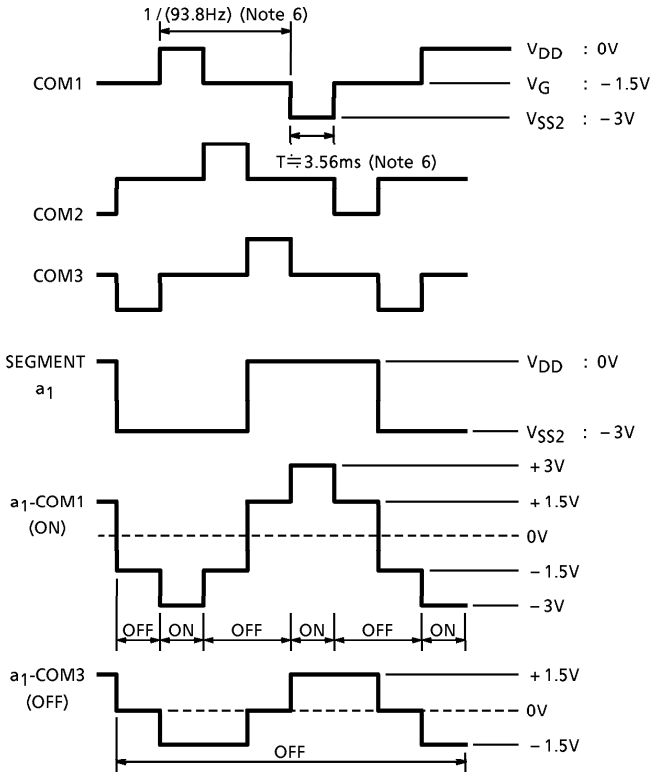
(Note 1, 2, 5) RESET Waveform, 1-cycle



(Note 3, 4, 5) KEY Waveform, 1-cycle



WAVEFORMS FOR DISPLAY



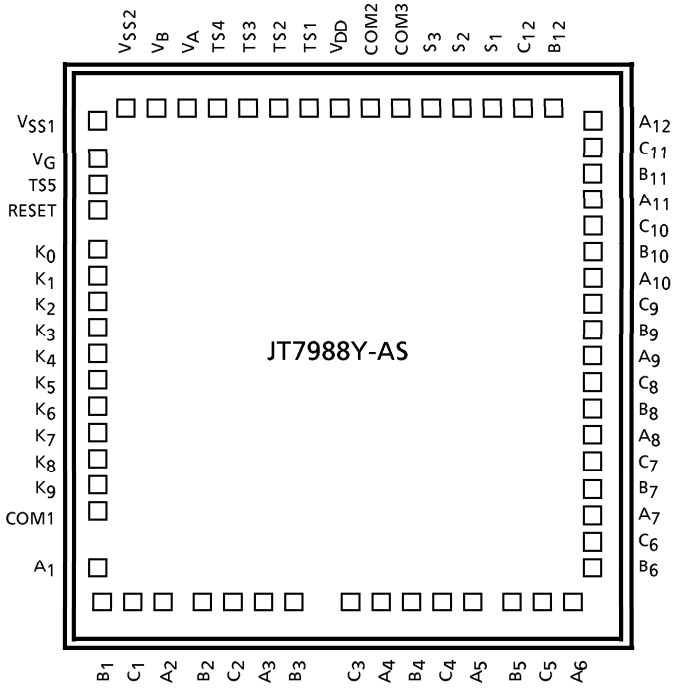
(Note 6) : Fϕ WAIT = 9kHZ

PAD LOCATION TABLE (μm)

NAME	X POINT	Y POINT
V_{SS2}	– 1215	1536
V_{SS1}	– 1404	1494
VG	– 1404	1260
TS5	– 1404	1059
RESET	– 1404	873
K_0	– 1404	612
K_1	– 1404	450
K_2	– 1404	288
K_3	– 1404	126
K_4	– 1404	– 36
K_5	– 1404	– 198
K_6	– 1404	– 360
K_7	– 1404	– 522
K_8	– 1404	– 684
K_9	– 1404	– 846
COM1	– 1404	– 1008
A_1	– 1404	– 1377
B_1	– 1326	– 1539
C_1	– 1164	– 1539
A_2	– 1002	– 1539
B_2	– 758	– 1539
C_2	– 596	– 1539
A_3	– 434	– 1539
B_3	– 272	– 1539
C_3	127	– 1539
A_4	289	– 1539
B_4	451	– 1539
C_4	613	– 1539
A_5	775	– 1539
B_5	1002	– 1539
C_5	1164	– 1539
A_6	1326	– 1539

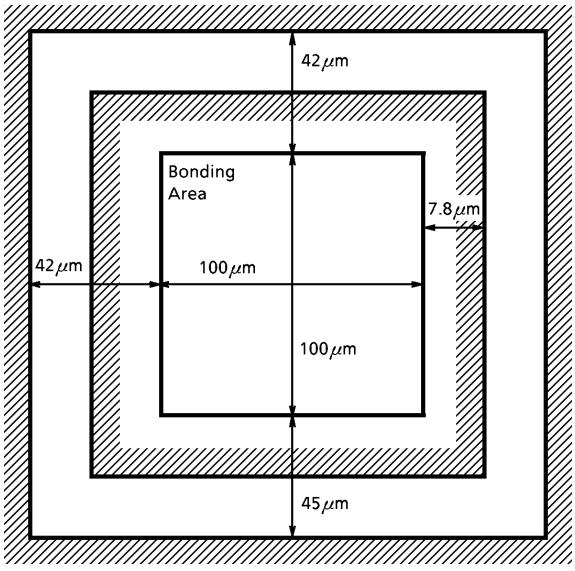
NAME	X POINT	Y POINT
B_6	1404	– 1377
C_6	1404	– 1170
A_7	1404	– 1008
B_7	1404	– 846
C_7	1404	– 684
A_8	1404	– 522
B_8	1404	– 360
C_8	1404	– 198
A_9	1404	– 36
B_9	1404	126
C_9	1404	288
A_{10}	1404	450
B_{10}	1404	612
C_{10}	1404	774
A_{11}	1404	936
B_{11}	1404	1098
C_{11}	1404	1260
A_{12}	1404	1494
B_{12}	1215	1536
C_{12}	1053	1536
S_1	869	1536
S_2	707	1536
S_3	545	1536
COM3	383	1536
COM2	218	1536
V_{DD}	0	1536
TS1	– 218	1536
TS2	– 380	1536
TS3	– 542	1536
TS4	– 729	1536
VA	– 891	1536
VB	– 1053	1536

CHIP LAYOUT



Chip size : 3.08×3.41 [mm]
Chip thickness : 450±20 [μm]
Substrate : V_{DD}

PAD LAYOUT

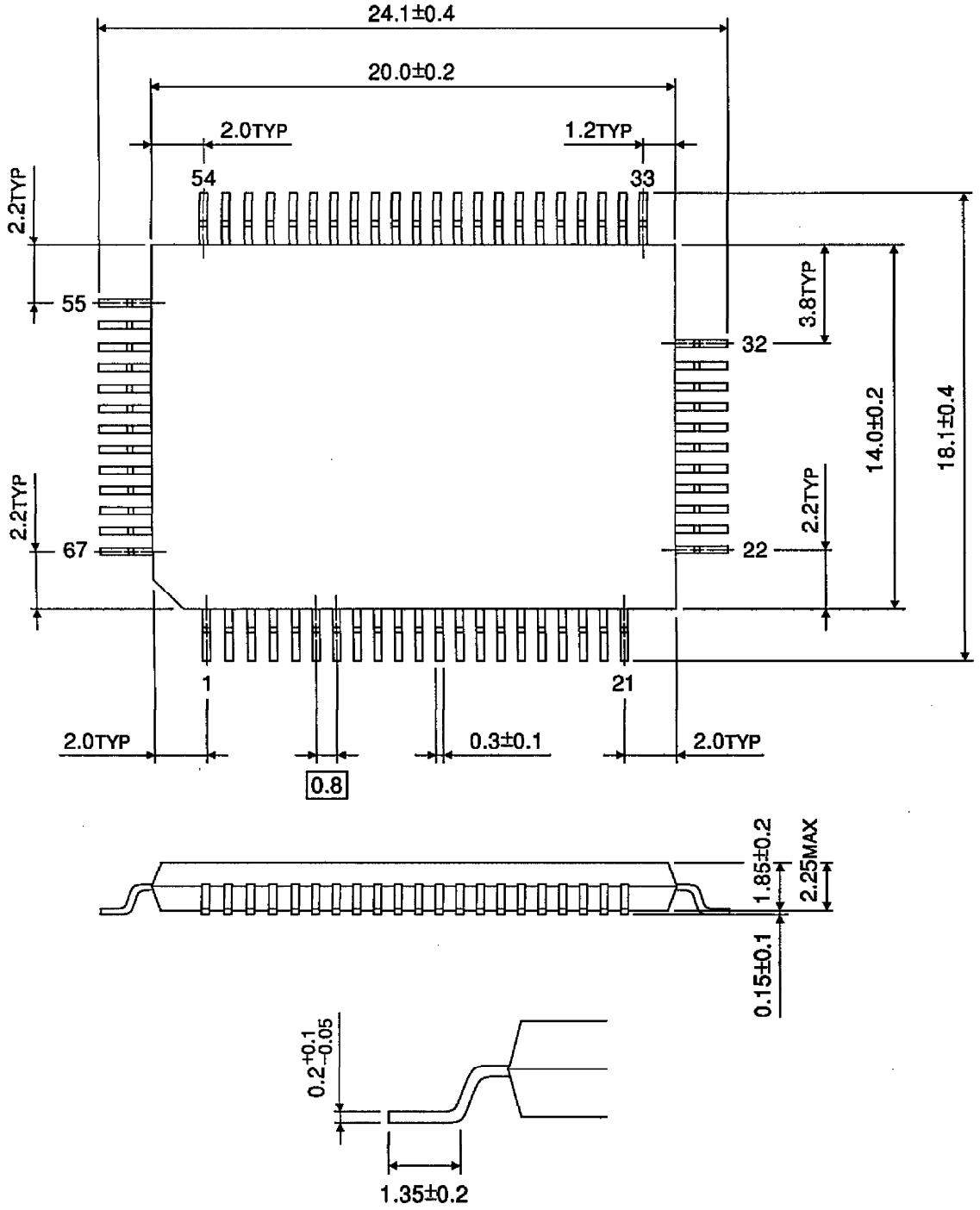


Scribe Line

PAD Pitch 162μm

PACKAGE DIMENSIONS

QFP67-P-1420-0.80 Unit : mm



Weight : 1.20g (Typ.)

General Specification for Bare Calculator LSI Chip

1. Purpose

This is to specify the quality standard for integrated circuits produced by TOSHIBA CORPORATION (hereinafter referred to as VENDOR) which are to be delivered to PURCHASER.

2. Definition

This specification applies only to the bare calculator LSI chips produced by VENDOR and purchased by PURCHASER and defines the general specification items.

3. Priority of specifications

When there are discrepancies in or questions arising from the specifications and instructions provided by VENDOR, the following documents shall apply, in the priority order shown.

1) Individual specifications for the bare calculator LSI chip
(both PURCHASER and VENDOR should refer to the technical data sheet for the relevant product.)
2) General specifications for the bare calculator LSI chip
3) Other related specifications and standards

4. Characteristics

To be shown in the individual specification sheets.
The individual specifications shall consist of the following four items.

1) Rating specifications
2) Electrical characteristics
3) Pin configuration and mechanical dimensions
4) Others

5. Inspection of product for delivery

5.1 Inspection lot

a) The inspection lot shall consist of products produced using the same material, working from the same design, via the same production process, using the same facilities, with the same assured quality and using the same quality assurance method; the lot number shall be put on all trays to allow tracing of the lot history.

b) The products in an inspection lot number should all be taken from the same VENDOR's lot number.

5.2 Sampling plan

Statistical sampling and inspection shall be in accordance with MIL-STD-105D single sampling plans for normal inspections, general inspection level Ⅱ.

The acceptable quality level (AQL) shall be as specified in the following table:

TEST	AQL (%)
Electrical	2.5
Visual	4.0

5.3 Electrical criteria

Criteria for electrical characteristics are prescribed in Attachment-1.

5.4 Visual criteria

Visual criteria are prescribed in Attachment-2.

6. Incoming inspection

6.1 General

a) PURCHASER's incoming inspection should be done within 15 days of PURCHASER receiving the products.

b) PURCHASER shall report the results of incoming inspection to VENDOR and provide VENDOR with detailed data of failure rate, quoting VENDOR's lot number for failed products, if VENDOR demands a report from PURCHASER.

6.2 Inspection procedure

PURCHASER should perform his incoming inspection according to the following procedure.

a) First: Visual inspection should be carried out

b) Second: Electrical and other inspections should be carried out before PURCHASER's manufacturing process is started.

7. Treatment for defective lots and products

Defective lots and defective products which are found in PURCHASER's incoming inspection can be returned to VENDOR with detailed description of failures.
However, if VENDOR does not receive the defective items within 30 days of PURCHASER's incoming inspection, VENDOR is absolved of responsibility for defects.

8. Packing and labeling

a) Dies shall be placed in die tray in order with the top metal surface facing up.

b) A pile consists of five trays and several piles are packed in a package. These piles and packages have printed labels on them as shown below.

Date	
Name	
Lot No.	
Net	
TOSHIBA MADE IN JAPAN	

c) PURCHASER shall return these packing materials to VENDOR at VENDOR's request.

9. Storage criteria

Solid state chips, unlike packaged devices, are non-hermetic devices and are normally fragile and small in size. They therefore, require special handling considerations as follows:

9.1 Chips must be stored under proper conditions to ensure that they are not subjected to a moist and/or contaminated atmosphere that will alter their electrical, physical or mechanical characteristics.
After the shipping container is opened, the chips must be stored under the following conditions:

A. Storage temperature: 40°C max
B. Relative humidity: 50% max
C. Clean, dust-free environment

9.2 The user must exercise proper care when handling chips or wafers so as to prevent even the slightest physical damage to the chip.

9.3 During chip-mounting and leads bonding the user must use proper assembly techniques to obtain proper electrical, thermal and mechanical performance.

9.4 After the chip has been mounted and the leads bonded, all necessary procedures must be followed by the user to ensure that these non-hermetic chips are not subjected to a moist or contaminated atmosphere which might cause the development of electrical conductive paths across the relatively small insulating surfaces.
In addition, proper consideration must be given to the protection of these devices from other harmful environmental factors which could conceivably adversely affect their proper performance.

10. Handling criteria

The user should find the following suggested precautions helpful when handling chips.
In any event, because of the extremely small size and the fragile nature of chips, care should be taken when handling these devices.

10.1 Grounding

a) Bonders, pellet pick-up tools, table tops, trimming and forming tools, sealing equipment and any other equipment used in chip handling should be properly grounded.

b) The operator should be properly grounded.

10.2 In-process handling

a) Assemblies or sub-assemblies of chips should be transported and stored in conductive carriers.

b) All external leads on the assemblies or sub-assemblies should be shorted together.

11. Visual Inspection Criteria

11.1 Visual inspection magnification shall be 40×

11.2 Defects defined:

11.2.1 Thickness

See individual specifications in the technical data sheets.

11.2.2 Chips and cracks

A die shall be rejected if:

Any crack or chip extends for more than a length of 35 μm inside the scribe line (see Figure 1).

11.2.3 Metallization

A die shall be rejected if:

a) more than 25% of the metallization of any bonding pad is missing.

b) there is a short or break which affects electrical characteristics in any lead pattern (see Figure 2).

11.2.4 Glass protection coat

A die shall be rejected if:

The glass protection coat covers more than 25% of any bonding pad.

11.2.5 Attached foreign material

A die shall be rejected if:

a) a die is covered by stains or attached foreign material the area of which is greater than five times the bonding pad area.

b) it exhibits residual ink, stains or attached foreign material which cover more than 20% of any active bonding pad (see Figure 3).

11.2.6 Others

A die shall be rejected if:

a) there are no probe needle scratches on any of the bonding pads.

b) if it has been marked with ink.

11.3 Parameter limits for samples should be applied as necessary

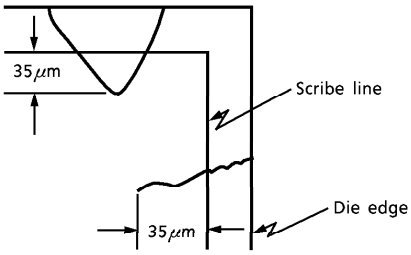


Figure 1

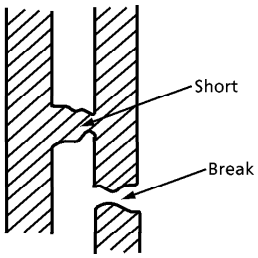


Figure 2 Lead pattern

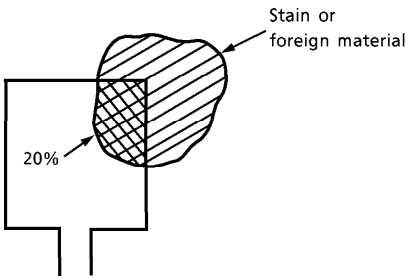
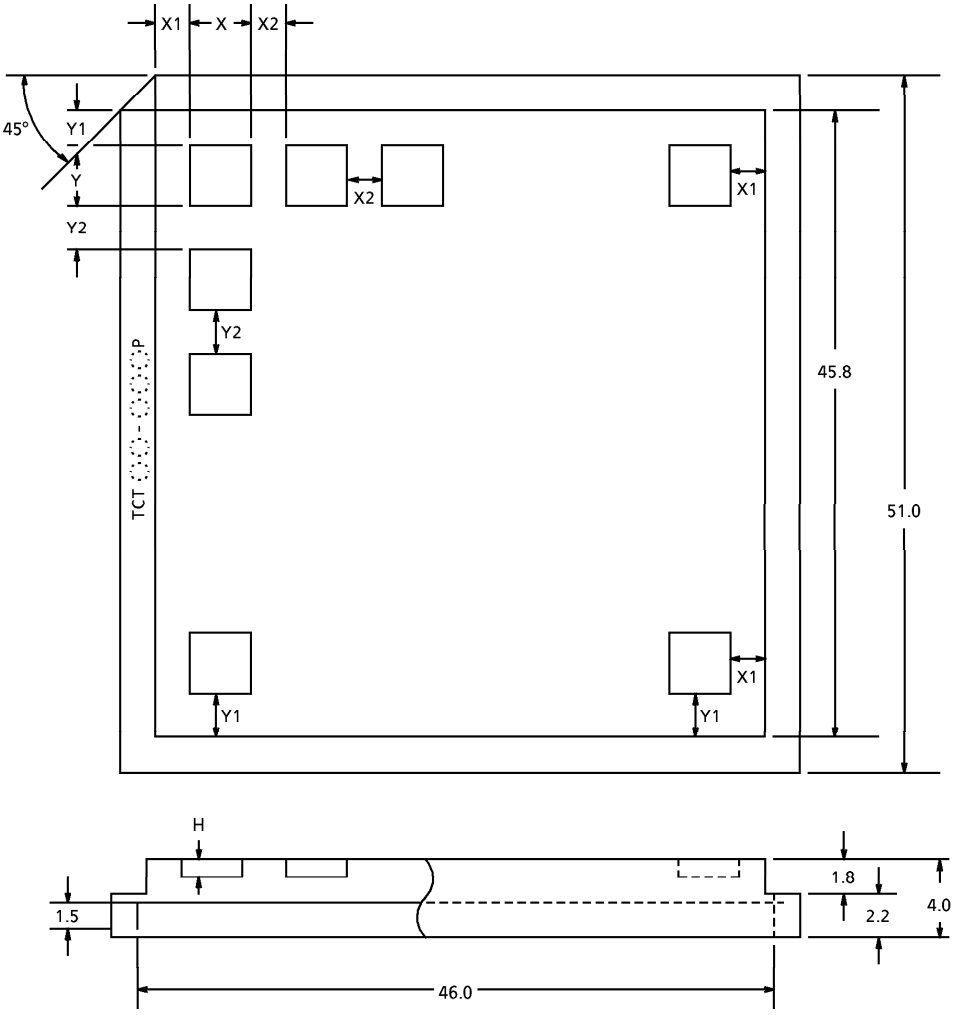


Figure 3

External Dimensions of Chip Tray



Please select a tray name from the table according to the chip size:

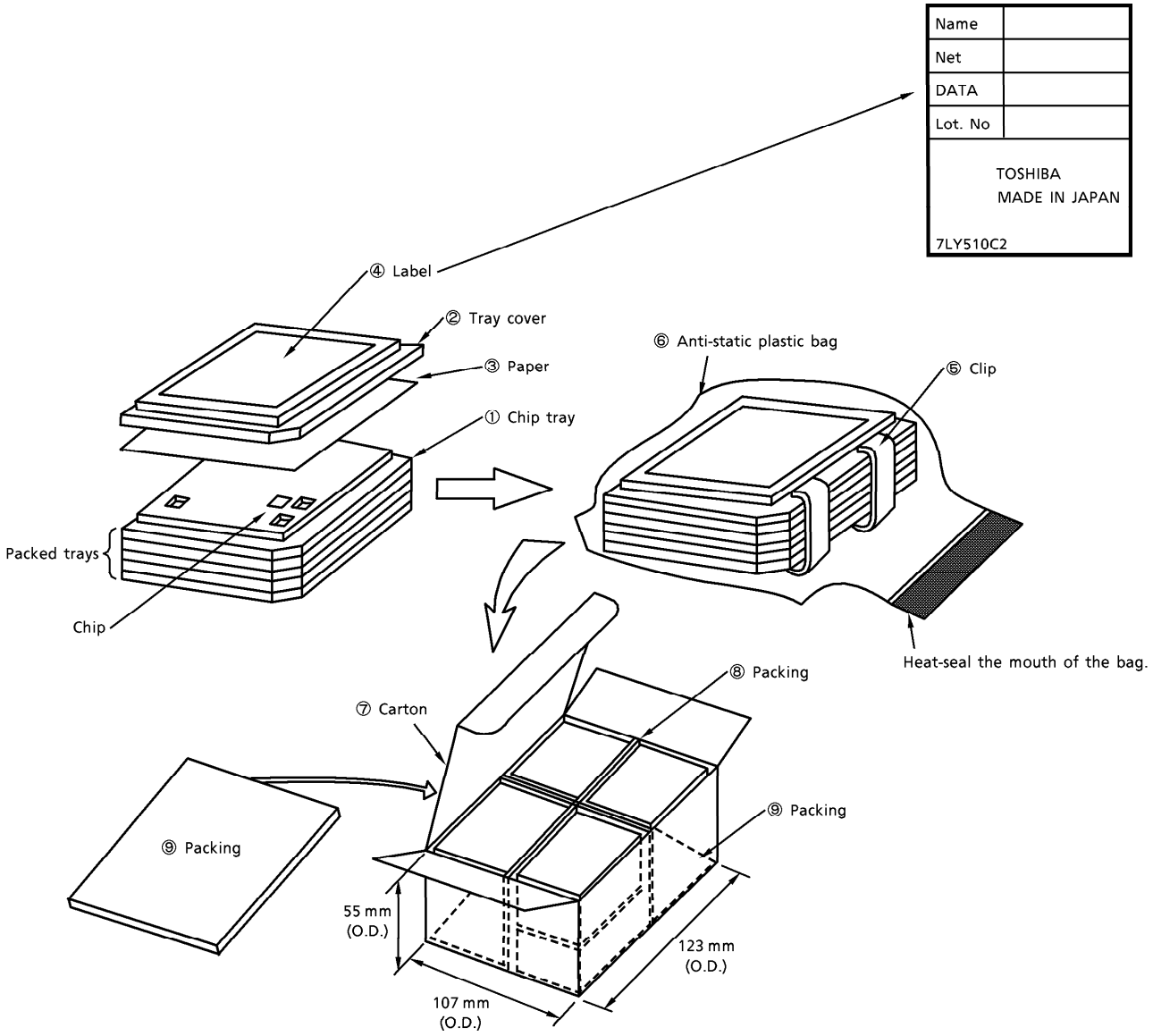
Unit: mm

Tray name	X	Y	H	No. of pockets (pcs)	X1	X2	Y1	Y2
TCT28-060P	2.80	2.80	0.60	10×10 (100)	1.700	1.800	1.700	1.600
TCT33-060P	3.30	3.30	0.60	10×10 (100)	1.900	1.000	1.900	1.000
TCT38-060P	3.80	3.80	0.60	10×10 (100)	1.200	0.600	1.200	0.600
TCT45-060P	4.50	4.50	0.60	7×7 (49)	2.050	1.700	2.050	1.700
TCT53-060P	5.30	5.30	0.60	7×7 (49)	1.350	1.000	1.350	1.000

Tray material:

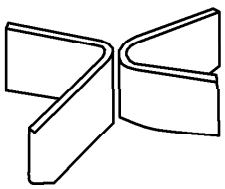
Carbon-bearing polypropylene

Packing Method 1



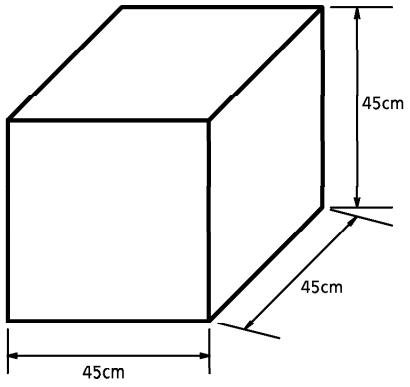
Place eight bags of chip trays in each carton ⑦. Lay one sheet of packing (7UF44F) ⑨ on top before closing the lid of the carton (see the diagram above).

Prepare the packing ⑧ by cutting a sheet of 7UF44F into halves and folding each half in half as shown below; use these halves as inner partitions.



Packing Method 2

Shipping box



- Inner box : Containing 20 boxes
- Weight : Approx. 15 kg (including packing material)
- Material : Corrugated cardboard
- IC contents : 36 × 5 × 8 × 20 = 28.800 pcs