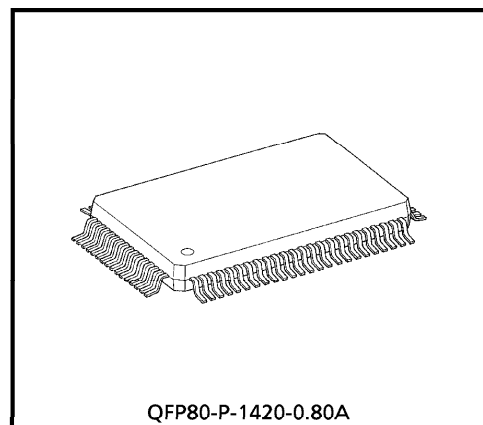


TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

T6M74A, JT6M74A-AS

T6M74A, JT6M74A-AS CMOS SINGLE-CHIP LSI FOR LCD CALCULATOR

The T6M74A, JT6M74A-AS is a CMOS single-chip microcomputer for 16-digit 1-memory calculator. T6M74A, JT6M74A-AS is the complete single-chip CMOS LSI for calculator with single power supply operation. Wide operating voltage range and low-power consumption make it suitable for 1.5 V solar battery operated. Besides T6M74A, JT6M74A-AS can selectable with a pin-programmable to function of Power timer and Memory hold. With the following features.



Weight : 1.52 g (Typ.)

FEATURES

- Display : 16 digits of data, 1 digit of sign, error symbol, memory load symbol.
- Algebraic mode.
- Standard 4 functions (+, -, ×, ÷)
- Automatic percentage operation with add-on, discount.
- Automatic delta percentage, mark-up and markdown operations.
- Square root.
- Constant calculation.
- Chain calculation.
- Change sign.
- Floating point or momentary mode (selectable with a switch).
- Fixed point ("0", "1", "2", "3", "4" or "6" places) or floating point (selectable with a switch).
- Adding point mode (selectable with a switch).

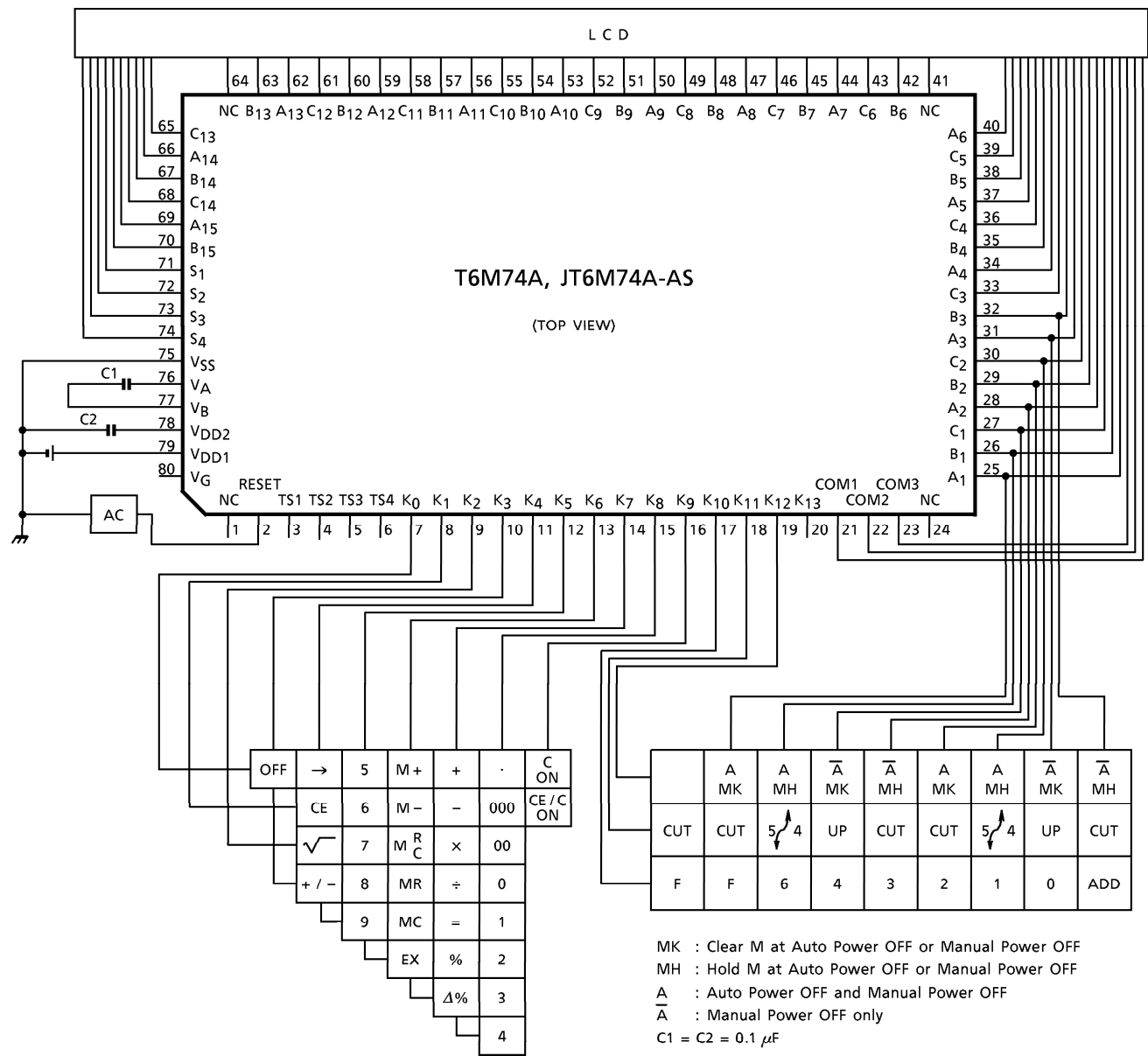
980910EBA2

- TOSHIBA is continually working to improve the quality and the reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to observe standards of safety, and to avoid situations in which a malfunction or failure of a TOSHIBA product could cause loss of human life, bodily injury or damage to property. In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent products specifications. Also, please keep in mind the precautions and conditions set forth in the TOSHIBA Semiconductor Reliability Handbook.
- The products described in this document are subject to the foreign exchange and foreign trade laws.
- The information contained herein is presented only as a guide for the applications of our products. No responsibility is assumed by TOSHIBA CORPORATION for any infringements of intellectual property or other rights of the third parties which may result from its use. No license is granted by implication or otherwise under any intellectual property or other rights of TOSHIBA CORPORATION or others.
- The information contained herein is subject to change without notice.

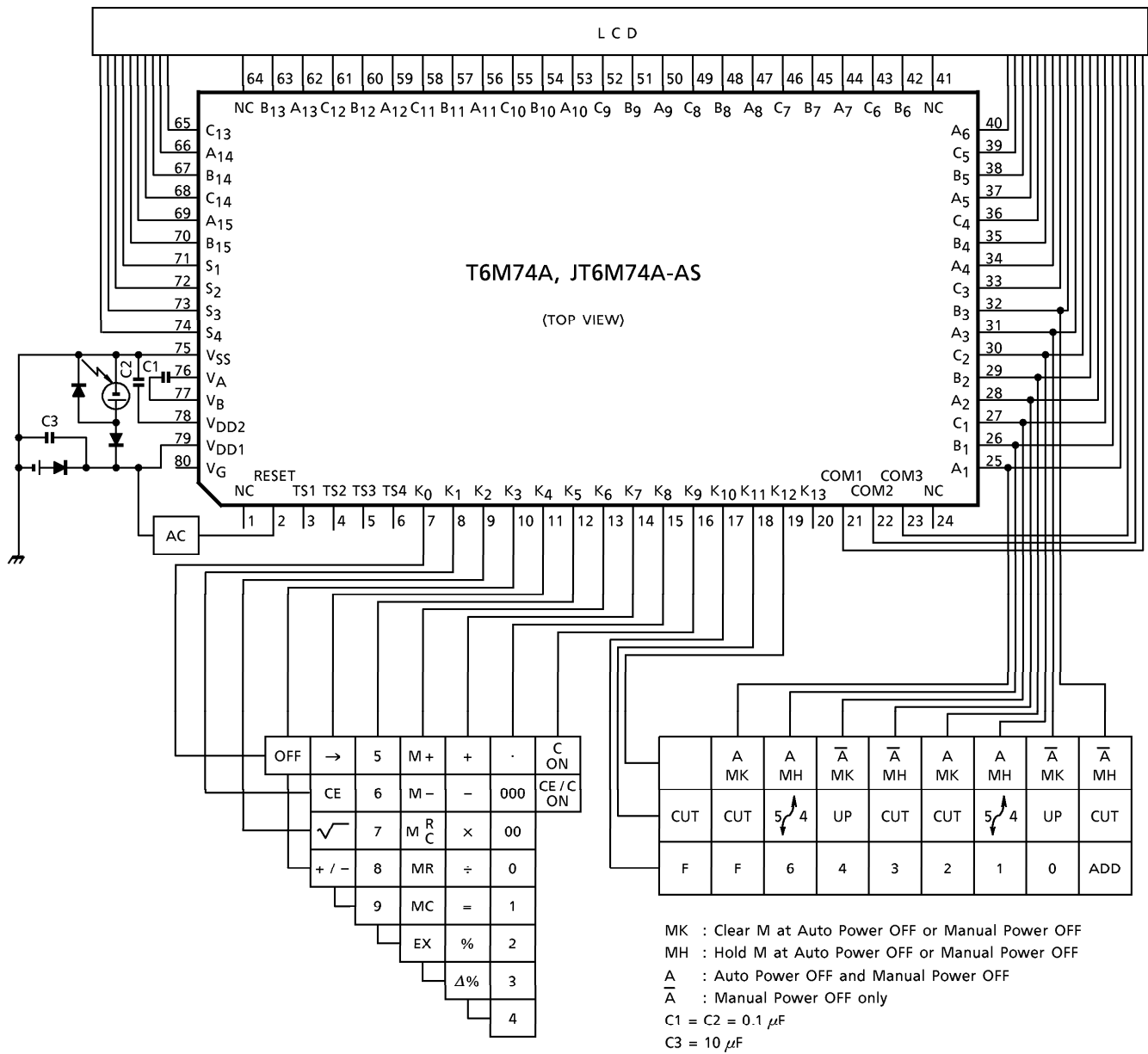
- Rounding switches (rounding up, down and off).
- Leading zero suppression.
- Trailing zero suppression.
- Punctuation on display, commas for thousands.
- Memory contents indicator, turned on with non-zero in the memory.
- Registration overflow, indicating that too many digits are entered (the most significant digit are protected).
- Result overflow, indicating during calculation (most function key are locked as it happened).
- Memory overflow indicating to flashing of memory load mark.
- Key roll over function.
- Floating minus.

SYSTEM BLOCK DIAGRAM

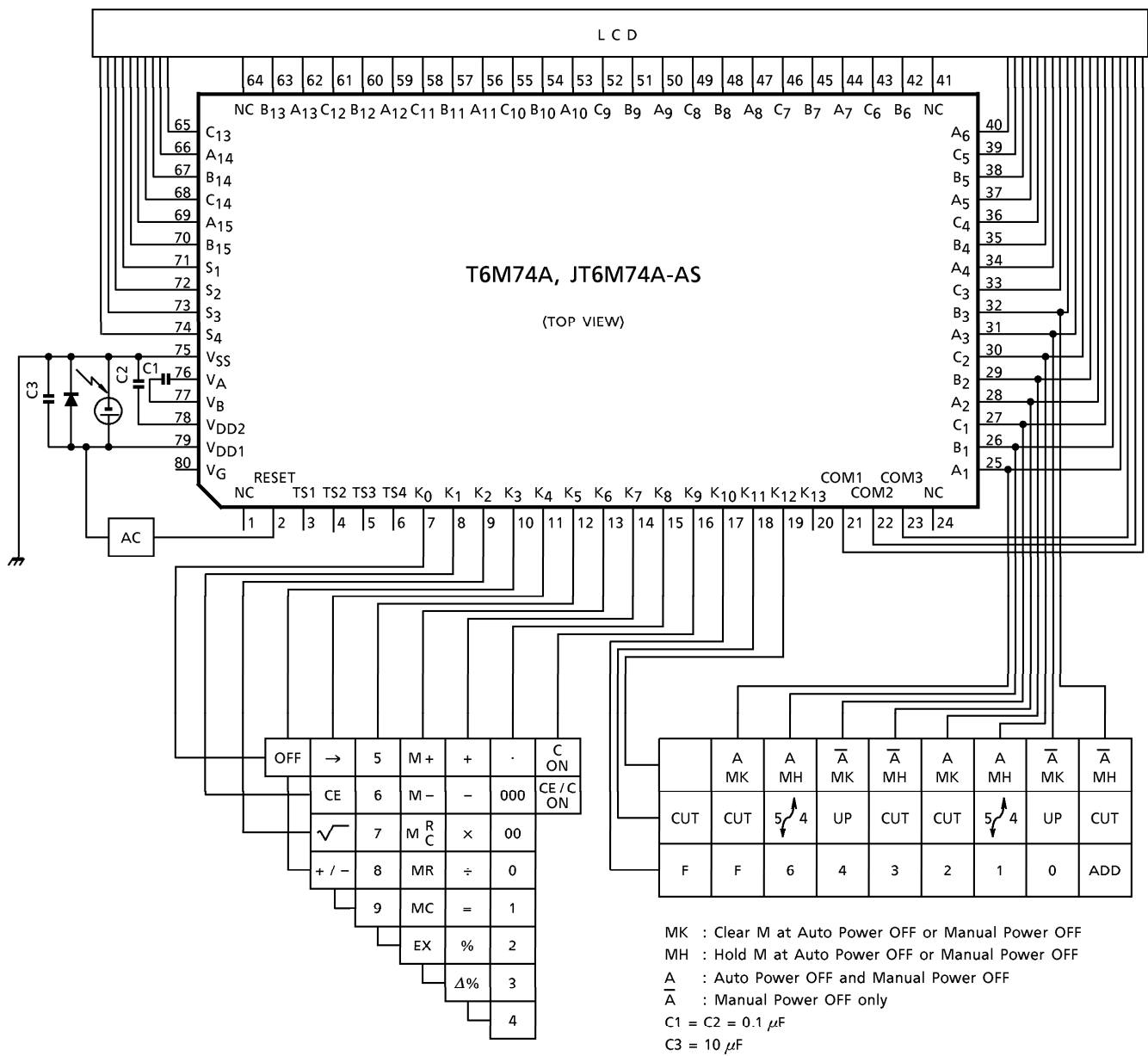
Battery Type



Dual Type

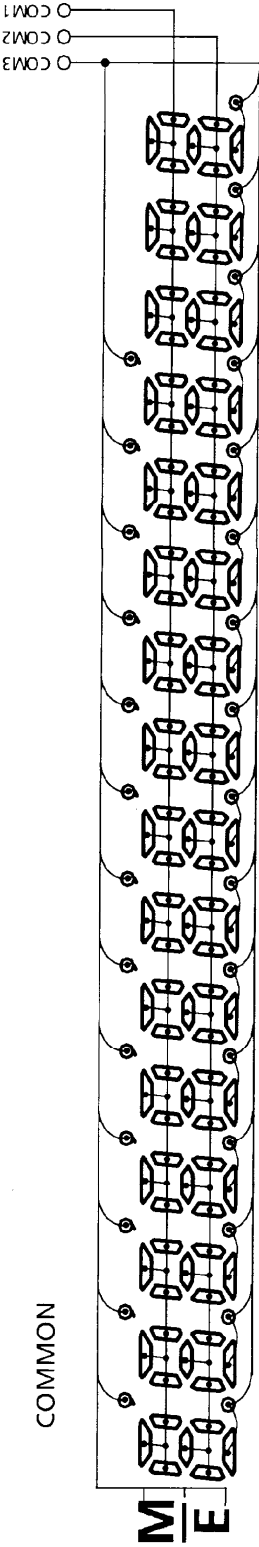
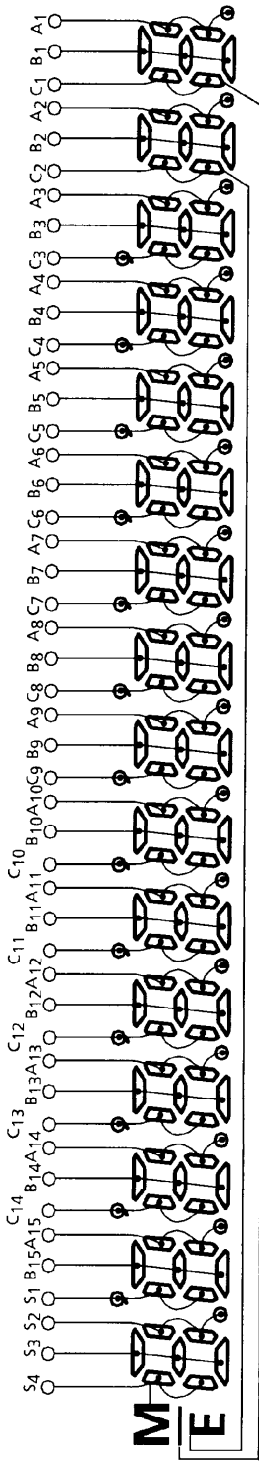


Solar Type



CONNECTION OF LCD

SEGMENT



T6M74A, JT6M74A-AS-06

The diagram illustrates a 10-bit programmable logic device (PLD) architecture. It features a grid of logic blocks connected by a network of lines. The blocks are labeled with functions such as OFF, CE, $\sqrt{\quad}$, $+/-$, 5, 6, 7, 8, 9, M+, M-, M^R_C, MR, MC, EX, M-, -, $\times$, $\div$, =, %, $\Delta\%$, and C ON. The blocks are connected to a network of lines labeled K0 through K9. A separate block labeled AC is connected to VDD1 and RESET.

Figure 1 shows a 3x9 grid of logic blocks for a 32-bit ALU. The columns are labeled with inputs: OPEN, A₁, B₁, C₁, A₂, B₂, C₂, A₃, B₃. The rows are labeled with control signals: K₁₂, K₁₁, K₁₀. The blocks contain various logic functions and constants, such as (Note), A, MK, A, MH, $\bar{A}$, MK, $\bar{A}$, MH, A, MK, A, MH, $\bar{A}$, MK, $\bar{A}$, MH, F, 6, 4, 3, 2, 1, 0, and ADD. Arrows indicate data flow between blocks and to the outputs.

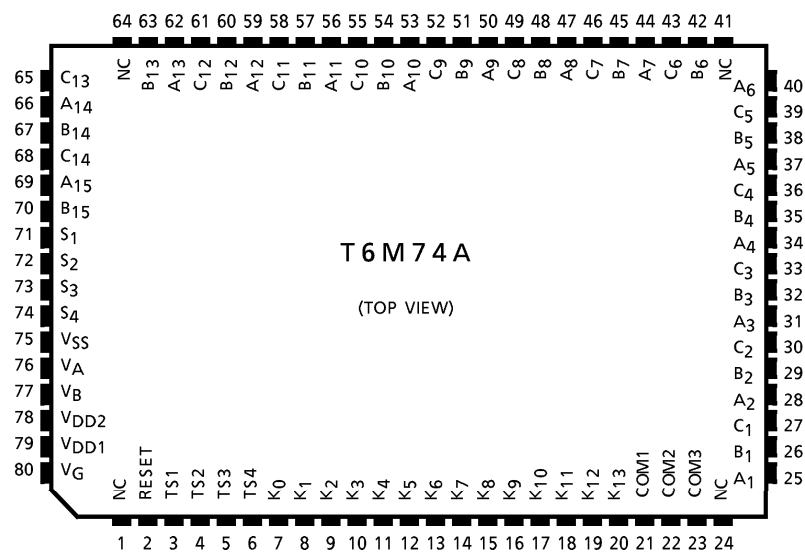
K₁₂ Selectable with Auto Power OFF mode an Memory Hold Status.
MH (Memory Hold), MK (Memory Kill)

K₁₁ Rounding

K₁₀ Selectable with Fixed point or Floating mode.

K12 line is No choose at the system power on then initial condition is A, MH Mode selected.

PIN ASSIGNMENT



SPECIFICATION OF CALCULATOR

Speed of calculation

Numeral		27.8~40.9 ms
Function	{ 1 $\boxed{+}$	42.7 ms
	{ 1 $\boxed{+}$ 2 $\boxed{+}$	83.9 ms
Addition and subtract	{ 123 $\boxed{+}$ 1 $\boxed{=}$	82.8 ms
	{ 9999999999999999 $\boxed{-}$ 0.0000000000000001 $\boxed{=}$	106.4 ms
Multiply	{ 123 $\boxed{\times}$ 2 $\boxed{=}$	110.8 ms
	{ 1 $\boxed{\times}$ 9999999999999999 $\boxed{=}$	309.9 ms
Device	{ 123 $\boxed{\div}$ 3 $\boxed{=}$	165.1 ms
	{ 9999999999999999 $\boxed{\div}$ 1 $\boxed{=}$	348.4 ms
Memory calculation	{ 2 $\boxed{M+}$	93.8 ms
	{ 9999999999999999 $\boxed{\div}$ 1 $\boxed{M+}$	388.1 ms
Square root	{ 9999999999999999 $\boxed{\sqrt{}}$	259.7 ms
	{ 2 $\boxed{\sqrt{}}$	170.2 ms

Operation example

1. Fixed point calculations

①	Key	Display	Fixed point place	②	Key	Display	Fixed point place
	C	0.	DP = 3 (5 / 4)		C	0.	DP = 0 (↱)
	2	2.			1	1.	
	÷	2.			•	1.	
	3	3.			2	1.2	
	=	0.667			3	1.23	
	2	2.			+	1.23	
	•	2.			1	1.	
	3	2.3			•	1.	
	+	2.3			1	1.1	
	4	4.			=	3.	
	M +	6.300			9	9.	
	1	1.			√	3.	
	•	1.			×	3.	
	2	1.2			1	1.	
	M +	1.200			•	1.	
	MR	7.5	DP = 4		1	1.1	DP = F
					=	3.3	

2. Adding point mode calculations

Key	Display	Key	Display	Key	Display
$\boxed{C}$	0.	$\boxed{M+}$	0.02M	$\boxed{=}$	33.27M –
1	1.	3	3.M	2	2.M
23	123	$\boxed{\cdot}$	3.M	$\boxed{+}$	0.02M
$\boxed{+}$	1.23	123	3.123M	9	9.M
3	3.	$\boxed{M+}$	3.12M	$\boxed{\cdot}$	9.M
$\boxed{=}$	1.26	$\boxed{MR}$	3.14M	$\boxed{\sqrt{}}$	3.M
3	3.	$\boxed{C}$	0.M	$\boxed{=}$	3.02M
2	32.	1	1.M		
$\boxed{\times}$	32.	23	123M		
3	3.	$\boxed{-}$	1.23M		
$\boxed{\cdot}$	3.	3	3.M		
000	3.000	4	34.M		
$\boxed{=}$	96.00	$\boxed{\cdot}$	34.M		
2	2.	5	34.5M		

3. Constant calculations

① Multiplication

Key	Display	Constant
k	k	
$\boxed{\times}$	k	
a	a	
$\boxed{=}$	k·a	k ×
b	b	k ×
$\boxed{=}$	k·b	k ×

③ Addition

a	a	
$\boxed{+}$	a	
k	k	
$\boxed{=}$	a + k	+ k
b	b	+ k
$\boxed{=}$	b + k	+ k

② Division

Key	Display	Constant
a	a	
$\boxed{\div}$	a	
k	k	
$\boxed{=}$	a / k	÷ k
b	b	÷ k
$\boxed{=}$	b / k	÷ k

④ Subtraction

a	a	
$\boxed{-}$	a	
k	k	
$\boxed{=}$	a – k	– k
b	b	– k
$\boxed{=}$	b – k	– k

⑤ Percentage

Key	Display	Constant
k	k	
$\boxed{\times}$	k	
a	a	
$\boxed{\%}$	$k \cdot a / 100$	$k \times$
b	b	$k \times$
$\boxed{\%}$	$k \cdot b / 100$	$k \times$

⑦ Add-on

k	k	
$\boxed{+}$	k	
a	a	
$\boxed{\%}$	$k \cdot (1 + a / 100)$	$k +$
b	b	$k +$
$\boxed{\%}$	$k \cdot (1 + b / 100)$	$k +$

4. $\Delta\%$ calculations

① Key Display

a	a
$\boxed{+}$	a
b	b
$\boxed{\Delta\%}$	$100 \cdot (a + b) / b$

5. Mark-up, mark-down calculations

① Mark-up

Key	Display
a	a
$\boxed{\div}$	a
b	b
$\boxed{\Delta\%}$	$a / (1 - b / 100)$
$\boxed{\Delta\%}$	$ a / (1 - b / 100) $

⑥ Percentage

Key	Display	Constant
a	a	
$\boxed{\div}$	a	
k	k	
$\boxed{\%}$	$100 \cdot a / k$	$\div k$
b	b	$\div k$
$\boxed{\%}$	$100 \cdot b / k$	$\div k$

⑧ Discount

k	k	
$\boxed{-}$	k	
a	a	
$\boxed{\%}$	$k \cdot (1 - a / 100)$	$k -$
b	b	$k -$
$\boxed{\%}$	$k \cdot (1 - b / 100)$	$k -$

② Key Display

a	a
$\boxed{-}$	a
b	b
$\boxed{\Delta\%}$	$100 \cdot (a - b) / b$

② Mark-down

Key	Display
a	a
$\boxed{\div}$	a
b	b
$\boxed{+/-}$	-b
$\boxed{\Delta\%}$	$a / (1 + b / 100)$
$\boxed{\Delta\%}$	$a / (1 + b / 100) - a$

6. Add-on, discount calculations

Add-on

Key	Display
① a	a
$\times$	a
b	b
$\%$	$a \cdot b / 100$
+	$a \cdot b / 100$
=	$a (1 + b / 100)$
③ a	a
+	a
b	b
$\%$	$a (1 + b / 100)$
⑤ a	a
$\times$	a
b	b
$\Delta\%$	$a \cdot (1 + b / 100)$

Discount

Key	Display
② a	a
$\times$	a
b	b
$\%$	$a \cdot b / 100$
-	$a \cdot b / 100$
=	$a (1 - b / 100)$
④ a	a
-	a
b	b
$\%$	$a (1 - b / 100)$
⑥ a	a
$\times$	a
b	b
+/-	- b
$\Delta\%$	$a (1 - b / 100)$

MAXIMUM RATINGS

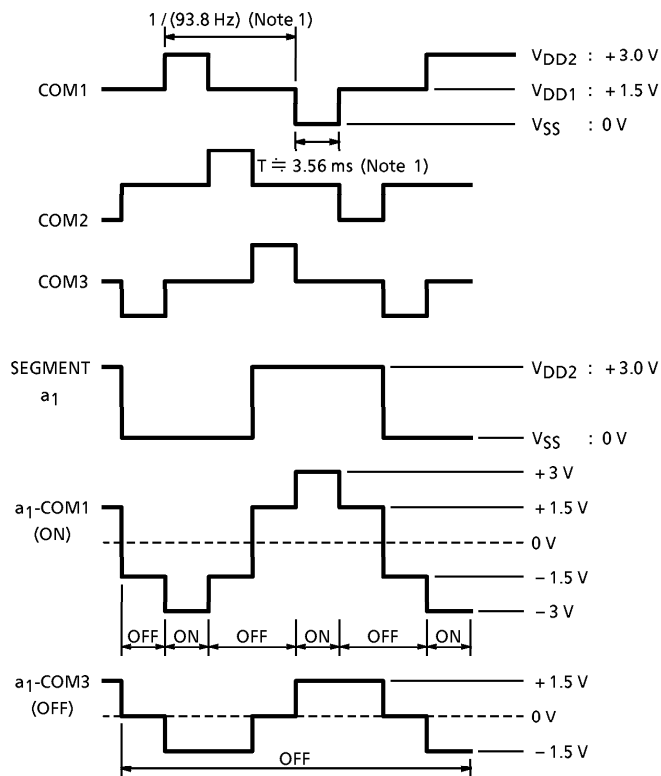
CHARACTERISTICS	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD1}	$-0.3 \sim 2.0$	V
Input Voltage	V_{IN}	$-0.3 \sim V_{DD1} + 0.3$	V
Operating Temperature	T_{opr}	$0 \sim 40$	°C
Storage Temperature	T_{stg}	$-55 \sim 125$	°C

ELECTRICAL CHARACTERISTICS ($V_{DD1} = 1.5 \pm 0.2$ V, $V_{DD2} = 3.0 \pm 0.4$ V, $V_{SS} = 0$ V, $T_a = 25^\circ\text{C}$)

CHARACTERISTICS	SYMBOL	TEST CIR-CUIT	PIN NAME	TEST CONDITION	MIN	TYP.	MAX	UNIT
Operating Voltage	V_{DD1}	—	—	—	1.2	1.5	2.0	V
"1" Input Voltage	$V_{IH}(1)$	—	K ₂ ~K ₉ RESET	—	$V_{DD1} - 0.4$	—	V_{DD1}	V
"1" Input Voltage	$V_{IH}(2)$	—	K ₁₀ ~K ₁₃	—	$V_{DD2} - 0.4$	—	V_{DD2}	V
"0" Input Voltage	V_{IL}	—	K ₂ ~K ₁₃ RESET	—	0	—	0.4	V
"1" Output Voltage	$V_{OH}(1)$	—	SEGMENT COM1~3	—	$V_{DD2} - 0.2$	—	V_{DD2}	V
"0" Output Voltage	$V_{OL}(1)$	—	SEGMENT COM1~3	—	0	—	0.2	V
"M" Output Voltage	V_{OM}	—	COM1~3	—	$V_{DD1} - 0.2$	—	$V_{DD1} + 0.2$	V
"1" Output Voltage	$V_{OH}(2)$	—	K ₁ ~K ₉	—	$V_{DD1} - 0.2$	—	V_{DD1}	V
"0" Output Voltage	$V_{OL}(2)$	—	K ₁ ~K ₁₃	—	0	—	0.2	V
"1" Output Resistance	R_{OH}	—	SEGMENT COM1~3	$V_{OUT} = V_{DD2} - 0.5$ V	—	—	70	k Ω
"0" Output Resistance	R_{OL}	—	SEGMENT COM1~3	$V_{OUT} = 0.5$ V	—	—	70	k Ω
KEY Pull Up Resistance	$R_{KEYH}(1)$	—	RESET	$V_{OUT} = V_{DD1} - 0.5$ V	—	—	25	k Ω
	$R_{KEYH}(2)$	—	K ₀ ~K ₉	$V_{OUT} = V_{DD1} - 0.5$ V	—	—	14	k Ω
	$R_{KEYH}(3)$	—	K ₁₀ ~K ₁₃	$V_{OUT} = 0$ V	120	—	800	k Ω
KEY Pull Down Resistance	$R_{KEYL}(1)$	—	RESET (1)	$V_{OUT} = V_{DD1}$	100	—	300	k Ω
	$R_{KEYL}(2)$	—	RESET (2)	$V_{OUT} = V_{DD1}$	18	—	300	k Ω
	$R_{KEYL}(3)$	—	K ₀ ~K ₉ (1)	$V_{OUT} = 0.5$ V	—	—	50	k Ω
	$R_{KEYL}(4)$	—	K ₀ ~K ₉ (2)	$V_{OUT} = V_{DD1}$	72	—	170	k Ω
Oscillating (WAIT)	$f_{\phi WAIT}$	—	—	$V_{DD1} = 1.5$ V	5.4	9.0	15.5	kHz
Frequency (OPERATE)	$f_{\phi OP}$	—	—	$V_{DD1} = 1.5$ V	20.0	34	61.3	kHz
Frame Frequency	f_F	—	SEGMENT COM1~3	$V_{DD1} = 1.5$ V	56.3	93.8	161.5	Hz

CHARACTERISTIC		SYMBOL	TEST CIR- CUIT	PIN NAME	TEST CONDITION	MIN	TYP.	MAX	UNIT
Supply Current	1 (WAIT)	I_{DDWAIT}	—	—	$V_{DD1} = 1.5\text{ V}$	—	—	3.3	μA
	2 (OPERATE)	I_{DDOP}	—	—	$V_{DD1} = 1.2\text{ V}$	—	—	8.9	μA
	3 (OFF)	I_{DDOFF}	—	—	$V_{DD1} = 1.5\text{ V}$	—	—	2.0	μA
Power Off Timer Times		T	—	—	$V_{DD1} = 1.5\text{ V}$	429	600	1001	s

WAVEFORMS FOR DISPLAY



(Note 1) : at $f\phi = 9\text{ kHz}$

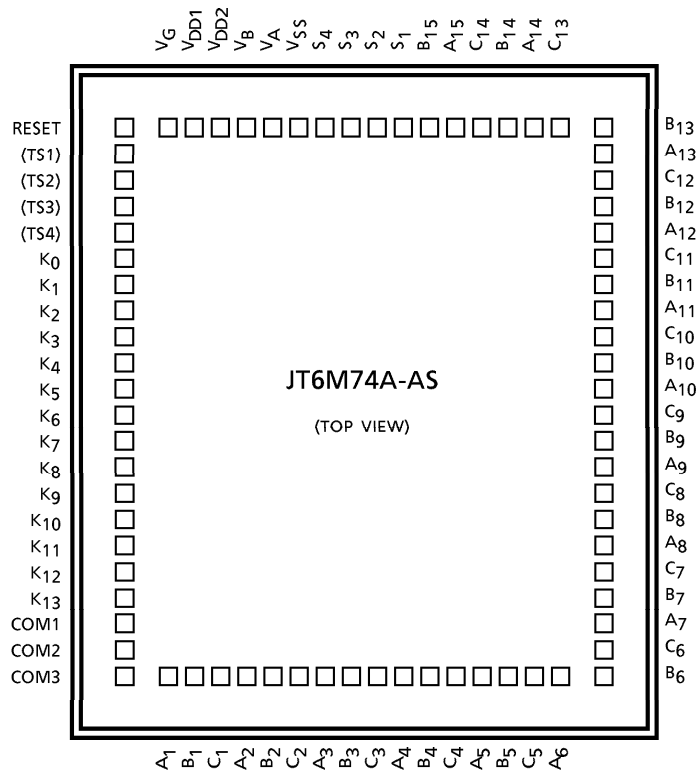
PAD LOCATION TABLE

(μm)

NAME	X POINT	Y POINT	NAME	X POINT	Y POINT
COM3	- 1757	- 1680	B ₁₃	1757	1680
COM2	- 1757	- 1520	A ₁₃	1757	1520
COM1	- 1757	- 1360	C ₁₂	1757	1360
K ₁₃	- 1757	- 1200	B ₁₂	1757	1200
K ₁₂	- 1757	- 1040	A ₁₂	1757	1040
K ₁₁	- 1757	- 880	C ₁₁	1757	880
K ₁₀	- 1757	- 720	B ₁₁	1757	720
K ₉	- 1757	- 560	A ₁₁	1757	560
K ₈	- 1757	- 400	C ₁₀	1757	400
K ₇	- 1757	- 240	B ₁₀	1757	240
K ₆	- 1757	- 80	A ₁₀	1757	80
K ₅	- 1757	80	C ₉	1757	- 80
K ₄	- 1757	240	B ₉	1757	- 240
K ₃	- 1757	400	A ₉	1757	- 400
K ₂	- 1757	560	C ₈	1757	- 560
K ₁	- 1757	720	B ₈	1757	- 720
K ₀	- 1757	880	A ₈	1757	- 880
(TS4)	- 1757	1040	C ₇	1757	- 1040
(TS3)	- 1757	1200	B ₇	1757	- 1200
(TS2)	- 1757	1360	A ₇	1757	- 1360
(TS1)	- 1757	1520	C ₆	1757	- 1520
RESET	- 1757	1680	B ₆	1757	- 1680
V _G	- 1388	1753	A ₆	1278	- 1752
V _{DD1}	- 1151	1753	C ₅	1118	- 1752
V _{DD2}	- 991	1753	B ₅	958	- 1752
V _B	- 831	1753	A ₅	798	- 1752
V _A	- 671	1753	C ₄	638	- 1752
V _{SS}	- 511	1753	B ₄	478	- 1752
S ₄	- 351	1753	A ₄	318	- 1752
S ₃	- 191	1753	C ₃	158	- 1752
S ₂	- 31	1753	B ₃	- 2	- 1752
S ₁	129	1753	A ₃	- 162	- 1752
B ₁₅	289	1753	C ₂	- 322	- 1752
A ₁₅	449	1753	B ₂	- 482	- 1752
C ₁₄	609	1753	C ₂	- 642	- 1752
B ₁₄	769	1753	C ₁	- 802	- 1752
A ₁₄	929	1753	B ₁	- 962	- 1752
C ₁₃	1089	1753	A ₁	- 1122	- 1752

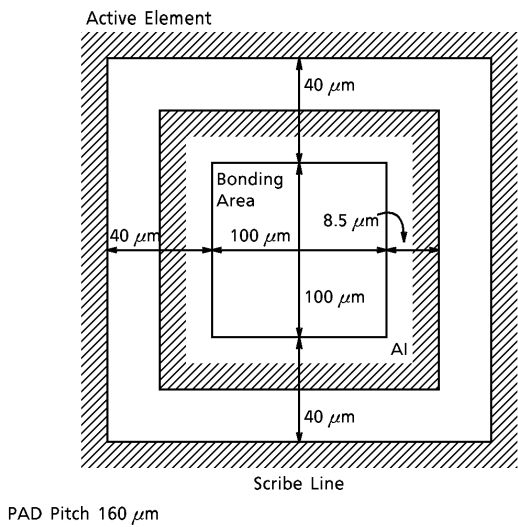
(Note) : () Do not connect.

CHIP LAYOUT



Chip size : 3.79 × 3.84 (mm)
Chip thickness : 440 ± 30 (μm)
Substrate : V_{SS}

PAD LAYOUT



QFP80-P-1420-0.80A

Technical drawing of a 100-pin Quad Flat Pack (QFP) package. The drawing includes a top view, a side view, and a detail view of the lead profile.

Top View Dimensions:

- Overall width: 24.8 ± 0.3 mm
- Overall height: 18.8 ± 0.3 mm
- Pin pitch: 0.8 mm
- Pin 1 location: Indicated by a circle and the number 1.
- Pin counts: 64 pins on the top edge, 41 pins on the right edge, 25 pins on the bottom edge, and 80 pins on the left edge.
- Internal dimensions: 20.0 ± 0.2 mm (width of the central area), 14.0 ± 0.2 mm (height of the central area), and 0.35 ± 0.1 mm (distance from the bottom edge to the center of the package).
- Other dimensions: 0.8 TYP (distance from the left edge to the center of the package), 0.16 (M) (distance from the bottom edge to the center of the package), and 0.8 mm (width of the lead).

Side View Dimensions:

- Maximum height: 3.05 MAX mm
- Body height: 2.7 ± 0.2 mm
- Lead height: 0.2 ± 0.1 mm

Detail View Dimensions:

- Lead thickness: $0.15^{+0.1}_{-0.05}$ mm
- Lead width: 1.2 ± 0.2 mm

2000-03-22 17/17