PCI CONTROLLER PLL CLOCK DRIVER

IDTCSP5940

FEATURES:

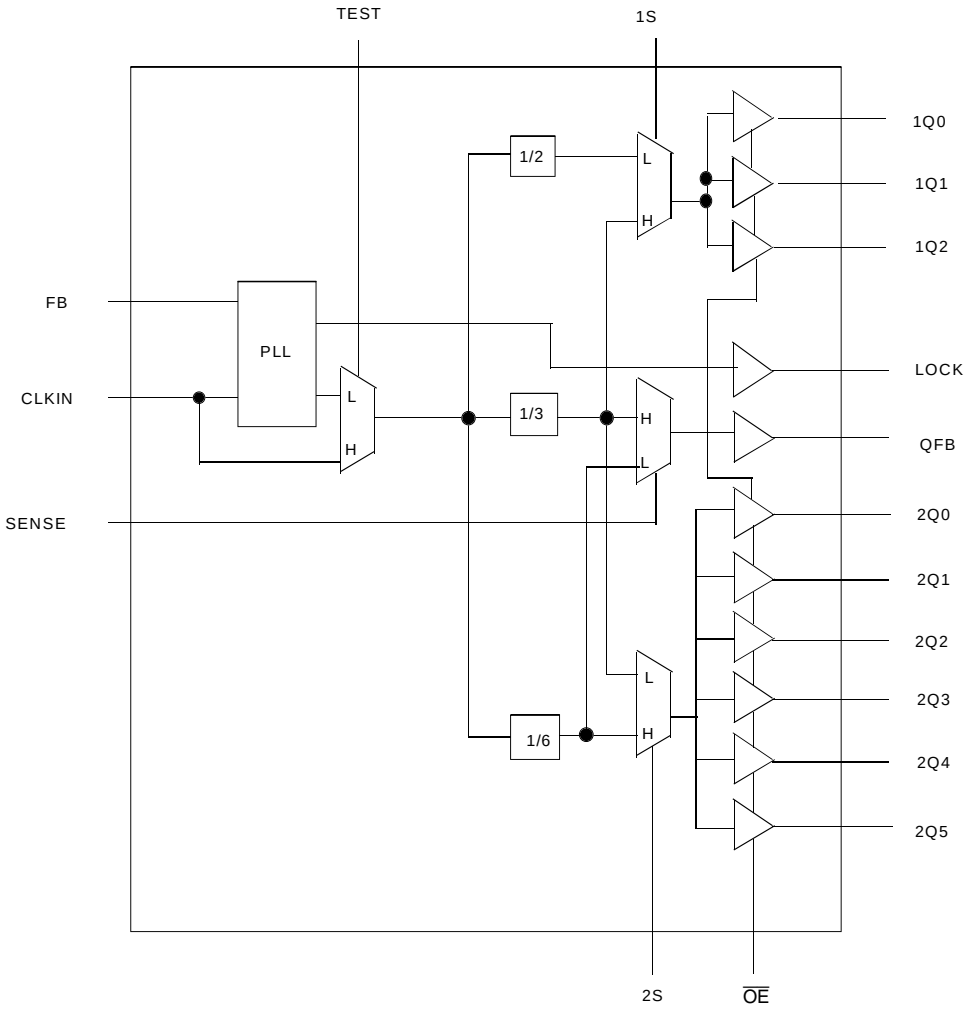
- 10 Clock Outputs configured in 3 groups
- Internal loop filter
- 5V tolerant inputs
- Output enable ($\overline{OE}$)
- PLL lock indicator output
- Extended -40 to 85°C operation
- Low skew guaranteed between outputs
- Sense control input
- Low output jitter
- 3V to 3.6V supply voltage
- Available in 28-pin QSOP package

DESCRIPTION:

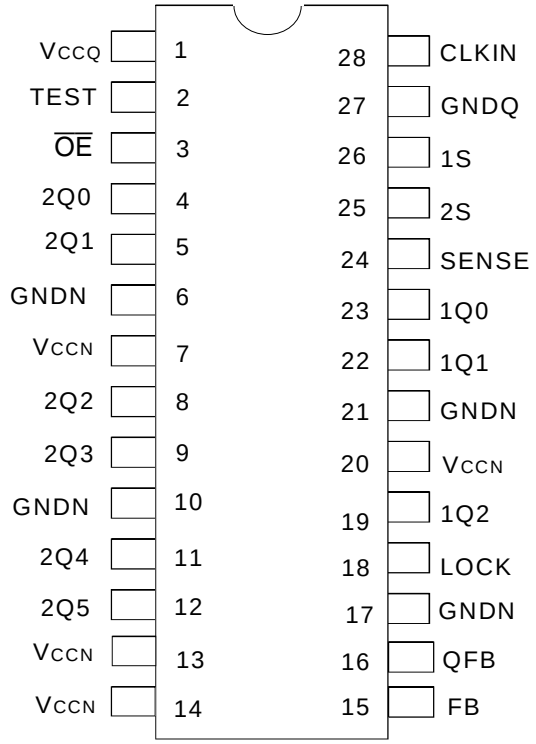
The CSP5940 is a high-performance, low skew, low jitter phase locked loop (PLL) clock driver. Two banks of outputs can be programmed to generate multiple copies of different clock frequencies from a single system clock input. The CSP5940 has been specially designed to interface PCI controllers by providing simultaneous 33MHz, 66MHz, and 99MHz clock outputs.

The CSP5940 has an internal RC filter which provides excellent jitter characteristics and eliminates the need for external components. The LOCK output asserts to indicate when phase lock has been achieved.

Functional Block Diagram



PIN CONFIGURATION



QSOP
TOP VIEW

ABSOLUTE MAXIMUM RATING (1)

Symbol	Description	Max.	Unit
	Supply Voltage to Ground	– 0.5 to + 7	V
	DC Input Voltage V_{IN}	– 0.5 to + 7	V
	DC Input Diode Current with $V_I < 0$	– 20	mA
	Maximum Power Dissipation at T_A = 70°	.80	W
	T_A = 85°	.66	
	T_{STG} Storage Temperature	–65 to 150	°C

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NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Min.	Typ.	Max.	Units
C_{IN}	Input Capacitance	—	4	6	pF
C_{OUT}	Output Capacitance	—	3	6	pF

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NOTE:
1. Limits guaranteed by characterization only.

FREQUENCY SELECTION

Sense	1S	2S	1Qx Output	2Qx Output
L	L	X	3 x CLKIN	
	H	X	2 x CLKIN	
	X	L		2 x CLKIN
	X	H		1 x CLKIN
H	L	X	1.5 x CLKIN	
	H	X	1 x CLKIN	
	X	L		1 x CLKIN
	X	H		0.5 x CLKIN

PIN DESCRIPTION

Pin Name	Description
CLKIN(1)	System Clock Input
FB	Feedback Input
QFB	Clock Output for PLL Feedback
SENSE(1)	Sense Input from System Control Bus. When LOW, system clock is from 24MHz to 33MHz. When HIGH, system clock is from 48MHz to 66MHz.
1S(1)	Select Input of Bank 1. When LOW, divide VCO frequency by 2. When HIGH, divide VCO frequency by 3.
1Q0:2	Clock Outputs of Bank 1
OE	Output Enable. Set LOW in normal operation. When HIGH, clock outputs are 3-stated.
2S(1)	Select Input of Bank 2. When LOW, divide VCO frequency by 3. When HIGH, divide VCO frequency by 6.
2Q0:5	Clock Outputs of Bank 2
LOCK	PLL lock indication signal. HIGH indicates positive lock. LOW indicates that the PLL is not locked and outputs may not be synchronized to the inputs.
TEST	Enables and Disables the PLL. Useful for testing purposes. Set LOW in normal operation.
V_{CCQ}	Power Supply (quiet) for PLL
V_{CCN}	Power Supply for Output Buffers
GNDQ	Ground Supply (quiet) for PLL
GNDN	Ground for Output Buffers

NOTE:

1. SENSE control input should ensure VCO operates at its optimal frequency range from 144MHz to 200MHz. When SENSE is LOW, VCO is running at 6xCLKIN. When SENSE is HIGH, VCO is running at 3xCLKIN. Operation with CLKIN input outside specified frequency ranges may result in invalid or out-of-lock outputs.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: T_A = – 40°C to +85°C

Symbol	Parameter	Test Conditions	Min.	Typ.(1)	Max.	Unit
V_{IH}	Input HIGH Voltage Level	Guaranteed Logic HIGH for Inputs	2	—	—	V
V_{IL}	Input LOW Voltage Level	Guaranteed Logic LOW for Inputs	—	—	0.8	V
V_{IC}	Clamp Diode Voltage Level	V_{CC} = 3V, I_{IN} = –18mA	—	– 0.7	– 1.2	V
V_{OH}	Output HIGH Voltage Level	V_{CC} = 3V, I_{OH} = –12mA	2.4	—	—	V
		V_{CC} = 3V, I_{OH} = –100µA	2.8	—	—	
V_{OL}	Output LOW Voltage Level	V_{CC} = 3V, I_{OL} = 12mA	—	—	.55	V
		V_{CC} = 3V, I_{OL} = 100µA	—	—	0.2	
I_{IN}	Input Leakage Current	V_{CC} = 3V, V_{IN} = 0V or 5.5V	—	—	1	µA

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NOTE:

1. Typical values are at V_{CC} = 3.3V, +25°C ambient.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = 3.6, OE = Test = V_{CC}, Sense 1S = Sense 2S = GND	—	0.6	5	mA
I_{CCD}	Dynamic Power Supply Current	All Outputs Unloaded	—	77	130	mA

OPERATING CHARACTERISTICS , T_A = 25°C

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Power Supply Voltage	3	3.6	V
V_{IN}	Input Voltage	0	3.6	V
V_{OUT}	Voltage Applied to 3-State Outputs	0	V_{CC}	V
T_A	Ambient Operating Temperature	-40	85	°C

SWITCHING CHARACTERISTICS (1)

Symbol	Parameter	Test Conditions(1)	Min.	Typ.	Max.	Unit
FCLKIN	Clock Input Frequency	Sense = L	24		33	MHz
		Sense = H	48		66	
TPD	CLKIN input to FB delay(1)	Measured at Vcc/2 with AC test load on QFB			200	ps
TSKQ	1Q output to QFB output skew same transition, same bank(3)	Measured at Vcc/2			150	ps
TSK1	Output to output skew same transition, same bank	Measured at Vcc/2			200	ps
TSK2	Output to output skew same transition, all outputs	Measured at Vcc/2			200	ps
TI/OJ	Input to output jitter Input ref to 1Q output 1000 samples	Measured TR of ref to TR of 1Q SPEC in RMS and peak to peak				
TI/OJcc	Input to output jitter Input ref to 1Q output 1000 samples	Measured TR of ref to TR of 1Q SPEC in RMS and cycle to cycle				
TJ	Cycle to cycle jitter (1) Peak to peak	fCLKIN = 66MHz, 1Qn = 66MHz, 2Qn = 66MHz			±100	ps
		fCLKIN = 66MHz, 1Qn = 66MHz, 2Qn = 33MHz			±100	
		fCLKIN = 33MHz, 1Qn = 99MHz, 2Qn = 66MHz			±100	
TPW	Ouput duty cycle distortion(1, 2)	Measured at Vcc/2	45%		55%	
TLOCK	CLKIN to phase lock			0.1	0.5	ms
TR	Rise Time(1)	0.8V to 2V		0.7	1.5	ns
TF	Fall Times(1)	2V to 0.8V		0.7	1.5	ns

NOTES:

1. Limits guaranteed by characterization but not tested.
2. Output signal is nominally 50% duty cycle: maximum error is ±5% of the period.
3. TSKQ is measured from TR of 1Q to TR of QFB.

TIMING DIAGRAM

Figure 1. AC Test Load and Waveforms

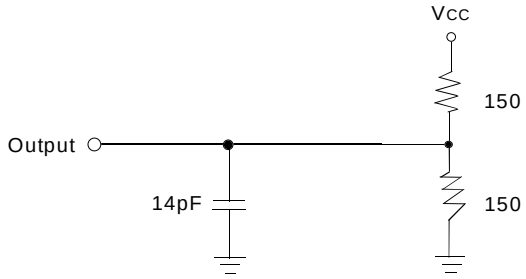


Figure 2. Input Test Waveform

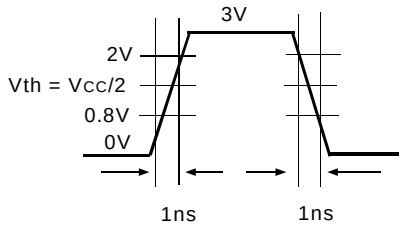


Figure 3. AC Timing Diagram

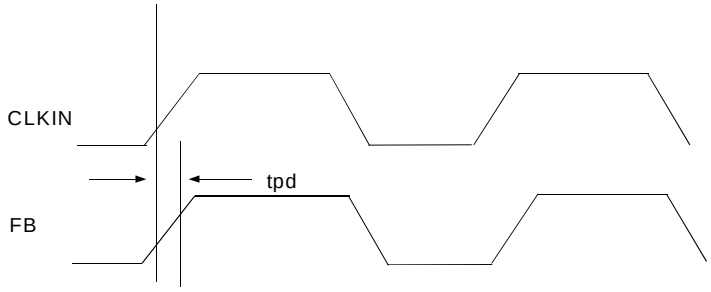


Figure 4. Output Waveform

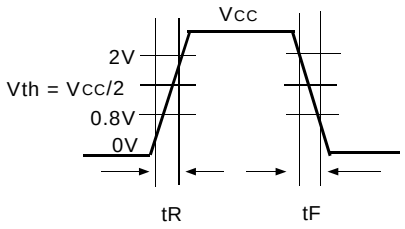
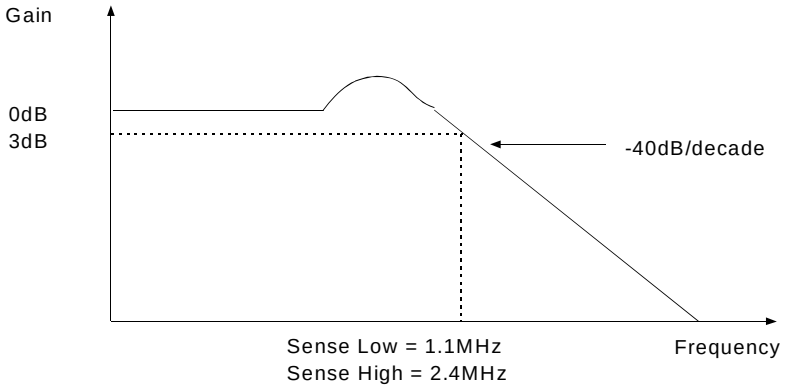


Figure 5. F_3dB Closed Loop Frequency

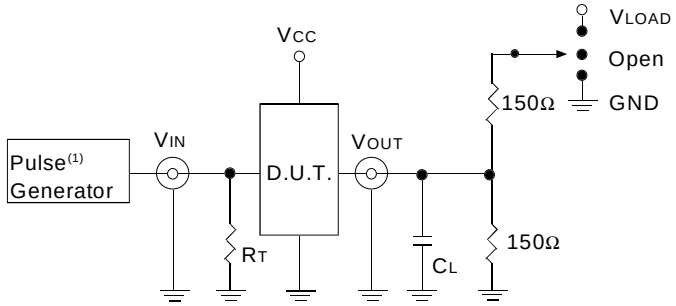


TEST CIRCUITS AND WAVEFORMS:

TEST CONDITIONS

Symbol	$V_{CC}^{(1)}$= 3.3V±0.3V	Unit
V_{LOAD}	6	V
V_{IH}	2.7	V
V_T	1.5	V
V_{LZ}	300	mV
V_{HZ}	300	mV
C_L	14	pF

TEST CIRCUITS FOR ALL OUTPUTS



DEFINITIONS:

C_L= Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V_{LOAD}
Disable High Enable High	GND
All Other tests	Open

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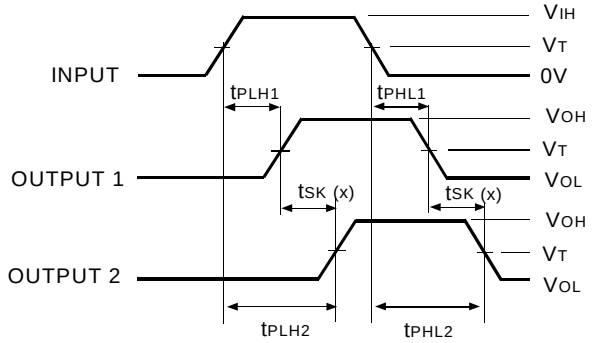
OUTPUT SKEW - t_{SK} (x)

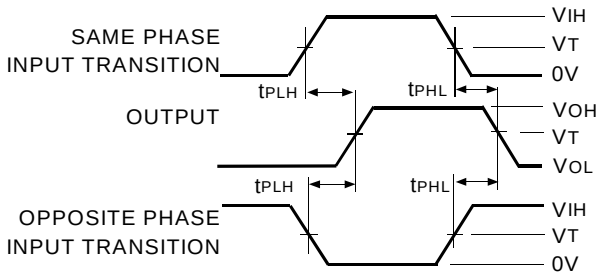


$t_{SK(x)} = |t_{PLH2} - t_{PLH1}|$ or $|t_{PHL2} - t_{PHL1}|$

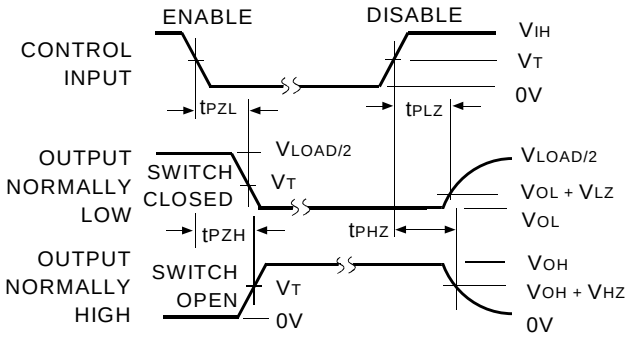
NOTES:

1. For t_{SK2} OUTPUT1 and OUTPUT2 are any two outputs.
2. For t_{SK1} OUTPUT1 and OUTPUT2 are in the same bank.

PROPAGATION DELAY



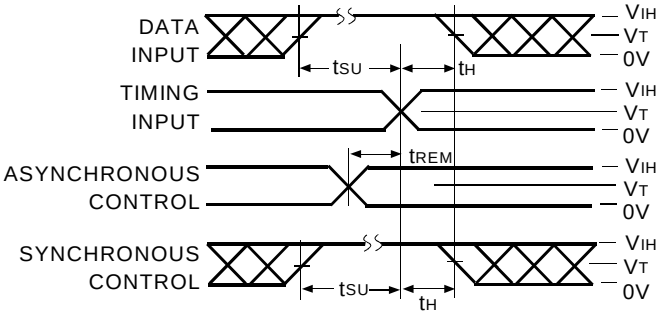
ENABLE AND DISABLE TIMES



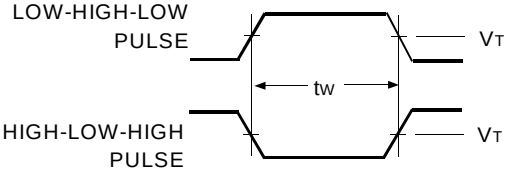
NOTE:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

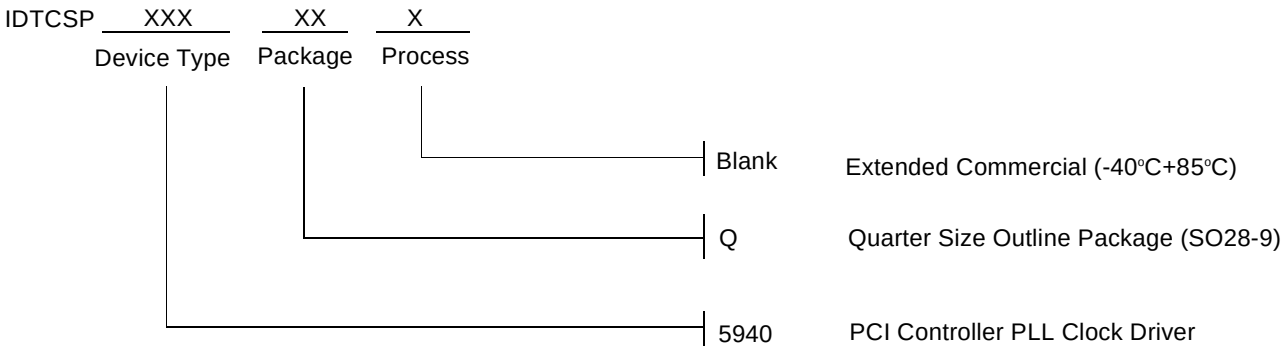
SET-UP, HOLD, AND RELEASE TIMES



PULSE WIDTH



ORDERING INFORMATION



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