



# 3.3V CMOS OCTAL BUFFER/DRIVER WITH 3- STATE OUTPUTS, 5 VOLT TOLERANT I/O, BUS-HOLD

**IDT74LVCH2244A**  
**ADVANCE**  
**INFORMATION**

## FEATURES:

- 0.5 MICRON CMOS Technology
- ESD > 2000V per MIL-STD-883, Method 3015;  
> 200V using machine model (C = 200pF, R = 0)
- 1.27mm pitch SOIC, 0.65mm pitch SSOP,  
0.635mm pitch QSOP, 0.65mm pitch TSSOP packages
- Extended commercial range of - 40°C to +85°C
- V<sub>CC</sub> = 3.3V ±0.3V, Normal Range
- V<sub>CC</sub> = 2.3V to 3.6V, Extended Range
- CMOS power levels (0.4μW typ. static)
- Rail-to-Rail output swing for increased noise margin
- All inputs, outputs and I/O are 5 Volt tolerant
- Supports hot insertion

## Drive Features for LVCH2244A:

- Balanced Output Drivers: ±12mA
- Low switching noise

## APPLICATIONS:

- 5V and 3.3V mixed voltage systems
- Data communication and telecommunication systems

## DESCRIPTION:

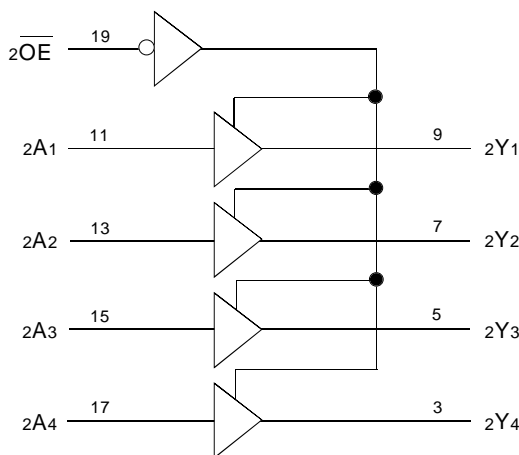
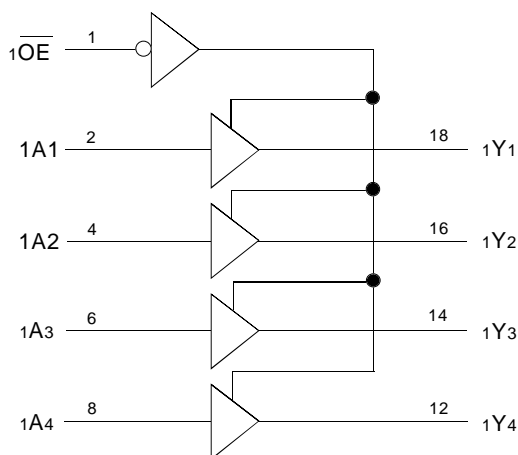
This octal buffer/driver is built using advanced dual metal CMOS technology. The LVCH2244A device is organized as two 4-bit line drivers with separate output-enable ( $\overline{OE}$ ) inputs. When  $\overline{OE}$  is low, the device passes data from the A inputs to the Y outputs. When  $\overline{OE}$  is high, the outputs are in the high-impedance state.

The LVCH2244A has series resistors in the device output structure which will significantly reduce line noise when used with light loads. This driver has been designed to drive ±12mA at the designated threshold levels.

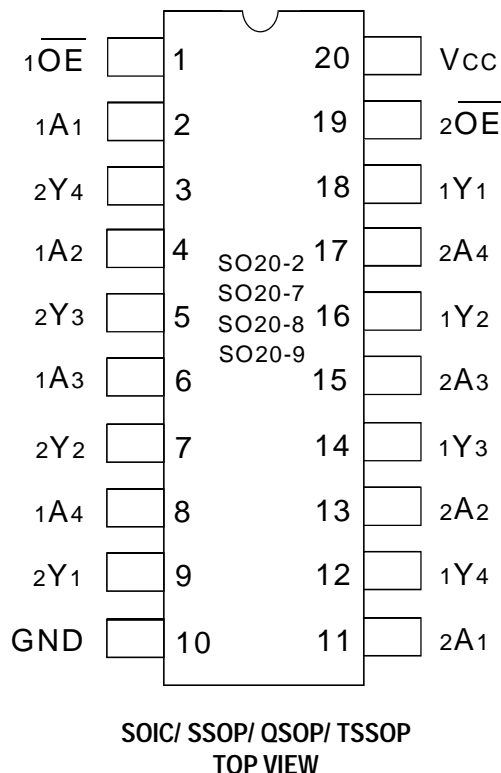
Inputs can be driven from either 3.3V or 5V devices. This feature allows the use of this device as a translator in a mixed 3.3V/5V system environment.

The LVCH2244A has "bus-hold" which retains the inputs' last state whenever the input goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistors.

## FUNCTIONAL BLOCK DIAGRAM



## PIN CONFIGURATION



## ABSOLUTE MAXIMUM RATINGS <sup>(1)</sup>

Symbol	Description	Max.	Unit
V <sub>TERM</sub>	Terminal Voltage with Respect to GND	– 0.5 to +6.5	V
T <sub>STG</sub>	Storage Temperature	– 65 to +150	°C
I <sub>OUT</sub>	DC Output Current	– 50 to +50	mA
I <sub>IK</sub> I <sub>OK</sub>	Continuous Clamp Current, V <sub>I</sub> < 0 or V <sub>O</sub> < 0	– 50	mA
I <sub>CC</sub> I <sub>SS</sub>	Continuous Current through each V <sub>CC</sub> or GND	±100	mA

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### NOTE:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## CAPACITANCE (T<sub>A</sub> = +25°C, f = 1.0MHz)

Symbol	Parameter <sup>(1)</sup>	Conditions	Typ.	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	4.5	6	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0V	5.5	8	pF
C <sub>I/O</sub>	I/O Port Capacitance	V <sub>IN</sub> = 0V	6.5	8	pF

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### NOTE:

- As applicable to the device type.

## PIN DESCRIPTION

Pin Names	Description
x $\overline{\text{OE}}$	Output-enable Inputs (Active LOW)
xAx	Data Inputs <sup>(1)</sup>
xYx	3-State Outputs

### NOTE:

- These pins have "Bus-hold". All other pins are standard inputs, outputs, or I/Os.

## FUNCTION TABLE (each buffer) <sup>(1)</sup>

Inputs		Outputs
x $\overline{\text{OE}}$	xAx	xYx
L	H	H
L	L	L
H	X	Z

### NOTE:

- H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Don't Care  
Z = High-Impedance

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition:  $T_A = -40^{\circ}\text{C}$  To  $+85^{\circ}\text{C}$

Symbol	Parameter	Test Conditions		Min.	Typ. <sup>(1)</sup>	Max.	Unit
$V_{IH}$	Input HIGH Voltage Level	$V_{CC} = 2.3\text{V to } 2.7\text{V}$		1.7	—	—	V
		$V_{CC} = 2.7\text{V to } 3.6\text{V}$		2	—	—	
$V_{IL}$	Input LOW Voltage Level	$V_{CC} = 2.3\text{V to } 2.7\text{V}$		—	—	0.7	V
		$V_{CC} = 2.7\text{V to } 3.6\text{V}$		—	—	0.8	
$I_{IH}$ $I_{IL}$	Input Leakage Current	$V_{CC} = 3.6\text{V}$	$V_I = 0 \text{ to } 5.5\text{V}$	—	—	$\pm 5$	$\mu\text{A}$
$I_{OZH}$ $I_{OZL}$	High Impedance Output Current (3-State Output pins)	$V_{CC} = 3.6\text{V}$	$V_O = 0 \text{ to } 5.5\text{V}$	—	—	$\pm 10$	$\mu\text{A}$
$I_{OFF}$	Input/Output Power Off Leakage	$V_{CC} = 0\text{V}, V_{IN} \text{ or } V_O \leq 5.5\text{V}$		—	—	$\pm 50$	$\mu\text{A}$
$V_{IK}$	Clamp Diode Voltage	$V_{CC} = 2.3\text{V}, I_{IN} = -18\text{mA}$		—	-0.7	-1.2	V
$V_H$	Input Hysteresis	$V_{CC} = 3.3\text{V}$		—	100	—	mV
$I_{CCL}$ $I_{CCH}$ $I_{CCZ}$	Quiescent Power Supply Current	$V_{CC} = 3.6\text{V}$	$V_{IN} = \text{GND or } V_{CC}$	—	—	10	$\mu\text{A}$
			$3.6 \leq V_{IN} \leq 5.5\text{V}^{(2)}$	—	—	10	
$\Delta I_{CC}$	Quiescent Power Supply Current Variation	One input at $V_{CC} - 0.6\text{V}$ , other inputs at $V_{CC}$ or GND		—	—	500	$\mu\text{A}$

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### NOTES:

1. Typical values are at  $V_{CC} = 3.3\text{V}$ ,  $+25^{\circ}\text{C}$  ambient.
2. This applies in the disabled state only.

## BUS-HOLD CHARACTERISTICS

Symbol	Parameter <sup>(1)</sup>	Test Conditions		Min.	Typ. <sup>(2)</sup>	Max.	Unit
$I_{BHH}$ $I_{BHL}$	Bus-Hold Input Sustain Current	$V_{CC} = 3.0\text{V}$	$V_I = 2.0\text{V}$	-75	—	—	$\mu\text{A}$
			$V_I = 0.8\text{V}$	75	—	—	
$I_{BHH}$ $I_{BHL}$	Bus-Hold Input Sustain Current	$V_{CC} = 2.3\text{V}$	$V_I = 1.7\text{V}$	—	—	—	$\mu\text{A}$
			$V_I = 0.7\text{V}$	—	—	—	
$I_{BHHO}$ $I_{BHLO}$	Bus-Hold Input Overdrive Current	$V_{CC} = 3.6\text{V}$	$V_I = 0 \text{ to } 3.6\text{V}$	—	—	$\pm 500$	$\mu\text{A}$

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### NOTES:

1. Pins with Bus-hold are identified in the pin description.
2. Typical values are at  $V_{CC} = 3.3\text{V}$ ,  $+25^{\circ}\text{C}$  ambient.

## OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Max.	Unit
VOH	Output HIGH Voltage	VCC = 2.3V to 3.6V	IOH = – 0.1mA	VCC – 0.2	—	V
		VCC = 2.3V	IOH = – 4mA	1.9	—	
			IOH = – 6mA	1.7	—	
		VCC = 2.7V	IOH = – 4mA	2.2	—	
			IOH = – 8mA	2	—	
		VCC = 3.0V	IOH = – 6mA	2.4	—	
			IOH = – 12mA	2	—	
VOL	Output LOW Voltage	VCC = 2.3V to 3.6V	IOL = 0.1mA	—	0.2	V
		VCC = 2.3V	IOL = 4mA	—	0.4	
			IOL = 6mA	—	0.55	
		VCC = 2.7V	IOL = 4mA	—	0.4	
			IOL = 8mA	—	0.6	
		VCC = 3.0V	IOL = 6mA	—	0.55	
			IOL = 12mA	—	0.8	

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### NOTE:

1. VIH and VIL must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate VCC range. TA = – 40°C to +85°C.

## OPERATING CHARACTERISTICS, TA = 25°C

Symbol	Parameter	Test Conditions	VCC = 2.5V±0.2V	VCC = 3.3V±0.3V	Unit
			Typical	Typical	
CPD	Power Dissipation Capacitance per buffer/driver Outputs enabled	CL = 0pF, f = 10Mhz	—	46	pF
CPD	Power Dissipation Capacitance per buffer/driver Outputs disabled		—	2	pF

## SWITCHING CHARACTERISTICS <sup>(1)</sup>

Symbol	Parameter	VCC = 2.5V±0.2V		VCC = 2.7V		VCC = 3.3V±0.3V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
tPLH tPHL	Propagation Delay xAX to xYx	—	—	—	6.4	1.5	5.5	ns
tPZH tPZL	Output Enable Time xOE to xYx	—	—	—	8.1	1	7.1	ns
tPHZ tPLZ	Output Disable Time xOE to xYx	—	—	—	7.3	1.5	6.8	ns
tsk(o)	Output Skew <sup>(2)</sup>	—	—	—	—	—	500	ps

### NOTES:

1. See test circuits and waveforms. TA = – 40°C to + 85°C.
2. Skew between any two outputs of the same package and switching in the same direction.

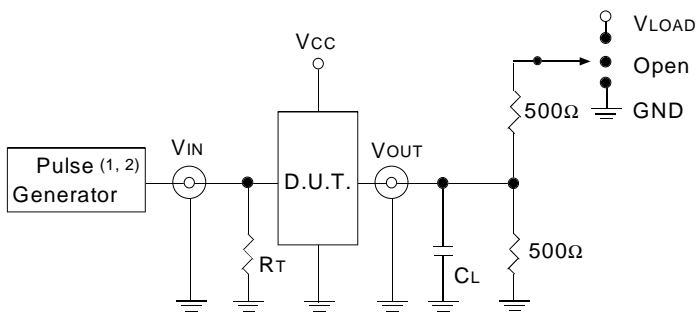
## TEST CIRCUITS AND WAVEFORMS

### TEST CONDITIONS

Symbol	V <sub>CC</sub> (1) = 3.3V ± 0.3V	V <sub>CC</sub> (1) = 2.7V	V <sub>CC</sub> (2) = 2.5V ± 0.2V	Unit
V <sub>LOAD</sub>	6	6	2 x V <sub>CC</sub>	V
V <sub>IH</sub>	2.7	2.7	V <sub>CC</sub>	V
V <sub>T</sub>	1.5	1.5	V <sub>CC</sub> / 2	V
V <sub>LZ</sub>	300	300	150	mV
V <sub>HZ</sub>	300	300	150	mV
C <sub>L</sub>	50	50	30	pF

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### TEST CIRCUITS FOR ALL OUTPUTS



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#### DEFINITIONS:

C<sub>L</sub> = Load capacitance: includes jig and probe capacitance.

R<sub>T</sub> = Termination resistance: should be equal to Z<sub>OUT</sub> of the Pulse Generator.

#### NOTES:

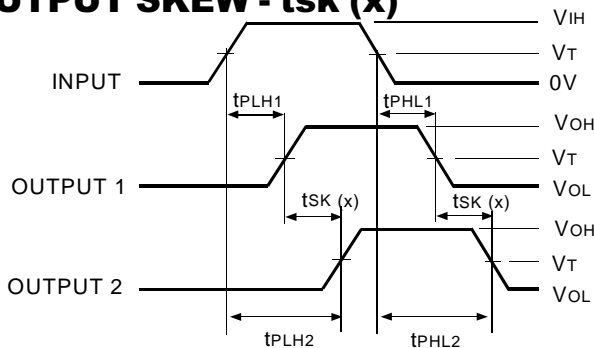
1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t<sub>F</sub> ≤ 2.5ns; t<sub>R</sub> ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t<sub>F</sub> ≤ 2ns; t<sub>R</sub> ≤ 2ns.

### SWITCH POSITION

Test	Switch
Open Drain	V <sub>LOAD</sub>
Disable Low	
Enable Low	
Disable High	GND
Enable High	
All Other tests	Open

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### OUTPUT SKEW - t<sub>SK</sub>(x)



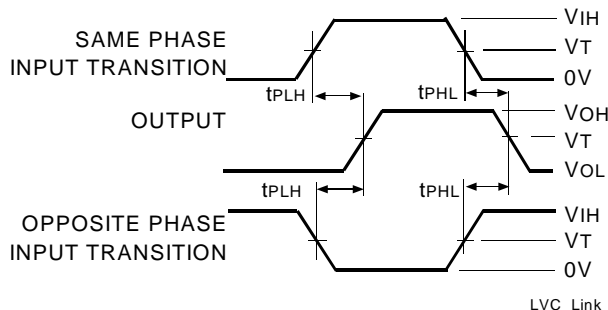
$$t_{SK}(x) = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

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#### NOTES:

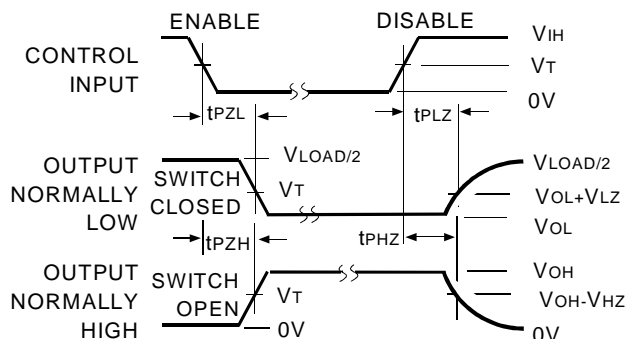
1. For t<sub>SK</sub>(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For t<sub>SK</sub>(b) OUTPUT1 and OUTPUT2 are in the same bank.

### PROPAGATION DELAY



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### ENABLE AND DISABLE TIMES

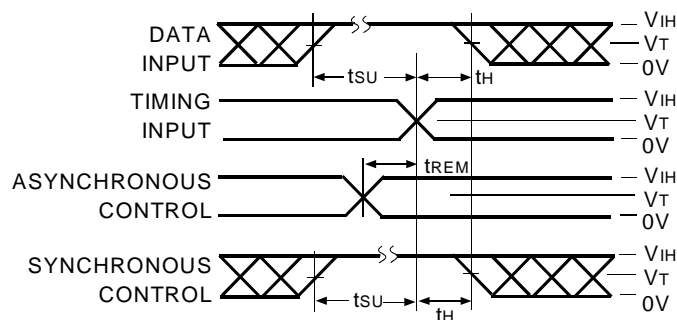


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#### NOTE:

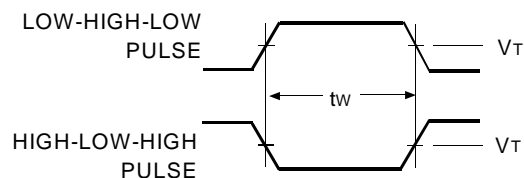
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

### SET-UP, HOLD, AND RELEASE TIMES



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### PULSE WIDTH



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## ORDERING INFORMATION

IDT	XX	LVC	X	XXXX	XX	
Temp. Range			Bus-Hold	Device Type	Package	
					SO	Small Outline IC (gull wing) (SO20-2)
					PY	Shrink Small Outline Package (SO20-7)
					Q	Quarter Size Small Outline Package (SO20-8)
					PG	Thin Shrink Small Outline Package (SO20-9)
				2244A		Octal Buffer/Driver with 3-State Outputs, $\pm 12\text{mA}$
			H			Bus-hold
				74		$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$



### CORPORATE HEADQUARTERS

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