Features

- 256K x 36 or 512K x 18 organization
- CMOS technology
- Synchronous late-select mode of operation with self-timed late write
- Single differential high-speed transceiver logic (HSTL) clock
- 3.3V power supply, 1.5V V_{DDQ}
- HSTL input and output levels
- Registered addresses, write enables, synchronous select and data-ins.
- Common I/O
- Asynchronous output enable and sleep mode inputs
- Boundary scan using a limited set of JTAG 1149.1 functions
- Byte write capability and global write enable
- 7 x 17 bump ball grid array package with SRAM JEDEC standard pinout and boundary scan order
- Programmable impedance output drivers

Description

The 3.3V IBM04188ETLAC and IBM04368ETLAC SRAMs are synchronous pipeline-mode, late select, high-performance CMOS static random-access memories that have wide I/O and achieve 3ns cycle times. Single differential K clocks are used to initiate the read/write operation, and all internal operations are self-timed. At the rising edge of the K clock, all addresses, write-enables, synchronous select, and data-ins are registered internally. Data-outs are updated from output registers on the next rising edge of the K clock. An internal write buffer allows write data to follow one cycle after addresses and controls. Address SAS is a late-select address. It performs a one-of-two decode on the data addressed by addresses SA1–SA18 in the previous cycle. The SRAM is operated with a single 3.3V power supply and is compatible with 1.5V HSTL I/O interfaces.

x36 BGA Bump Layout (Top View)

	1	2	3	4	5	6	7
A	V_{DDQ}	SA14	SA11	NC	SA10	SA7	V_{DDQ}
B	NC	NC	SA13	NC	SA9	SA6	NC
C	NC	SA15	SA12	V_{DD}	SA8	SA5	NC
D	DQ21	DQ20	V_{SS}	ZQ	V_{SS}	DQ15	DQ14
E	DQ24	DQ22	V_{SS}	$\overline{SS}$	V_{SS}	DQ13	DQ11
F	V_{DDQ}	DQ23	V_{SS}	$\overline{G}$	V_{SS}	DQ12	V_{DDQ}
G	DQ19	DQ18	$\overline{SBWc}$	NC	$\overline{SBWb}$	DQ17	DQ16
H	DQ25	DQ26	V_{SS}	NC	V_{SS}	DQ9	DQ10
J	V_{DDQ}	V_{DD}	V_{REF}	V_{DD}	V_{REF}	V_{DD}	V_{DDQ}
K	DQ28	DQ27	V_{SS}	K	V_{SS}	DQ8	DQ7
L	DQ34	DQ35	$\overline{SBWd}$	$\overline{K}$	$\overline{SBWa}$	DQ0	DQ1
M	V_{DDQ}	DQ30	V_{SS}	$\overline{SW}$	V_{SS}	DQ5	V_{DDQ}
N	DQ29	DQ31	V_{SS}	SA1	V_{SS}	DQ4	DQ6
P	DQ32	DQ33	V_{SS}	SAS	V_{SS}	DQ2	DQ3
R	NC	SA16	M1[1]	V_{DD}	M2[1]	SA4	NC
T	NC	NC	SA17	SA2	SA3	NC	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

1. M1 and M2 are clock mode pins that must be connected to V_{SS} and V_{SS} respectively.

x18 BGA Bump Layout (Top View)

	1	2	3	4	5	6	7
A	V_{DDQ}	SA14	SA11	NC	SA10	SA7	V_{DDQ}
B	NC	NC	SA13	NC	SA9	SA6	NC
C	NC	SA15	SA12	V_{DD}	SA8	SA5	NC
D	DQ10	NC	V_{SS}	ZQ	V_{SS}	DQ7	NC
E	NC	DQ11	V_{SS}	$\overline{SS}$	V_{SS}	NC	DQ6
F	V_{DDQ}	NC	V_{SS}	$\overline{G}$	V_{SS}	DQ5	V_{DDQ}
G	NC	DQ9	$\overline{SBWc}$	NC	NC	NC	DQ8
H	DQ12	NC	V_{SS}	NC	V_{SS}	DQ4	NC
J	V_{DDQ}	V_{DD}	V_{REF}	V_{DD}	V_{REF}	V_{DD}	V_{DDQ}
K	NC	DQ13	V_{SS}	K	V_{SS}	NC	DQ3
L	DQ17	NC	NC	$\overline{K}$	$\overline{SBWa}$	DQ0	NC
M	V_{DDQ}	DQ14	V_{SS}	$\overline{SW}$	V_{SS}	NC	V_{DDQ}
N	DQ15	NC	V_{SS}	SA1	V_{SS}	DQ2	NC
P	NC	DQ16	V_{SS}	SAS	V_{SS}	NC	DQ1
R	NC	SA16	M1[1]	V_{DD}	M2[1]	SA4	NC
T	NC	SA18	SA17	NC	SA3	SA2	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

1. M1 and M2 are clock mode pins that must be connected to V_{SS} and V_{SS} respectively.

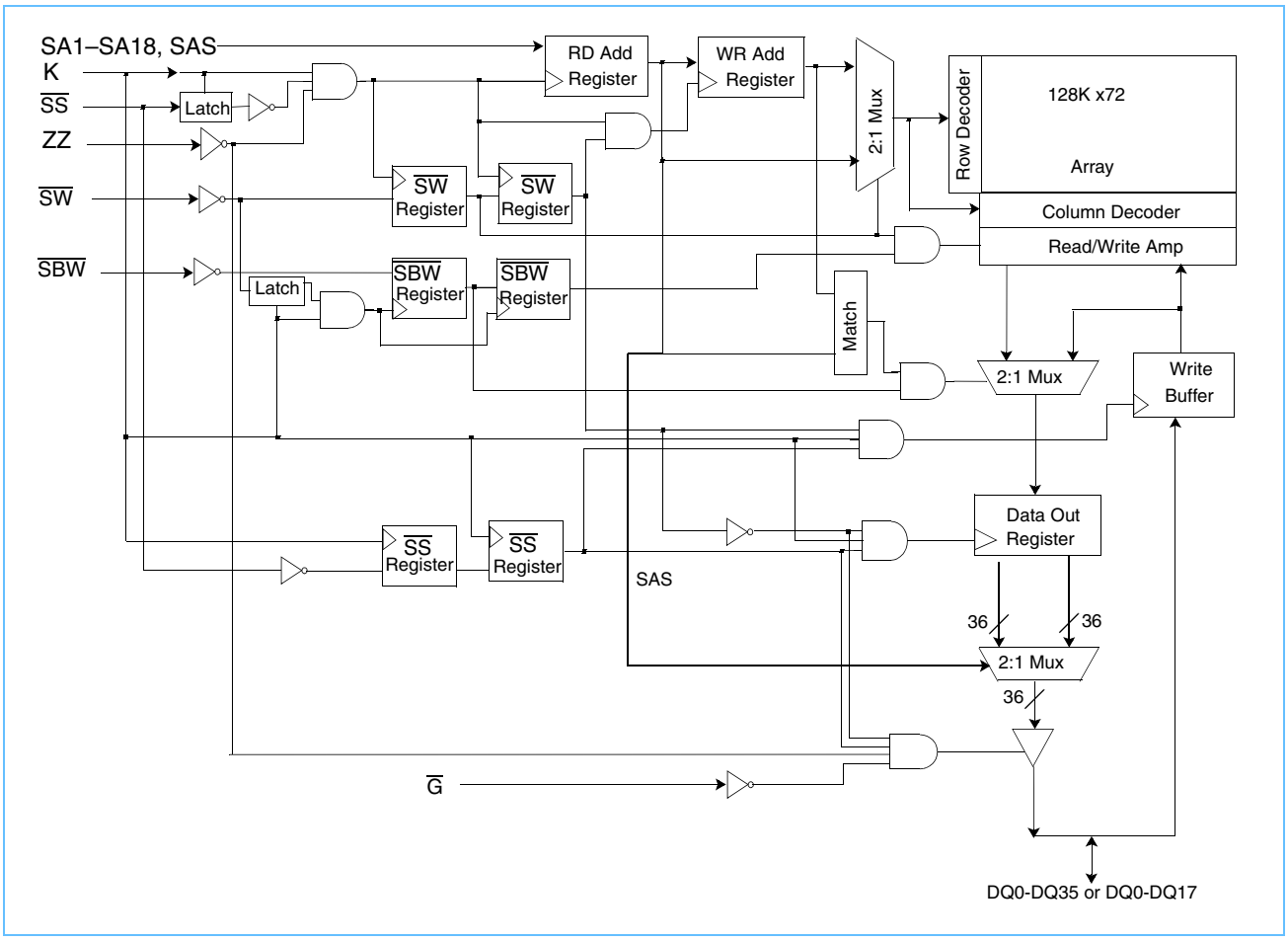
Pin Description

SA1–SA18	Address Input	$\overline{G}$	Asynchronous Output Enable
SAS	Late Select Address Input	$\overline{SS}$	Synchronous Select
DQ0–DQ35	Data I/O	M1, M2	Clock Mode Inputs- M1 must be set to V_{SS} M2 must be set to V_{DD}
K, $\overline{K}$	Differential Input Register Clocks	V_{REF}	HSTL Input Reference Voltage
$\overline{SW}$	Write Enable, Global	V_{DD}	Power Supply (+3.3V)
$\overline{SBWa}$	Write Enable, Byte a (DQ0–DQ8)	V_{SS}	Ground
$\overline{SBWb}$	Write Enable, Byte b (DQ9–DQ17)	V_{DDQ}	Output Power Supply
$\overline{SBWc}$	Write Enable, Byte c (DQ18–DQ26)	ZZ	Asynchronous Sleep Mode
$\overline{SBWd}$	Write Enable, Byte d (DQ27–DQ35)	ZQ	Output Driver Impedance Control
TMS, TDI, TCK	IEEE® 1149.1 Test Inputs (LVTTL levels)	NC	No Connect
TDO	IEEE 1149.1 Test Output (LVTTL level)		

Ordering Information

Part Number	Organization	Cycle Time (ns)	Package
IBM04188ETLAC-28	512K x 18	2.85	7 x 17 BGA
IBM04188ETLAC-30	512K x 18	3.0	7 x 17 BGA
IBM04188ETLAC-33	512K x 18	3.3	7 x 17 BGA
IBM04188ETLAC-37	512K x 18	3.7	7 x 17 BGA
IBM04368ETLAC-28	256K x 36	2.85	7 x 17 BGA
IBM04368ETLAC-30	256K x 36	3.0	7 x 17 BGA
IBM04368ETLAC-33	256K x 36	3.3	7 x 17 BGA
IBM04368ETLAC-37	256K x 36	3.7	7 x 17 BGA

Block Diagram



SRAM Features

Late Write

The late-write function allows write data to be registered one cycle after addresses and controls. This feature eliminates one of two bus-turnaround cycles normally required when going from a read to a write operation. Late write is accomplished by buffering write addresses and data. The SRAM array update occurs during the third write cycle. Read-cycle addresses are monitored to determine if read data is to be supplied from the SRAM array or the write buffer. The bypassing of the SRAM array occurs on a byte-by-byte basis. When one byte is written during a write cycle, read data from the last written address has new byte data from the write buffer and remaining bytes from the SRAM array.

Mode Control

Mode control pin M1 must be set to V_{SS} and M2 to V_{SS}.

Sleep Mode

Sleep mode is enabled by switching asynchronous signal ZZ high. When the SRAM is in sleep mode, the outputs go to a High-Z state and the SRAM draws standby current. SRAM data is preserved and a recovery time (t_{ZZR}) is required before the SRAM resumes normal operation.

Programmable Impedance and Power Up Requirements

An external resistor, RQ, must be connected between the ZQ pin on the SRAM and V_{SS} to allow the SRAM to adjust its output driver impedance. The value of RQ must be five times the value of the intended line impedance driven by the SRAM. The allowable range of RQ to guarantee impedance matching with a tolerance of 15% is between 175Ω and 350Ω. Periodic readjustment of the output driver impedance is necessary because the impedance is affected by drifts in supply voltage and temperature. One evaluation occurs every 64 clock cycles, and each evaluation can move the output driver impedance level one step at a time towards the optimum level. The output driver has 64 discrete binary weighted steps. Impedance updates for zeros occur whenever the SRAM is driving ones for the same DQs; impedance updates for ones occur whenever the SRAM is driving zeros. Updates of both zeros and ones occur when the SRAM is in High-Z. The SRAM requires 4µs of power-up time after V_{DD} reaches its operating range. Furthermore, to guarantee the output driver impedance, the SRAM requires 2048 clock cycles and a Read ‘0’ and Read ‘1’ or a Read ‘1’ and a Read ‘0’ across all outputs. The RC time constant of the loaded RQ trace must be less than 3ns.

Power-Up and Power-Down Sequence

The power supplies need to be powered up in the following sequence:

V_{DD}, V_{DDQ}, V_{REF}, followed by inputs

The power-down sequence must be in the reverse order. V_{DDQ} must not exceed V_{DD}.

Late Select

Address SAS is the late select address. It is registered along with addresses SA1–SA18. The pipelined data clocked out in cycle n+1 is selected by addresses SA1–SA18 and registered in cycle n, and SAS is registered in cycle n+1.

Clock Truth Table

K	ZZ	$\overline{SS}$	$\overline{SW}$	$\overline{SBWa}$	$\overline{SBWb}$	$\overline{SBWc}$	$\overline{SBWd}$	DQ (n)	DQ (n+1)	MODE
L→H	L	L	H	X	X	X	X	X	D_{OUT} 0-35	Read Cycle All Bytes
L→H	L	L	L	L	H	H	H	X	D_{IN} 0-8	Write Cycle First Byte
L→H	L	L	L	H	L	H	H	X	D_{IN} 9-17	Write Cycle Second Byte
L→H	L	L	L	H	H	L	H	X	D_{IN} 18-26	Write Cycle Third Byte
L→H	L	L	L	H	H	H	L	X	D_{IN} 27-35	Write Cycle Fourth Byte
L→H	L	L	L	L	L	L	L	X	D_{IN} 0-35	Write Cycle All Bytes
L→H	L	L	L	H	H	H	H	X	High-Z	Abort Write Cycle
L→H	L	H	X	X	X	X	X	X	High-Z	Deselect Cycle
X	H	X	X	X	X	X	X	High-Z	High-Z	Sleep Mode

Output Enable Truth Table

Operation (n)	$\overline{G}$ (n, n + 1)	DQ (n)	DQ (n + 1)
Read	L	X	D_{OUT} 0-35
Read	H	High-Z	High-Z
Sleep (ZZ = H)	X	High-Z	High-Z
Write ($\overline{SW}$ = L)	L	X	High-Z
Deselect ($\overline{SS}$ = H)	L	X	High-Z

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
V_{DD}	Power Supply Voltage	-0.5 to 4.3	V	1
V_{DDQ}	Output Power Supply Voltage	-0.5 to 2.825	V	1
V_{IN}	Input Voltage	-0.5 to 4.3	V	1, 2
V_{DQIN}	DQ Input Voltage	-0.5 to 2.825	V	1
T_A	Operating Temperature	0 to +85	°0C	1
T_J	Junction Temperature	0 to +110	°0C	1
T_{STG}	Storage Temperature	-55 to +125	°C	1
I_{OUT}	Short Circuit Output Current	25	mA	1

1. Stresses greater than those listed under “Absolute Maximum Ratings” can cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods can affect reliability.
2. Excludes DQ inputs.

Recommended DC Operating Conditions (T_A = 0 to + 85°C)

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
V_{DD}	Supply Voltage	3.3 - 5%	3.3	3.3 + 10%	V	1
V_{DDQ}	Output Driver Supply Voltage	1.4	1.5	1.6	V	1
V_{IH}	Input High Voltage	V_{REF} + 0.1		V_{DDQ} + 0.3	V	1, 2
V_{IL}	Input Low Voltage	-0.3		V_{REF} - 0.1	V	1, 3
V_{REF}	Input Reference Voltage	0.68	0.75	0.9	V	1, 6
$V_{IN - CLK}$	Clocks Signal Voltage	-0.3		V_{DDQ} + 0.3	V	1, 4
$V_{DIF - CLK}$	Differential Clocks Signal Voltage	0.1		V_{DDQ} + 0.6	V	1, 5
$V_{CM - CLK}$	Clocks Common Mode Voltage	0.55		0.90	V	1
I_{OUT}	Output Current		5	8	mA	

1. All voltages referenced to V_{SS}. All V_{DD}, V_{DDQ}, and V_{SS} pins must be connected.
2. V_{IH}(Max)DC = V_{DDQ} + 0.3V, V_{IH}(Max)AC = V_{DDQ} + 0.85V (pulse width ≤ 4.0ns).
3. V_{IL}(Min)DC = - 0.3 V, V_{IL}(Min)AC = -1.5V (pulse width ≤ 4.0ns).
4. V_{IN-CLK} specifies the maximum allowable DC excursions of each differential clock (K, $\overline{K}$).
5. $V_{DIF-CLK}$ specifies the minimum clock differential voltage required for switching.
6. Peak-to-peak AC component superimposed on V_{REF} may not exceed 5% of V_{REF}.

DC Electrical Characteristics (T_A = 0 to +85°C, V_{DD} = 3.3V -5%, +10%)

Symbol	Parameter			Min.	Max.	Units	Notes
I_{DD}	Average Power Supply Operating Current I_{OUT} = 0, V_{IN} = V_{IH} or V_{IL}, ZZ & $\overline{SS}$ = V_{IL}	x36	-28		550	mA	1
			-30		475		
			-33		410		
			-37		330		
		x18	-28		450	mA	1
			-30		400		
			-33		330		
			-37		265		
I_{SBSS}	Power Supply Standby Current $\overline{SS}$ = V_{IH}, ZZ = V_{IH} All other inputs = V_{IH} or V_{IH}, I_{IH} = 0				150	mA	1
I_{SBZZ}	Power Supply Sleep Current ZZ = V_{IH} All other inputs = V_{IH} or V_{IL} I_{OUT} = 0				120	mA	1, 4
I_{LI}	Input Leakage Current Any input (except JTAG) V_{IN} = V_{SS} or V_{DDQ}			-2	+2	µA	
I_{LO}	Output Leakage Current V_{OUT} = V_{SS} or V_{DDQ}, DQ in High-Z			-5	+5	µA	
V_{OH}	Output High Level Voltage (I_{OH} = -8mA)			V_{DDQ} - .4	V_{DDQ}	V	2, 3
V_{OL}	Output Low Level Voltage (I_{OL} = +8mA)			V_{SS}	V_{SS} + .4	V	2, 3
I_{LIJTAG}	JTAG Leakage Current V_{IN} = V_{SS} or V_{DD}			-150	+10	µA	5

1. I_{OUT} = chip output current.
2. Minimum impedance output driver.
3. JEDEC standard JESD8-6 class 1 compatible.
4. When ZZ = high, specification is guaranteed at 75°C junction temperature.
5. For JTAG inputs only.

Programmable Impedance Output Driver DC Electrical Characteristics

(T_A= 0 to +85°C, V_{DD} = 3.3V ± 5%)

Symbol	Parameter	Min.	Max.	Units	Notes
V_{OH}	Output High Voltage	V_{DDQ} / 2	V_{DDQ}	V	1, 2
V_{OL}	Output Low Voltage	V_{ss}	V_{DDQ} / 2	V	2, 3

1. I_{OH} = (V_{DDQ} / 2) / (RQ / 5) ± 15% @ V_{OH} = V_{DDQ} / 2 (for: 175Ω ≤ RQ ≤ 350Ω).
2. I_{OL} = (V_{DDQ} / 2) / (RQ / 5) ± 15% @ V_{OL} = V_{DDQ} / 2 (for: 175Ω ≤ RQ ≤ 350Ω).
3. Parameter tested with RQ = 250Ω and V_{DDQ} = 1.5V.

PBGA Thermal Characteristics

Symbol	Parameter	Rating	Units
RΘJC	Thermal Resistance Junction to Case	1.6	°C/W

Capacitance (T_A=0 to +85°C, V_{DD}=3.3 –5%, +10% V, f=1MHz)

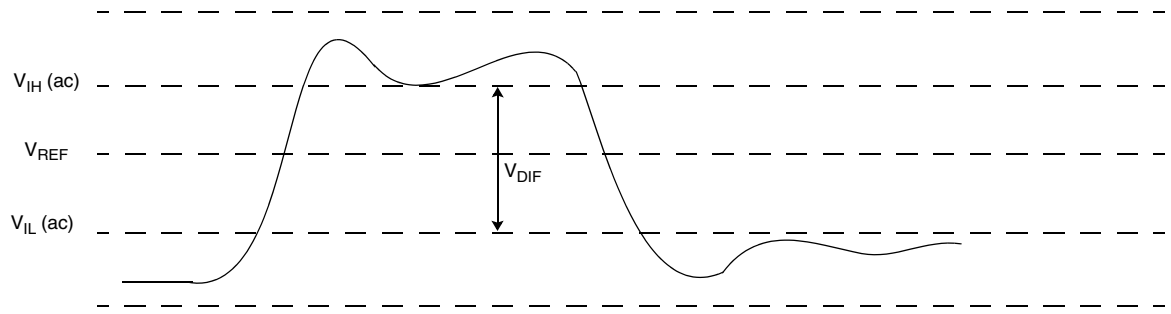
Symbol	Parameter	Test Condition	Max.	Units
C_{IN}	Input Capacitance	V_{IN} = 0V	4	pF
C_{OUT}	Data I/O Capacitance (DQ0–DQ35)	V_{OUT} = 0V	4	pF
K_{CLK}	K Clock Capacitance	V_{OUT} = 0V	3.5	pF

AC Input Characteristics (T_A= 0 to +85°C, V_{DD} = 3.3V ± 5%)

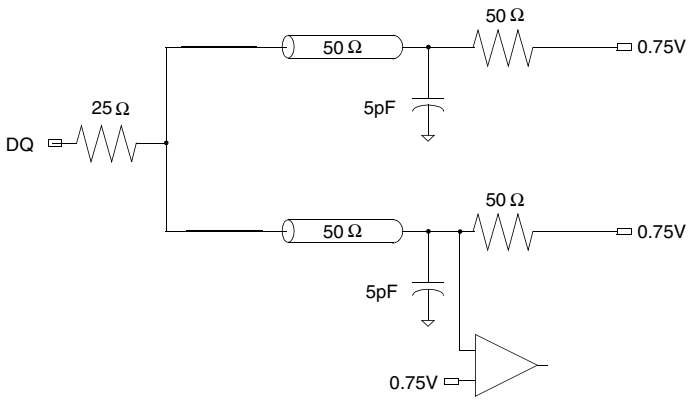
Symbol	Parameter	Min.	Max.	Units	Notes
V_{IH} (ac)	AC Input Logic High	V_{REF} + 400		mV	3, 4
V_{IL} (ac)	AC Input Logic Low		V_{REF} - 400	mV	3,
V_{DIF} (ac)	Clock Input Differential Voltage	800		mV	2, 3
V_{REF} (ac)	V_{REF} Peak-to-Peak AC Voltage		5% V_{REF} (DC)	mV	1, 5

1. The peak-to-peak AC component superimposed on V_{REF} may not exceed 5% of the DC component of V_{REF}.
2. SRAM performance is a function of clock input differential voltage (V_{DIF}).
3. To guarantee AC characteristics, V_{IH}, V_{IL}, T_{rise}, and T_{fall} of inputs and clocks must be within 20% of each other. If these conditions are not met then:
   - Setup time is measured from clock crossing to inputs at their switched V_{IHAC}, V_{ILAC} levels.
   - Hold time is measured from clock crossing to inputs switching out of their valid V_{IHAC}, V_{ILAC} levels.
4. See *AC Input Definition* on page 10.
5. A model of the SRAM internal V_{REF} is available. IBM recommends using this model in the board V_{REF} design.

AC Input Definition



AC Test Loading



AC Test Conditions (T_A = 0 to +85°C, V_{DD} = 3.3V ± 5%, V_{DDQ} = 1.5V)

Symbol	Parameter	Conditions	Units	Notes
V_{IH}	Input High Level	1.25	V	
V_{IL}	Input Low Level	0.25	V	
V_{REF}	Input Reference Voltage	0.75	V	
$V_{DIF-CLK}$	Differential Clocks Voltage	1.0	V	
V_{CM-CLK}	Clocks Common Mode Voltage	0.75	V	
T_R	Input Rise Time	0.5	ns	
T_F	Input Fall Time	0.5	ns	
	I/O Signals Reference Level (except K, C Clocks)	0.75	V	
	Clocks Reference Level	Differential Cross Point	V	
	Output Load Conditions			1

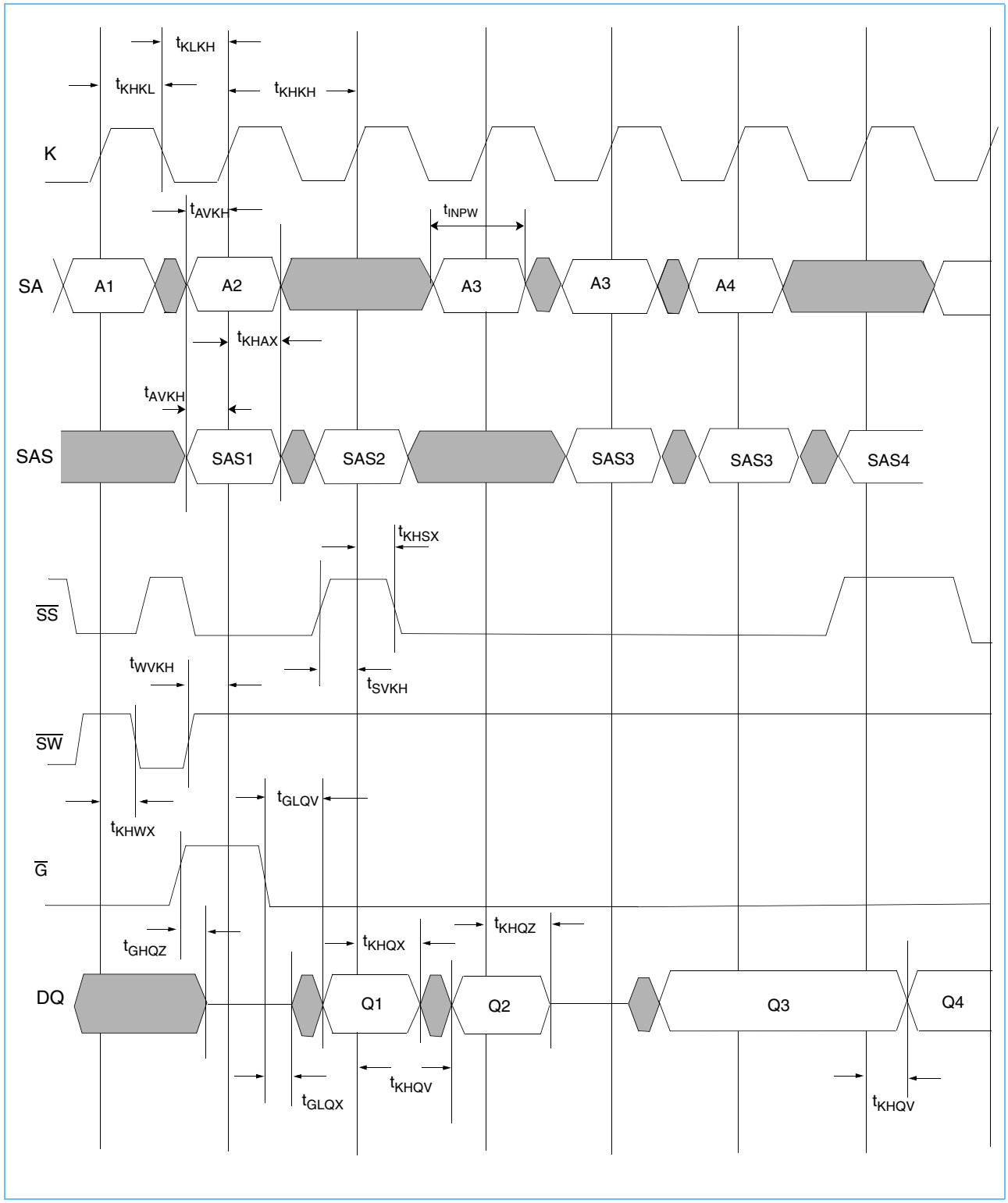
1. See *AC Test Loading* on page 10

AC Characteristics (T_A = 0 to +85°C, VDD = 3.3V ± 5%)

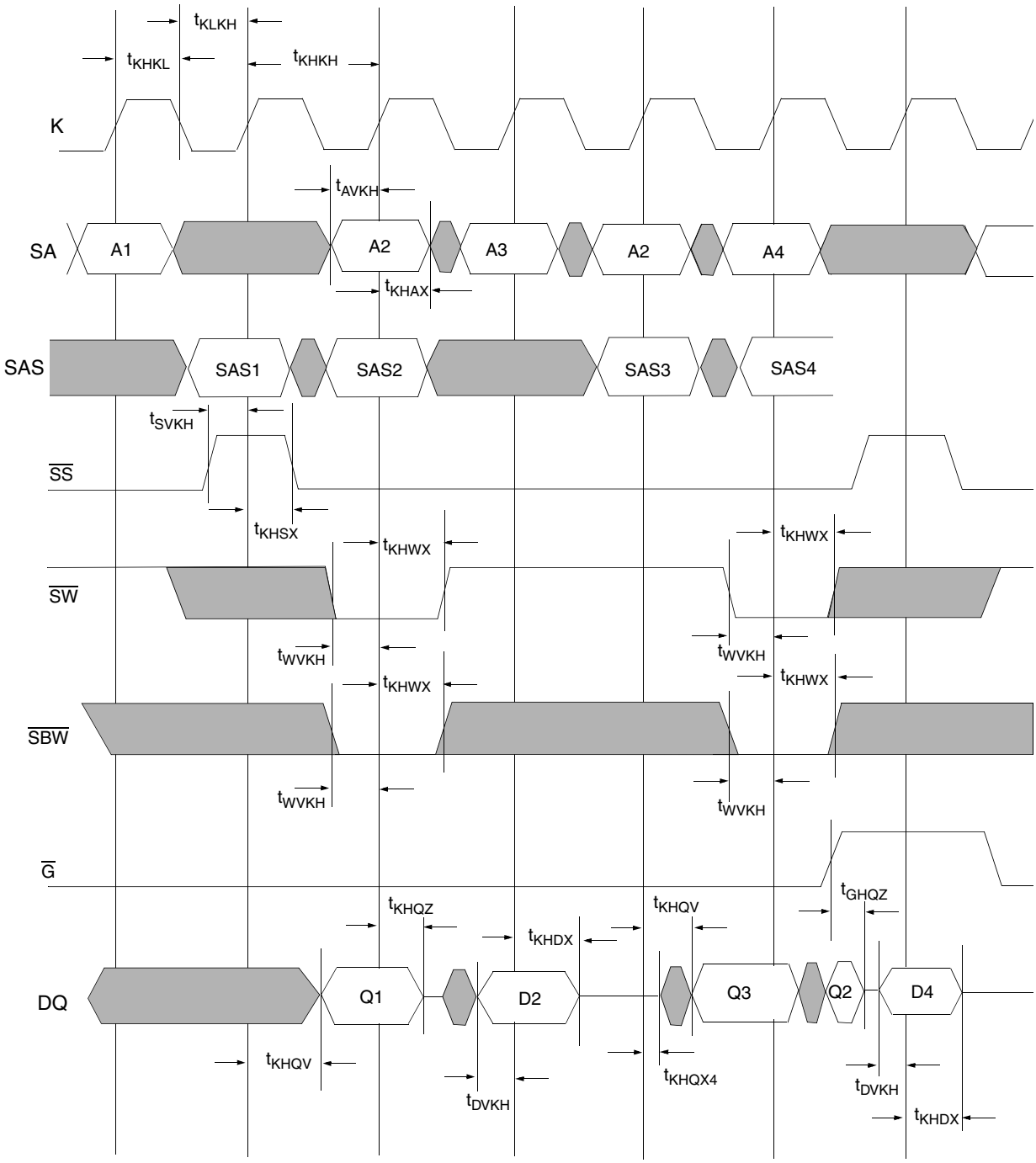
Symbol	Parameter	-28		-30		-33		-37		Units	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{KHKH}	Cycle Time	2.85		3.0		3.3		3.7		ns	
t_{KHKL}	Clock High Pulse Width	1.2		1.2		1.2		1.2		ns	
t_{KLKH}	Clock Low Pulse Width	1.2		1.2		1.2		1.2		ns	
t_{KHQV}	Clock to Output Valid		1.6		1.5		1.6		1.6	ns	1, 2, 3, 5
t_{KHQX}	Data Out Hold Time	0.65	1.6	0.65	1.5	0.65	1.6	0.65	1.6	ns	1, 2, 3
t_{AVKH}	Address Setup Time	0.3		0.3		0.3		0.3		ns	2, 3, 4
t_{KHAX}	Address Hold Time	0.6		0.5		0.6		0.7		ns	2, 4
t_{SVKH}	Sync Select Setup Time	0.3		0.3		0.3		0.3		ns	2, 3
t_{KHSX}	Sync Select Hold Time	0.6		0.5		0.6		0.7		ns	2
t_{WVKH}	Write Enables Setup Time	0.3		0.3		0.3		0.3		ns	2, 3
t_{KHWX}	Write Enables Hold Time	0.6		0.5		0.6		0.7		ns	2
t_{DVKH}	Data In Setup Time	0.3		0.3		0.3		0.3		ns	2, 3
t_{KHDX}	Data In Hold Time	0.6		0.5		0.6		0.7		ns	2
t_{INPW}	Input Pulse Width	1.3		1.2		1.3		1.5		ns	6
t_{KHQZ}	Clock High to Output High-Z	0.65	2.0	0.65	1.8	0.65	2.0	0.65	2.5	ns	1, 3
t_{KHQX4}	Clock High to Output Active	0.65		0.65		0.65		0.65		ns	1, 2, 3
t_{GHQZ}	Output Enable to High-Z		1.6		1.5		1.6		2.0	ns	1
t_{GLQX}	Output Enable to Low-Z	0.5		0.5		0.5		0.5		ns	1
t_{GLQV}	Output Enable to Output Valid		1.6		1.5		1.6		2.0	ns	1
t_{ZZR}	Sleep Mode Recovery Time		20		20		20		20	ns	
t_{ZZE}	Sleep Mode Enable Time		6.0		6.0		6.0		8.0	ns	
t_{SSZZ}	Sync-to-Sleep Time	2		2		2		2		ns	

1. See *AC Test Loading* on page 10.
2. To guarantee AC characteristics; V_{IH}, V_{IL}, T_{rise}, and T_{fall} of inputs and clocks must be within 20% of each other. If these conditions are not met then:
   - Setup time is measured from clock crossing to inputs at their switched V_{IHAC}, V_{ILAC} levels.
   - Hold time is measured from clock crossing to inputs switching out of their valid V_{IHAC}, V_{ILAC} levels.
3. Verified by design and tested without guardbands.
4. Includes late-select address (SAS).
5. Tested with guardband to a register latch access that guarantees the pipeline access.
6. Cannot have an input pulse width that consists of |minimum setup time| + |minimum hold time|.

Timing Diagram (Read and Deselect Cycles)



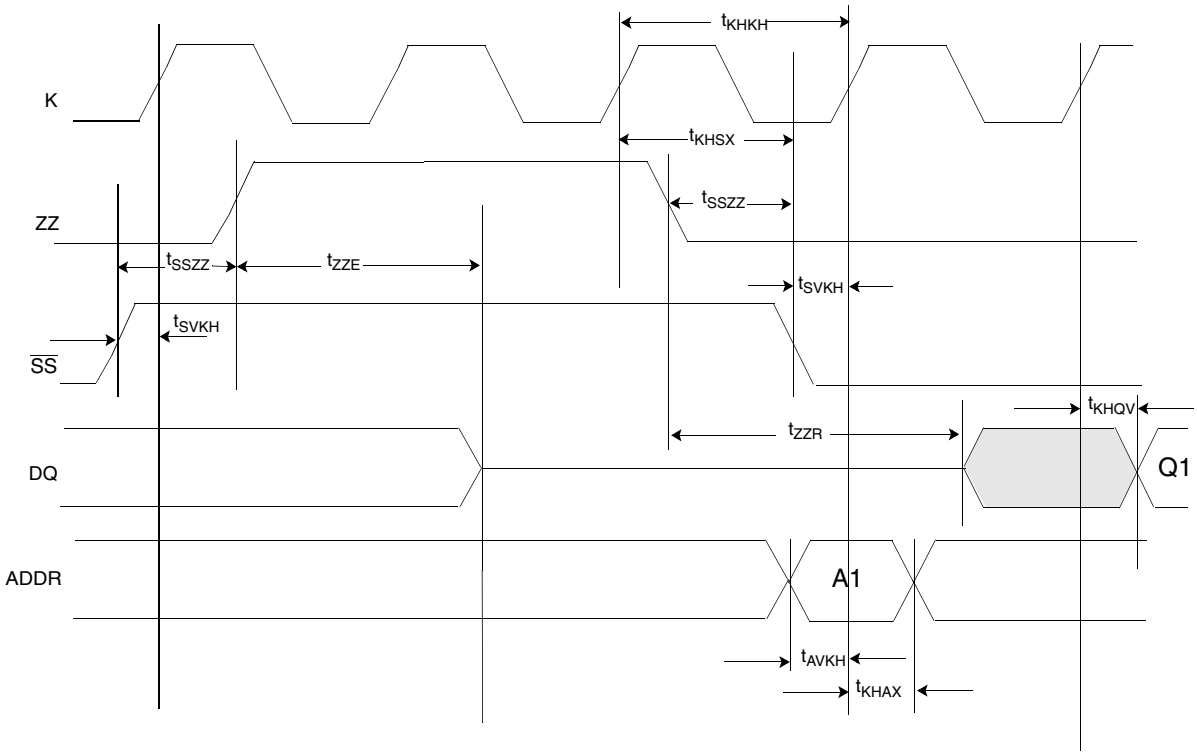
Timing Diagram (Read, Write Cycles)



NOTES:

1. D2 is the input data written in memory location A2.
2. Q2 is output data read from the write buffer, as a result of address A2 being a match from the last write cycle address.

Timing Diagram (Asynchronous Sleep Mode)



IEEE 1149.1 Tap and Boundary Scan

The SRAM provides a limited set of JTAG functions intended to test the interconnection between SRAM I/Os and printed circuit board traces or other components. There is no multiplexer in the path from I/O pins to the RAM core.

In conformance with IEEE standard 1149.1, the SRAM contains a TAP controller, instruction register, boundary scan register, bypass register and ID register.

The TAP controller has a standard 16-state machine that resets internally upon power-up; therefore, a TRST signal is not required.

Signal list:

- TCK: Test Clock
- TMS: Test Mode Select
- TDI: Test Data In
- TDO: Test Data Out

JTAG Recommended DC Operating Conditions (T_A = 0 to 85°C)

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
V_{IH1}	JTAG Input High Voltage	2.2	—	V_{DD} + 0.3	V	1
V_{IL1}	JTAG Input Low Voltage	-0.3	—	0.8	V	1
V_{OH1}	JTAG Output High Level	2.4	—	—	V	1, 2
V_{OL1}	JTAG Output Low Level	—	—	0.4	V	1, 3

1. All JTAG inputs/outputs are LVTTL compatible only.
2. $I_{OH1} \geq$ -I8mAI.
3. $I_{OL1} \geq$ +I8mAI.

JTAG AC Test Conditions (T_A = 0 to +85°C, V_{DD} = 3.3V ± 5%)

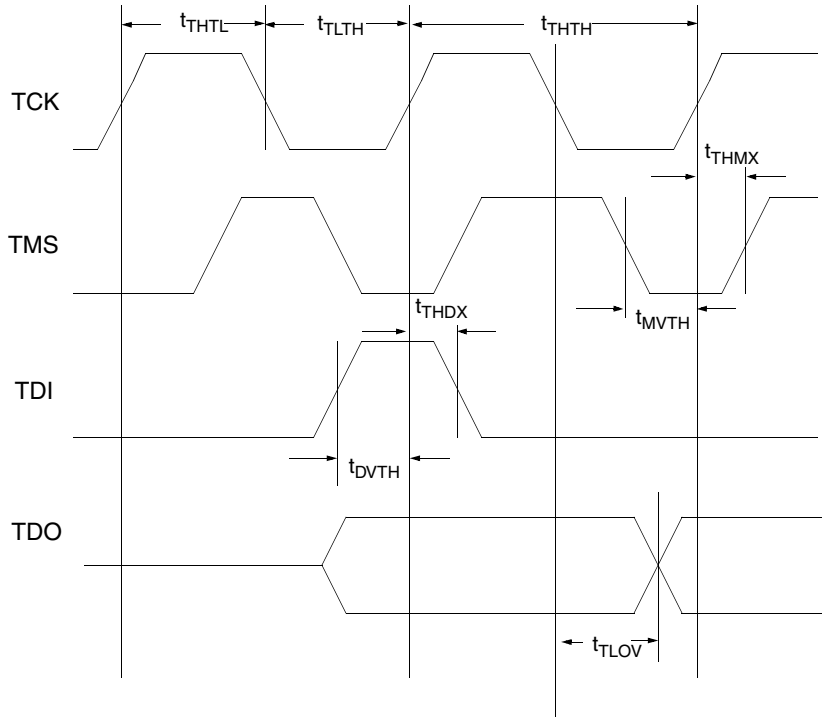
Symbol	Parameter	Conditions	Units
V_{IH1}	Input Pulse High Level	3.0	V
V_{IL1}	Input Pulse Low Level	0.0	V
T_{R1}	Input Rise Time	2.0	ns
T_{F1}	Input Fall Time	2.0	ns
	Input and Output Timing Reference Level	1.5	V

JTAG AC Characteristics (T_A= 0 to +85°C, V_{DD} = 3.3V ± 5%)

Symbol	Parameter	Min.	Max.	Units	Notes
t_{THTH}	TCK Cycle Time	20		ns	
t_{THTL}	TCK High Pulse Width	7		ns	
t_{TLTH}	TCK Low Pulse Width	7		ns	
t_{MVTH}	TMS Setup	4		ns	
t_{THMX}	TMS Hold	4		ns	
t_{DVTH}	TDI Setup	4		ns	
t_{THDX}	TDI Hold	4		ns	
t_{TLOV}	TCK Low to Valid Data		7	ns	1

1. *AC Test Loading* on page 10.

JTAG Timing Diagram



Scan Register Definition

Register Name	Bit Size x18	Bit Size x36
Instruction	3	3
Bypass	1	1
ID	32	32
Boundary Scan	51	70

1. The boundary-scan chain consists of the following bits:
   - 36 or 18 bits for data inputs depending on x36 or x18 configuration
   - 19 bits for SA1–SA18, SAS for x36; 20 bits for SA1–SA19, SAS for x18
   - 4 bits for $\overline{\text{SBWa}}$– $\overline{\text{SBWd}}$ in x36, 2 bits for $\overline{\text{SBWa}}$ and $\overline{\text{SBWb}}$ in x18
   - 9 bits for K, $\overline{\text{K}}$, ZQ, $\overline{\text{SS}}$, $\overline{\text{G}}$, $\overline{\text{SW}}$, ZZ, M1, and M2
   - 2 bits for place holders
2. K and $\overline{\text{K}}$ clocks connect to a differential receiver that generates a single-ended clock signal. This signal and its inverted value are used for boundary-scan sampling.

ID Register Definition

Part	Field Bit Number and Description				
	Revision Number (31:28) IBM Internal Use	Device Density and Configuration (27:18)	Vendor Definition (17:12)	Manufacture JEDEC Code (11:1)	Start Bit(0)
512K x 18	XXXX	1011110011	101010	00010100100	1
512K x 18	XXXX	1011110011	101010	00010100100	1

Instruction Set

Code	Instruction	Notes
000	SAMPLE-Z	1, 4
001	IDCODE	1
010	SAMPLE-Z	1, 4
011	PRIVATE	5
100	SAMPLE	3, 4
101	PRIVATE	5
110	PRIVATE	5
111	BYPASS	2

1. Places DQs in High-Z in order to sample all input data regardless of other SRAM inputs.
2. BYPASS register is initiated to V_{SS} when BYPASS instruction is invoked. The BYPASS register also holds the last serially loaded TDI when exiting the Shift DR state.
3. SAMPLE instruction does not place DQs in High-Z.
4. SRAM must not be in Sleep mode (ZZ = H) when SAMPLE-Z or SAMPLE instructions are invoked.
5. PRIVATE is reserved for the exclusive use of IBM. Invoking this instruction will cause improper SRAM functionality.

This part has not been designed to comply with the following sections of IEEE 1149.1:

- 7.2.1.b, e
- 7.7.1.a-f
- 10.1.1.b, e
- 10.7.1.a-d

Boundary Scan Order (x36)

Exit Order	Signal	Bump #	Exit Order	Signal	Bump #	Exit Order	Signal	Bump #
1	M2	5R	25	DQ12	6F	49	DQ26	2H
2	SAS	4P	26	DQ11	7E	50	DQ25	1H
3	SA2	4T	27	DQ13	6E	51	$\overline{SBWc}$	3G
4	SA4	6R	28	DQ14	7D	52	ZQ	4D
5	SA3	5T	29	DQ15	6D	53	$\overline{SS}$	4E
6	ZZ	7T	30	SA7	6A	54	PH[1]	4G
7	DQ2	6P	31	SA5	6C	55	PH[2]	4H
8	DQ3	7P	32	SA8	5C	56	$\overline{SW}$	4M
9	DQ4	6N	33	SA10	5A	57	$\overline{SBWd}$	3L
10	DQ6	7N	34	SA6	6B	58	DQ28	1K
11	DQ5	6M	35	SA9	5B	59	DQ27	2K
12	DQ0	6L	36	SA13	3B	60	DQ34	1L
13	DQ1	7L	37	PH[1]	2B	61	DQ35	2L
14	DQ7	6K	38	SA11	3A	62	DQ30	2M
15	DQ8	7K	39	SA12	3C	63	DQ29	1N
16	$\overline{SBWa}$	5L	40	SA15	2C	64	DQ31	2N
17	$\overline{K}$	4L	41	SA14	2A	65	DQ32	1P
18	K	4K	42	DQ20	2D	66	DQ33	2P
19	$\overline{G}$	4F	43	DQ21	1D	67	SA17	3T
20	$\overline{SBWb}$	5G	44	DQ22	2E	68	SA16	2R
21	DQ10	7H	45	DQ24	1E	69	SA1	4N
22	DQ9	6H	46	DQ23	2F	70	M1	3R
23	DQ16	7G	47	DQ18	2G			

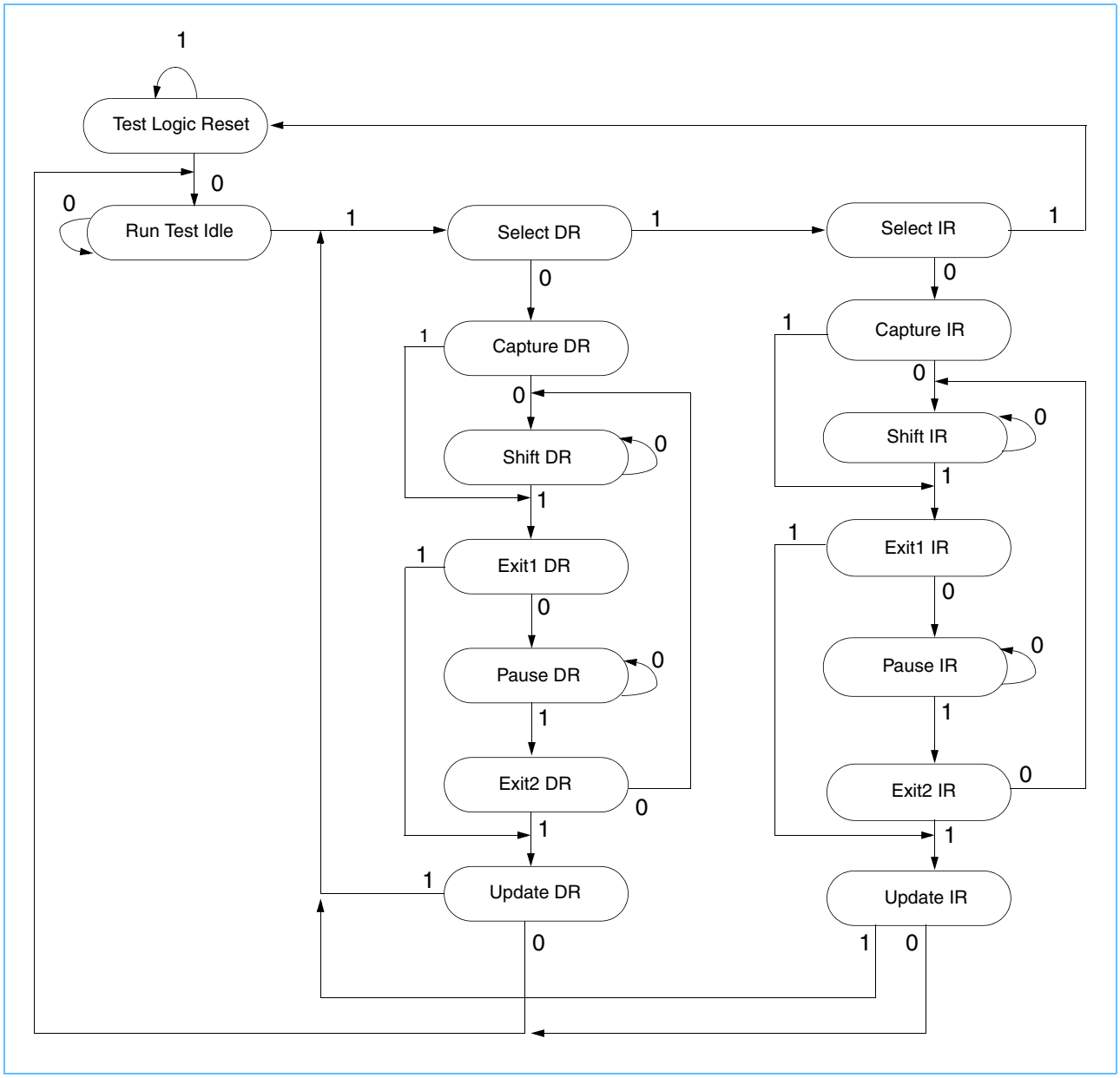
1. PH: Place holder connected to V_{SS}
2. PH: Place holder connected to V_{DD}

Boundary Scan Order (x18)

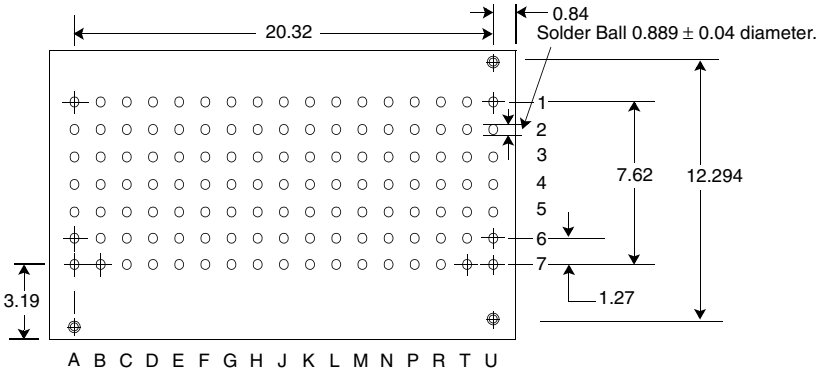
Exit Order	Signal	Bump #	Exit Order	Signal	Bump #
1	M2	5R	27	PH[1]	2B
2	SA2	6T	28	SA11	3A
3	SAS	4P	29	SA12	3C
4	SA4	6R	30	SA15	2C
5	SA3	5T	31	SA14	2A
6	ZZ	7T	32	DQ10	1D
7	DQ1	7P	33	DQ11	2E
8	DQ2	6N	34	DQ9	2G
9	DQ0	6L	35	DQ12	1H
10	DQ3	7K	36	$\overline{SBWb}$	3G
11	$\overline{SBWa}$	5L	37	ZQ	4D
12	$\overline{K}$	4L	38	$\overline{SS}$	4E
13	K	4K	39	PH[1]	4G
14	$\overline{G}$	4F	40	PH[2]	4H
15	DQ4	6H	41	$\overline{SW}$	4M
16	DQ8	7G	42	DQ13	2K
17	DQ5	6F	43	DQ17	1L
18	DQ6	7E	44	DQ14	2M
19	DQ7	6D	45	DQ15	1N
20	SA7	6A	46	DQ16	2P
21	SA5	6C	47	SA17	3T
22	SA8	5C	48	SA16	2R
23	SA10	5A	49	SA1	4N
24	SA6	6B	50	SA19	2T
25	SA9	5B	51	M1	3R

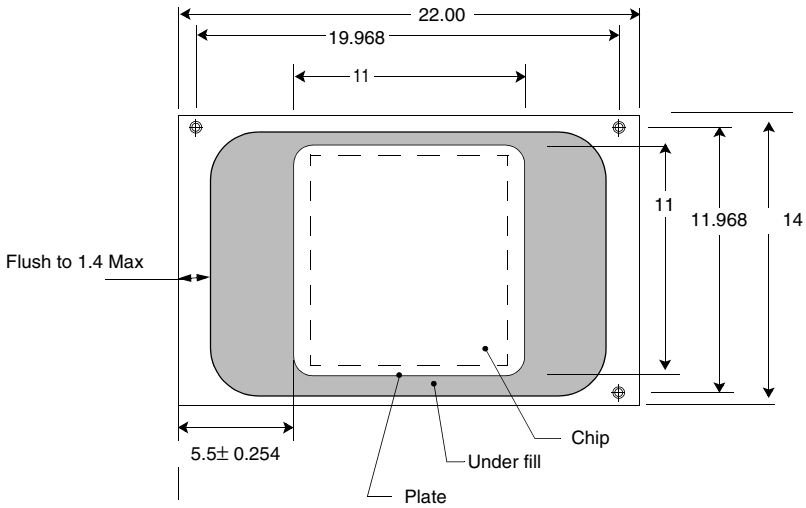
1. PH: Place holder connected to V_{SS}
2. PH: Place holder connected to V_{DD}

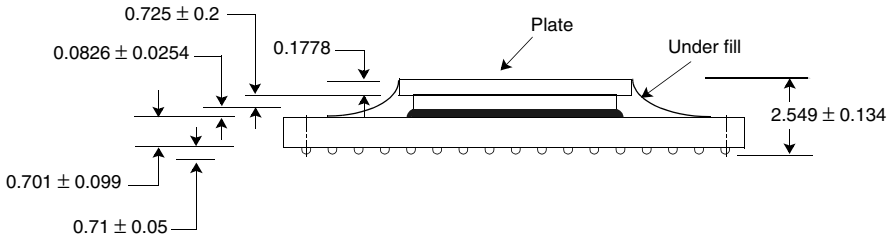
TAP Controller State Machine



7 x 17 BGA Dimensions







Note: All dimensions in millimeters

Revision Log

Rev	Contents of Modification
June 7, 2002	Initial release (00).

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