Features

- 8Mb: 256K x 36 or 512K x 18 organizations
  4Mb: 128K x 36 or 256K x 18 organizations
- CMOS Technology
- Double Data Rate and Single Data Rate Synchronous Modes of Operation
- Pipeline Mode of Operation
- Self-Timed Late Write with Full Data Coherency
- Single Differential Extended HSTL Clock
- +2.5V Power Supply, Ground, 1.6V V_{DDQ}, and 1.05V V_{REF}
- Extended HSTL Input
- HSTL Outputs
- Registered Addresses, Controls, and Data Ins
- Burst Mode of operation
- Common I/O
- Asynchronous Output Enable
- Boundary Scan using limited set of JTAG 1149.1 functions
- 9 x 17 Bump Ball Grid Array Package with SRAM JEDEC Standard Pinout and Boundary SCAN Order
- Programmable Impedance Output Drivers

Description

The IBM0436A4CFLBB, IBM0418A4CFLBB, IBM0418A8CFLBB, and IBM0436A8CFLBB SRAMs are Synchronous Pipeline Mode, high-performance CMOS Static Random Access Memories that are versatile, have wide I/O, and achieve 3.0ns cycle times. Differential CK clocks are used to initiate the read/write operation and all internal operations are self-timed. At the rising edge of the CK clock, all Addresses, Controls, and Data Ins are registered internally. Data Outs are updated from output registers off the next rising and falling edge of the K clock, hence the Double Data Rate. Internal Write buffers allow write data to follow one cycle after addresses and controls. The chip is operated with a single +2.5V power supply and is compatible with HSTL I/O interfaces.

x36 BGA Pinout (Top View)

	1	2	3	4	5	6	7	8	9
A	V_{SS}	V_{DDQ}	SA	SA	ZQ	SA	SA	V_{DDQ}	V_{SS}
B	DQ	DQ	SA	V_{SS}	B1(LD)	V_{SS}	SA	DQ	DQ
C	V_{SS}	V_{DDQ}	SA	SA	$\overline{G}$	SA	SA	V_{DDQ}	V_{SS}
D	DQ	DQ	NC	V_{SS}	V_{DD}	VSS	SA(8M)	DQ	DQ
E	V_{SS}	V_{DDQ}	V_{SS}	V_{DD}	V_{REF}	V_{DD}	V_{SS}	V_{DDQ}	V_{SS}
F	DQ	CQ	DQ	V_{DD}	V_{DD}	V_{DD}	DQ	CQ	DQ
G	V_{SS}	V_{DDQ}	V_{SS}	V_{SS}	CK	V_{SS}	V_{SS}	V_{DDQ}	V_{SS}
H	DQ	DQ	DQ	V_{DD}	$\overline{CK}$	V_{DD}	DQ	DQ	DQ
J	V_{SS}	V_{DDQ}	V_{SS}	V_{DD}	V_{DD}	V_{DD}	V_{SS}	V_{DDQ}	V_{SS}
K	DQ	DQ	DQ	V_{SS}	B2(WE)	V_{SS}	DQ	DQ	DQ
L	V_{SS}	V_{DDQ}	V_{SS}	$\overline{LBO}$	B3(DDR)	NC	V_{SS}	V_{DDQ}	V_{SS}
M	DQ	$\overline{CQ}$	DQ	V_{DD}	V_{DD}	V_{DD}	DQ	$\overline{CQ}$	DQ
N	V_{SS}	V_{DDQ}	V_{SS}	V_{DD}	V_{REF}	V_{DD}	V_{SS}	V_{DDQ}	V_{SS}
P	DQ	DQ	NC	V_{SS}	V_{DD}	V_{SS}	SA	DQ	DQ
R	V_{SS}	V_{DDQ}	V_{DD}	SA	SA1	SA	V_{DD}	V_{DDQ}	V_{SS}
T	DQ	DQ	SA	V_{SS}	SA0	V_{SS}	SA	DQ	DQ
U	V_{SS}	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}	V_{SS}

x18 BGA Pinout (Top View)

	1	2	3	4	5	6	7	8	9
A	V_{SS}	V_{DDQ}	SA	SA	ZQ	SA	SA	V_{DDQ}	V_{SS}
B	NC	DQ	SA	V_{SS}	B1(LD)	V_{SS}	SA	NC	DQ
C	V_{SS}	V_{DDQ}	SA	SA	$\overline{G}$	SA	SA	V_{DDQ}	V_{SS}
D	DQ	NC	NC	V_{SS}	V_{DD}	V_{SS}	SA(8M)	DQ	NC
E	V_{SS}	V_{DDQ}	V_{SS}	V_{DD}	V_{REF}	V_{DD}	V_{SS}	V_{DDQ}	V_{SS}
F	NC	CQ	NC	V_{DD}	V_{DD}	V_{DD}	DQ	NC	DQ
G	V_{SS}	V_{DDQ}	V_{SS}	V_{SS}	CK	V_{SS}	V_{SS}	V_{DDQ}	V_{SS}
H	DQ	NC	DQ	V_{DD}	$\overline{CK}$	V_{DD}	NC	DQ	NC
J	V_{SS}	V_{DDQ}	V_{SS}	V_{DD}	V_{DD}	V_{DD}	V_{SS}	V_{DDQ}	V_{SS}
K	NC	DQ	NC	V_{SS}	B2(WE)	V_{SS}	DQ	NC	DQ
L	V_{SS}	V_{DDQ}	V_{SS}	$\overline{LBO}$	B3(DDR)	NC	V_{SS}	V_{DDQ}	V_{SS}
M	DQ	NC	DQ	V_{DD}	V_{DD}	V_{DD}	NC	$\overline{CQ}$	NC
N	V_{SS}	V_{DDQ}	V_{SS}	V_{DD}	V_{REF}	V_{DD}	V_{SS}	V_{DDQ}	V_{SS}
P	NC	DQ	SA	V_{SS}	V_{DD}	V_{SS}	SA	NC	DQ
R	V_{SS}	V_{DDQ}	V_{DD}	SA	SA1	SA	V_{DD}	V_{DDQ}	V_{SS}
T	DQ	NC	SA	V_{SS}	SA0	V_{SS}	SA	DQ	NC
U	V_{SS}	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}	V_{SS}

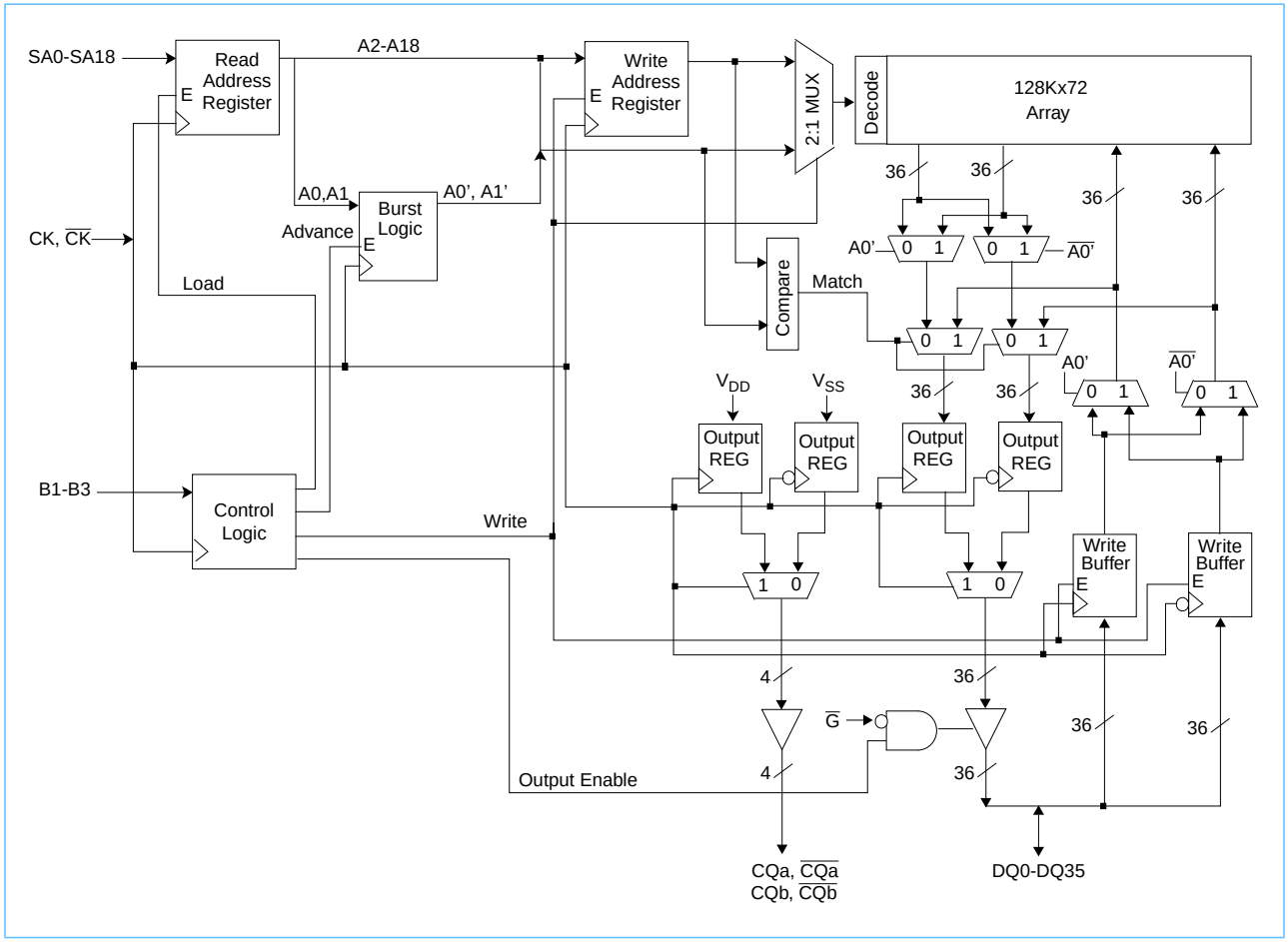
Pin Description

SA0-SA18	Address Inputs SA0-SA1 Burst control starting addresses SA0-SA18 for 512K x 18 SA0-SA17 for 256K x 36 SA0-SA17 for 256K x 18 SA0-SA16 for 128K x 36	TMS,TDI,TCK	IEEE 1149.1 Test Inputs (LVTTL levels)
DQ0-DQ35	Data I/O DQ0-DQ17 for 512K x 18 DQ0-DQ35 for 256K x 36	TDO	IEEE 1149.1 Test Output (LVTTL level)
CQ, $\overline{CQ}$	Output Differential Echo Clocks	V_{REF}(2)	Extended HSTL Input Reference Voltage
CK, $\overline{CK}$	Differential Input Register Clocks	V_{DD}	Power Supply (+2.5V)
B1	Synchronous Function Control Input. B1 = 0 Loads a new Address	V_{SS}	Ground
B2	Synchronous Function Control Input (WE). B2 = 0 starts Write & B2 = 1 starts Read.	V_{DDQ}	Output Power Supply
B3	Synchronous Function Control Input. B3 = 0 starts a DDR (Burst) operation. B3 = 1 starts a SDR (Single Data Rate)	ZQ	Input pin for Output Driver Impedance Control.
$\overline{LBO}$	Linear Burst Order, ($\overline{LBO}$ =1 interleave mode, $\overline{LBO}$ = 0 linear mode)	NC	No Connect
$\overline{G}$	Asynchronous Output Enable		

Ordering Information

Part Number	Organization	Speed	Leads
IBM0418A4CFLBB-3P	256K x 18	1.7ns Access / 3.0ns Cycle	9 x 17 BGA
IBM0418A4CFLBB-3	256K x 18	1.8ns Access / 3.5ns Cycle	9 x 17 BGA
IBM0418A4CFLBB-4	256K x 18	2.0ns Access / 4.0ns Cycle	9 x 17 BGA
IBM0418A4CFLBB-4H	256K x 18	2.0ns Access / 4.5ns Cycle	9 x 17 BGA
IBM0418A4CFLBB-5	256K x 18	2.5ns Access / 5.0ns Cycle	9 x 17 BGA
IBM0436A4CFLBB-3P	128K x 36	1.7ns Access / 3.0ns Cycle	9 x 17 BGA
IBM0436A4CFLBB-3	128K x 36	1.8ns Access / 3.5ns Cycle	9 x 17 BGA
IBM0436A4CFLBB-4	128K x 36	2.0ns Access / 4.0ns Cycle	9 x 17 BGA
IBM0436A4CFLBB-4H	128K x 36	2.0ns Access / 4.5ns Cycle	9 x 17 BGA
IBM0436A4CFLBB-5	128K x 36	2.5ns Access / 4.5ns Cycle	9 x 17 BGA
IBM0418A8CFLBB-3P	512K x 18	1.7ns Access / 3.0ns Cycle	9 x 17 BGA
IBM0418A8CFLBB-3	512K x 18	1.8ns Access / 3.5ns Cycle	9 x 17 BGA
IBM0418A8CFLBB-4	512K x 18	2.0ns Access / 4.0ns Cycle	9 x 17 BGA
IBM0418A8CFLBB-4H	512K x 18	2.0ns Access / 4.5ns Cycle	9 x 17 BGA
IBM0418A8CFLBB-5	512K x 18	2.5ns Access / 4.5ns Cycle	9 x 17 BGA
IBM0436A8CFLBB-3P	256K x 36	1.7ns Access / 3.0ns Cycle	9 x 17 BGA
IBM0436A8CFLBB-3	256K x 36	1.8ns Access / 3.5ns Cycle	9 x 17 BGA
IBM0436A8CFLBB-4	256K x 36	2.0ns Access / 4.0ns Cycle	9 x 17 BGA
IBM0436A8CFLBB-4H	256K x 36	2.0ns Access / 4.5ns Cycle	9 x 17 BGA
IBM0436A8CFLBB-5	256K x 36	2.5ns Access / 4.5ns Cycle	9 x 17 BGA

Block Diagram (x36 Double Data Rate Mode)



SRAM Features

SRAM Clocking

The SRAM main clocks, CK and $\overline{CK}$, run at the frequency of the internal SRAM core. The main clocks are used to register all inputs of the SRAM as well as generating Data Outs and Echo clocks.

Echo Clocks

Echo clocks CQ and $\overline{CQ}$ are generated from the CK and $\overline{CK}$ clocks with a delay representative of the DQ access time. They are generated from a path that mimics the entire data path from the input registers to the output drivers. When the CK clock goes high, the CQ clock will go high. Likewise the CQ clock goes high when the CK clock goes high.

Echo clocks keep running during Write and NOP operations. Echo clock operation is identical for both Double Data Rate and Single Data Rate operations. The close tracking of echo clocks and DQ timings allows the echo clocks to be used as capture clocks of the Data Outs by the receiving device.

Late Write

The Late Write function allows write data to be registered one CK cycle after addresses and controls. This feature eliminates one bus-turnaround cycle necessary when going from a Read to a Write operation. Late Write is accomplished by buffering write addresses and data so that the write operation occurs during the next write cycle. When a read cycle occurs after a write cycle, address and write data are stored temporarily in holding registers. During the third write cycle (Double Write Buffer) preceded by a read cycle, the SRAM array will be updated with address and data from the holding registers. Read cycle addresses are monitored to determine if read data is to be supplied from the SRAM array or the write buffer. **Full data coherency is maintained for both DDR and SDR operations**. As a result, NOP (write buffer flush) operations are not required going from write cycles to read cycles.

RQ Programmable Impedance

An external resistor, RQ, must be connected between the ZQ pin on the SRAM and V_{SS} to allow for the SRAM to adjust its output driver impedance. The value of RQ must be 5X the value of the intended line impedance driven by the SRAM. The allowable range of RQ to guarantee impedance matching is between 175Ω and 350Ω, with the tolerance described in Programmable Impedance Output Driver DC Electrical Characteristics on page 12. The RQ resistor should be placed less than two inches away from the ZQ ball on the SRAM module. The total external capacitance (including wiring) seen by the ZQ ball should be minimized (less than 7.5 pF).

Programmable Impedance and Power-Up Requirements

Periodic readjustment of the output driver impedance is necessary as the impedance is greatly affected by drifts in supply voltage and temperature. One evaluation occurs every 64 clock cycles and each evaluation may move the output driver impedance level only one step at a time towards the optimum level. The output driver has 64 discrete binary weighted steps. The impedance update of the output driver occurs when the SRAM is in High-Z. Write and Deselect operations will synchronously switch the SRAM into and out of High-Z, triggering an update. The user may choose to invoke asynchronous $\overline{G}$ updates by providing a $\overline{G}$ setup and hold about the K clock to guarantee the proper update. There are no power-up requirements for the SRAM; however, to guarantee optimum output driver impedance after power up, the SRAM needs 4096 clock cycles followed by a Low-Z to High-Z transition.

Power-Up and Power-Down Sequencing

The Power supplies need to be powered up in the following manner: V_{DD}, V_{DDQ}, V_{REF}, and Inputs. The power down sequencing must be the reverse. V_{DDQ} can be allowed to exceed V_{DD} by no more than 0.6V.

Synchronous Function Control

The function control is dependent on the state of the three function control pins captured on the rising edge of CK, as described in the following table ("n" refers to the current cycle, "n-1" refers to the previous internal SRAM cycle and "n+1" refers to the next internal SRAM cycle):

Synchronous Function Controls (Truth Table)

$B1_{(n-1)}$	$B2_{(n-1)}$	$B3_{(n-1)}$	$B1_{(n)}$	$B2_{(n)}$	$B3_{(n)}$	Function (n)
X	X	X	0	0	1	Load New Address, Single Data Rate (SDR) Write
X	X	X	0	0	0	Load New Address, Double Data Rate (DDR), Write
X	X	X	0	1	1	Load New Address, SDR Read
X	X	X	0	1	0	Load New Address, DDR Read
0	0	1	1	1	X	Continue Burst, SDR Write
0	0	0	1	1	X	Continue Burst, DDR Write
0	1	1	1	1	X	Continue Burst, SDR Read
0	1	0	1	1	X	Continue Burst, DDR Read
1	1	X	1	1	X	Continue Burst
X	X	X	1	0	X	NOP, (High-Z cycle n+1)
1	0	X	1	X	X	NOP, (High-Z cycle n+1)

Burst Order Definition

The DC state of the $\overline{LBO}$ pin determines the burst order of the addresses given the starting address when LD(B1) is Low. The following tables define the order of Addresses for the two different states of $\overline{LBO}$.

Address Sequence when $\overline{LBO}$ = 1 (Interleave Burst)

	SA1	SA0	SA1	SA0	SA1	SA0	SA1	SA0
Starting address	0	0	0	1	1	0	1	1
2nd address	0	1	0	0	1	1	1	0
3rd address	1	0	1	1	0	0	0	1
4th address	1	1	1	0	0	1	0	0

Address Sequence when $\overline{LBO}$ = 0 (Linear Burst)

	SA1	SA0	SA1	SA0	SA1	SA0	SA1	SA0
Starting address	0	0	0	1	1	0	1	1
2nd address	0	1	1	0	1	1	0	0
3rd address	1	0	1	1	0	0	0	1
4th address	1	1	0	0	0	1	1	0

Clock Truth Table

CK	B1(n)	B2(n)	B3 (n)	DQ (n)	DQ (n+1)	DQ (n+1.5)	MODE
L→H	L	H	H	X	D_{out} 0-35	Previous Data held	Read Cycle SDR
L→H	L	H	L	X	D_{out} 0-35a	D_{out} 0-35b	Read Cycle DDR
L→H	L	L	H	X	D_{IN} 0-35	X	Write Cycle SDR
L→H	L	L	L	X	D_{IN} 0-35a	D_{IN} 0-35b	Write Cycle DDR
L→H	H	L	X	X	High-Z	High-Z	NOP (Deselect) Cycle
L→H	H	H	X				Continue Burst Operation

Output Enable Truth Table

Operation (n, n+1)	$\overline{G}$ (n)	DQ (n)	DQ (n+1)
Read	L	D_{OUT} 0-35	D_{OUT} 0-35
Read	H	High-Z	High-Z
Write (B2 = L)	X	X	High-Z
Deselect (NOP) (B1 = H,B2 = L))	X	X	High-Z

Absolute Maximum Ratings

Item	Symbol	Rating	Units	Notes
Power Supply Voltage	V_{DD}	-0.5 to 2.825	V	1
Input Voltage	V_{IN}	-0.5 to 4.3	V	1, 2
DQ Input Voltage	V_{DQIN}	-0.5 to 2.825	V	1
Output Supply Voltage	V_{DDQ}	-0.5 to 2.825	V	1
Operating Temperature	T_A	0 to 85	°C	1
Junction Temperature	T_J	110	°C	1
Storage Temperature	T_{STG}	-55 to +125	°C	1
Short Circuit Output Current	I_{OUT}	25	mA	1

1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Excludes DQ inputs.

Recommended DC Operating Conditions (T_A = 0 to +85°C)

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Supply Voltage	V_{DD}	2.5V-5%	2.5	2.5V+10%	V	1
Output Driver Supply Voltage	V_{DDQ}	1.4	1.5	1.6	V	1
Input High Voltage	V_{IH}	V_{REF} +0.1	—	V_{DD} + 0.3	V	1, 2
Input Low Voltage	V_{IL}	-0.3	—	V_{REF} -0.1	V	1, 3
Input Reference Voltage	V_{REF}	0.8	1.0	1.05	V	1, 6
Clocks Signal Voltage	$V_{IN - CLK}$	-0.3	—	V_{DD} + 0.3	V	1, 4
Differential Clocks Signal Voltage	$V_{DIF - CLK}$	0.1	—	V_{DD}+ 0.6	V	1, 5
Clocks Common Mode Voltage	$V_{CM - CLK}$	0.8	—	1.05	V	1

1. All voltages referenced to V_{SS}. All V_{DD}, V_{DDQ}, and V_{SS} pins must be connected.
2. V_{IH}(Max)DC = V_{DD} + 0.3 V, V_{IH}(Max)AC = V_{DD}+ 0.85 V (pulse width ≤ 4.0ns).
3. V_{IL}(Min)DC = - 0.3 V, V_{IL}(Min)AC = -1.5 V (pulse width ≤ 4.0ns).
4. V_{IN-CLK} specifies the maximum allowable DC excursions of each differential clock (CK, $\overline{CK}$).
5. $V_{DIF-CLK}$ specifies the minimum Clock differential voltage required for switching.
6. Peak to Peak AC component superimposed on V_{REF} may not exceed 5% of V_{REF}.

DC Electrical Characteristics (T_A = 0 to +85°C, V_{DD} = 2.5V -5%, +10%)

Parameter	Symbol	Min.	Max.	Units	Notes
Average Power Supply Operating Current - **x36** I_{OUT} = 0, V_{IN} = (V_{IH} or V_{IL}), Device Selected	I_{DD3P} I_{DD3} I_{DD4} I_{DD4H} I_{DD5}	— —	690 620 540 505 470	mA	1, 3
Average Power Supply Operating Current - **x18** I_{OUT} = 0, V_{IN} = (V_{IH} or V_{IL}), Device Selected	I_{DD3P} I_{DD3} I_{DD4} I_{DD4H} I_{DD5}	— —	670 600 520 485 450	mA	1, 3
Power Supply Standby Current ($\overline{SS}$ = V_{IH}, ZZ = V_{IH}. All other inputs = V_{IH} or V_{IH}, I_{IH} = 0)	I_{SBSS}	—	150	mA	1
Input Leakage Current, any input (except JTAG) (V_{IN} = V_{SS} or V_{DDQ})	I_{LI}	-2	+2	µA	
Output Leakage Current (V_{OUT} = V_{SS} or V_{DDQ}, DQ in High-Z) Output Leakage Current (2.1V >V_{OUT} >V_{DDQ}, DQ in High-Z Output Leakage Current (V_{OUT} > 2.1V, DQ in High-Z	I_{LO}	-5	+5 +70 +120	µA	
Output “High” Level Voltage (I_{OH} = -8mA)	V_{OH}	V_{DDQ} -.4	V_{DDQ}	V	2, 4
Output “Low” Level Voltage (I_{OL} = +8mA)	V_{OL}	V_{SS}	V_{SS} + .4	V	2, 4
JTAG Leakage Current (V_{IN} = V_{SS} or V_{DD})	I_{LIJTAG}	-50	+10	µA	5

1. I_{OUT} = Chip Output Current.
2. Minimum Impedance Output Driver.
3. The numeric suffix indicates part operating at speed as indicated in the AC Characteristics figure on page 13: i.e., I_{DD4} indicates 4ns cycle time.
4. JEDEC Standard JESD8-6 Class 1 Compatible.
5. For JTAG inputs only.

PBGA Thermal Characteristics

Item	Symbol	Rating	Units
Thermal Resistance Junction to Case	RΘJC	1	°C/W

Capacitance (T_A = 0 to +85°C, V_{DD} = 2.5V -5%, +10%, f = 1MHz)

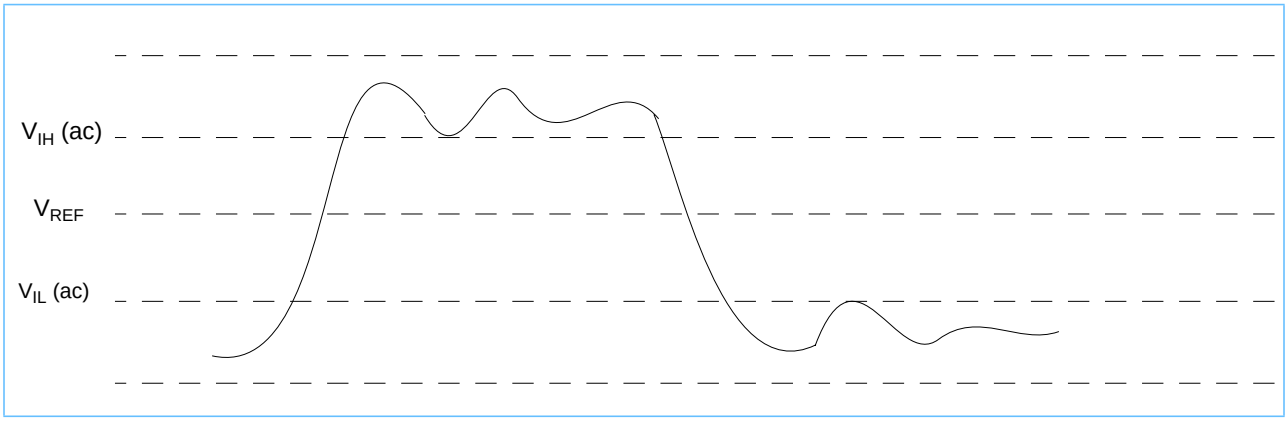
Parameter	Symbol	Test Condition	Max	Units
Input Capacitance	C_{IN}	V_{IN} = 0V	4	pF
Data I/O Capacitance (DQ0-DQ35)	C_{OUT}	V_{OUT} = 0V	5.6	pF
K Clock Capacitance	$C_{KCL}K$	V_{OUT} = 0V	3.5	pF

AC Input Characteristics

Item	Symbol	Min	Max	Units	Notes
AC Input Logic High	V_{IH} (ac)	V_{REF} + 0.4		V	3
AC Input Logic Low	V_{IL} (ac)		V_{REF} - 0.4	V	3
Clock Input Differential Voltage	V_{DIF} (ac)	0.7		V	2
V_{REF} Peak to Peak ac Voltage	V_{REF} (ac)		5% V_{REF} (dc)	V	1

1. The peak to peak AC component superimposed on V_{REF} may not exceed 5% of the DC component of V_{REF}.
2. Performance is a function of V_{IH} and V_{IL} levels to clock inputs.
3. See the AC Input Definition figure below.

AC Input Definition



Programmable Impedance Output Driver DC Electrical Characteristics

(T_A = 0 to +85°C, V_{DD} = 2.5V -5%, +10%, V_{DDQ} = 1.5V)

Parameter	Symbol	Min.	Max.	Units	Notes
Output “High” Level Voltage	V_{OH}	V_{DDQ} / 2	V_{DDQ}	V	1, 3
Output “Low” Level Voltage	V_{OL}	V_{SS}	V_{DDQ} / 2	V	2, 3

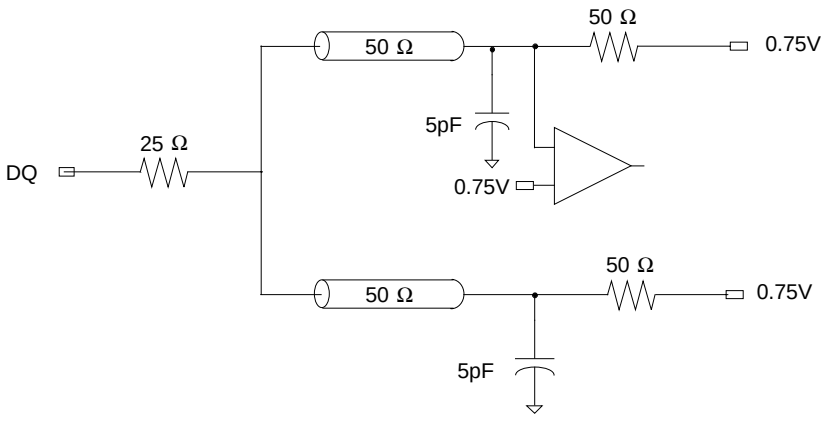
1. $I_{OH} = \left(\frac{VDDQ}{2}\right) / \left(\frac{RQ}{5} + 5\right) \pm 15\%$ @ $V_{OH} = V_{DDQ}$ / 2 For: 150Ω ≤ RQ ≤ 350Ω.
2. $I_{OL} = \left(\frac{VDDQ}{2}\right) / \left(\frac{RQ}{5}\right) \pm 15\%$ @ $V_{OL} = V_{DDQ}$ / 2 For: 150Ω ≤ RQ ≤ 350Ω.
3. Parameter tested with RQ = 250Ω and V_{DDQ} = 1.5V.

AC Test Conditions (T_A = 0 to +85°C, V_{DD} = 2.5V -5%, +10%, V_{DDQ} = 1.5V)

Parameter	Symbol	Conditions	Units	Notes
Input High Level	V_{IH}	1.7	V	
Input Low Level	V_{IL}	0.3	V	
Input Reference Voltage	V_{REF}	1.0	V	
Differential Clocks Voltage	$V_{DIF-CLK}$	1.0	V	
Clocks Common Mode Voltage	V_{CM-CLK}	1.0	V	
Input Rise Time	T_R	0.5	ns	
Input Fall Time	T_F	0.5	ns	
I/O Signals Reference Level (except CK Clocks)		1.0	V	
Clocks Reference Level		Differential Cross Point	V	
Output Load Conditions				1

1. See the AC Test Loading figure below.

AC Test Loading

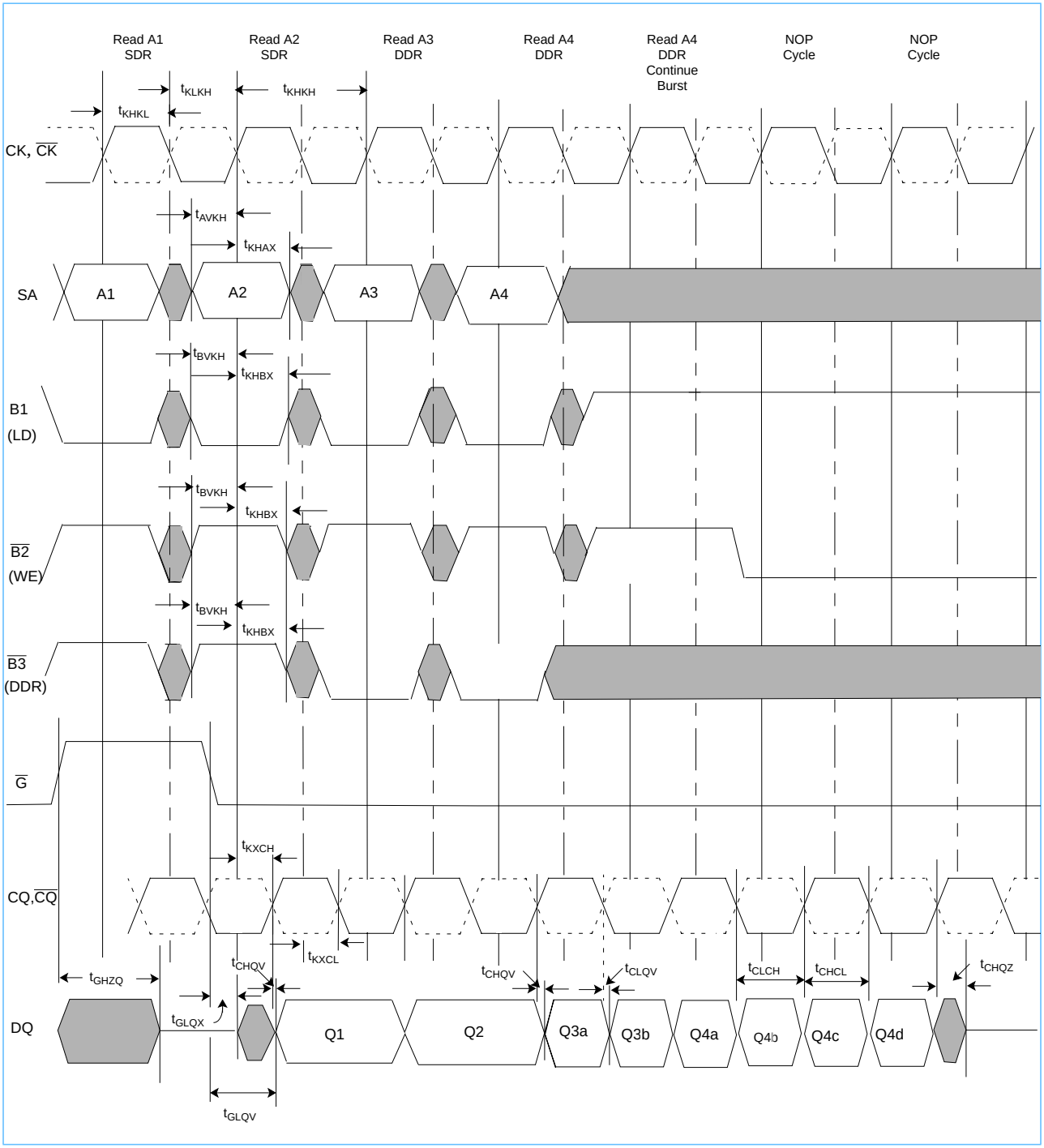


AC Characteristics (T_A = 0 to +85°C, V_{DD} = 2.5V -5%, +10%)

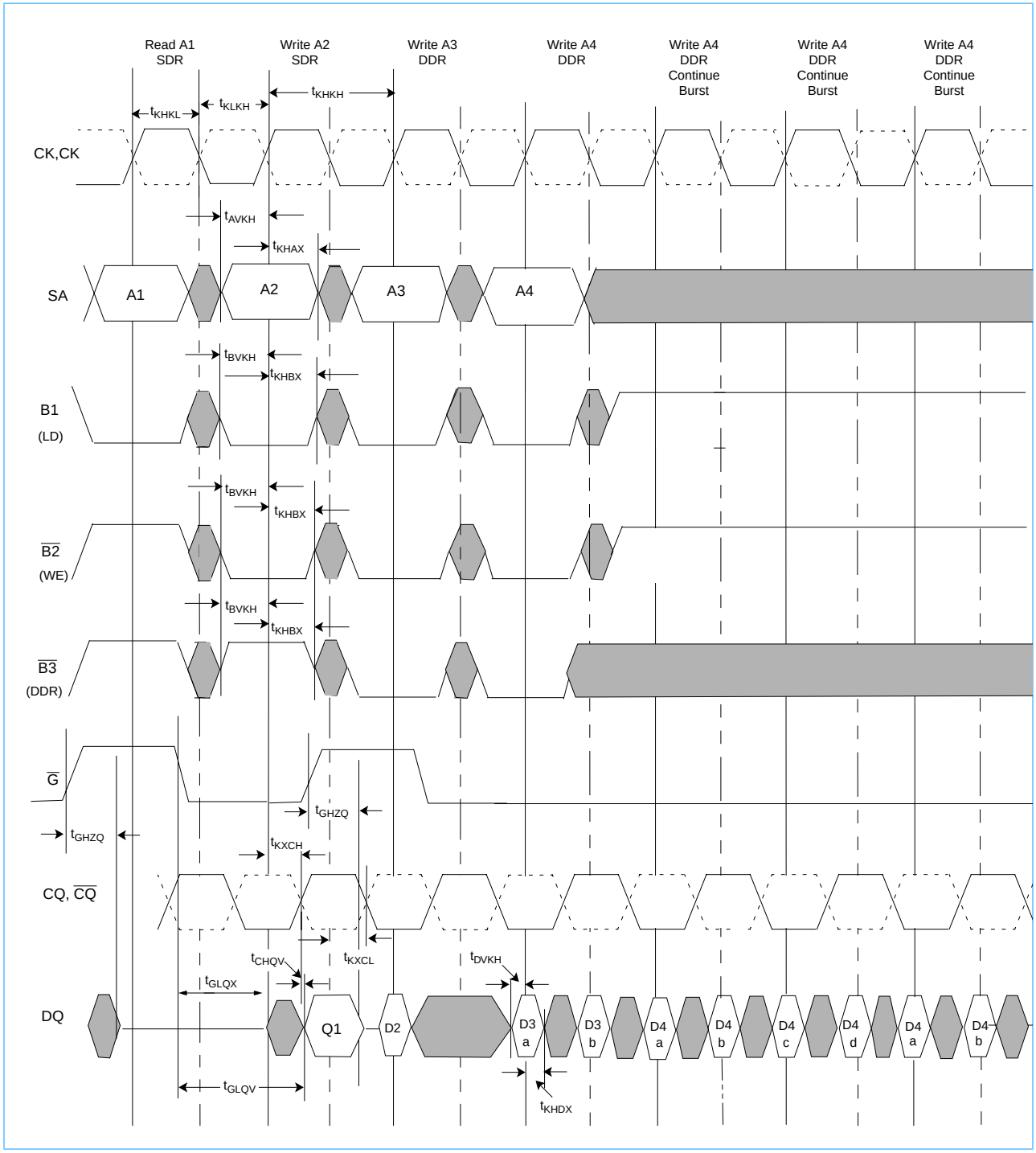
Parameter	Sym-bol	-3P		-3		-4		-4H		-5		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Cycle Time	t_{KHKH}	3.0	—	3.5	—	4.0	—	4.5	—	5.0	—	ns	
CK Clock High Pulse Width	t_{KHKL}	1.4	—	1.5	—	1.5	—	1.5	—	2.0	—	ns	
CK Clock Low Pulse Width	t_{KLKH}	1.4	—	1.5	—	1.5	—	1.5	—	2.0	—	ns	
Address Setup Time	t_{AVKH}	0.35	—	0.35	—	0.5	—	0.5	—	0.5	—	ns	3, 5
Address Hold Time	t_{KHAX}	0.4	—	0.4	—	0.5	—	0.5	—	0.5	—	ns	3, 5
Function Control (B1,B2,B3) Setup Time	t_{BVKH}	0.4	—	0.4	—	0.5	—	0.5	—	0.5	—	ns	3, 5
Function Control (B1,B2,B3) Hold Time	t_{KHBX}	0.3	—	0.4	—	0.5	—	0.5	—	0.5	—	ns	3, 5
Data In Setup Time	t_{DVKH}	0.4	—	0.4	—	0.4	—	0.4	—	0.4	—	ns	3, 5
Data In Hold Time	t_{KHDX}	0.3	—	0.4	—	0.4	—	0.4	—	0.4	—	ns	3, 5
Echo Clock (CQ) High Pulse Width	t_{CHCL}	t_{KHKL} -0.1	t_{KHKL} +0.1	t_{KHKL} -0.1	t_{KHKL} +0.1	t_{KHKL} -0.1	t_{KHKL} +0.1	t_{KHKL} -0.1	t_{KHKL} +0.1	t_{KHKL} -0.1	t_{KHKL} +0.1	ns	
Echo Clock (CQ) Low Pulse Width	t_{CLCH}	t_{KLKH} -0.1	t_{KLKH} +0.1	t_{KLKH} -0.1	t_{KLKH} +0.1	t_{KLKH} -0.1	t_{KLKH} +0.1	t_{KLKH} -0.1	t_{KLKH} +0.1	t_{KLKH} -0.1	t_{KLKH} +0.1	ns	
Clock (CK) crossing to Echo clock (CQ) High	t_{KXCH}	—	1.7	—	1.8	—	2.0	—	2.0	—	2.5	ns	
Clock (CK) crossing to Echo clock (CQ) Low	t_{KXCL}	—	1.7	—	1.8	—	2.0	—	2.0	—	2.5	ns	
Echo clock (CQ) High to output valid	t_{CHQV}	—	0.2	—	0.2	—	0.2	—	0.2	—	0.2	ns	4
Echo clock (CQ) Low to output valid	t_{CLQV}	—	0.2	—	0.2	—	0.2	—	0.2	—	0.2	ns	4
Echo clock (CQ) High to output Hold	t_{CHQX}	-0.2	—	-0.2	—	-0.2	—	-0.2	—	-0.2		ns	4
Echo clock (CQ) Low to output Hold	t_{CLQX}	-0.2	—	-0.2	—	-0.2	—	-0.2	—	-0.2		ns	4
Echo clock (CQ) High to output High-Z	t_{CHQZ}	—	0.2	—	0.2	—	0.2	—	0.2	—	0.2	ns	4
Echo clock (CQ) High to output Low-Z	t_{CHLZ}	-0.2	—	-0.2	—	-0.2	—	-0.2	—	-0.2		ns	4
Output Enable ($\overline{G}$) High to High-Z	t_{GHQZ}	—	2.5	—	2.5	—	2.5	—	2.5	—	3.0	ns	1
Output Enable ($\overline{G}$) Low to Low-Z	t_{GLQX}	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	ns	1
Output Enable ($\overline{G}$) to Output Valid	t_{GLQV}	—	2.0	—	2.0	—	2.0	—	2.0	—	2.5	ns	1
Output Enable ($\overline{G}$) Setup Time	t_{GHKH}	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	ns	1, 2
Output Enable ($\overline{G}$) Hold TIme	t_{KHGX}	1.0	—	1.0	—	1.0	—	1.0	—	1.0	—	ns	1, 2

1. See the AC Test Loading figure on page 12.
2. Output Driver Impedance update specifications for $\overline{G}$ induced updates. Write and NOP cycles will also induce Output Driver updates during High-Z.
3. During normal operation, V_{IH},V_{IL},T_{RISE}, and T_{FALL} of inputs must be within 20% of V_{IH}, V_{IL}, T_{RISE}, and T_{FAL} of Clock.
4. These values will be guaranteed by design.for all sorts.
5. Values will be guaranteed by design.for -3P and -3 speed sorts.

Read and NOP Cycles



Read Write Cycles



IEEE 1149.1 TAP and Boundary Scan

The SRAM provides a limited set of JTAG functions intended to test the interconnection between SRAM I/Os and printed circuit board traces or other components. There is no multiplexer in the path from I/O pins to the RAM core.

In conformance with IEEE Std. 1149.1, the SRAM contains a TAP controller, Instruction register, Boundary Scan register, Bypass register and ID register.

The TAP controller has a standard 16-state machine that resets internally upon power-up, therefore, TRST signal is not required.

Signal List

- TCK: Test Clock
- TMS: Test Mode Select
- TDI: Test Data In
- TDO: Test Data Out

JTAG DC Operating Characteristics (T_A = 0 to +85°C)

Operates with JEDEC Standard 8-5 (2.5V) logic signal levels

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
JTAG Input High Voltage	V_{IH1}	1.7	—	V_{DD}+0.3	V	1
JTAG Input Low Voltage	V_{IL1}	-0.3	—	0.8	V	1
JTAG Output High Level	V_{OH1}	2.1	—	—	V	1, 2
JTAG Output Low Level	V_{OL1}	—	—	0.2	V	1, 3

1. All JTAG inputs and outputs are LVTTL compatible only.
2. $I_{OH1} \geq -|2mA|$.
3. $I_{OL1} \geq +|2mA|$.

JTAG AC Test Conditions (T_A = 0 to +85°C, V_{DD} = 2.5V -5%, +10%)

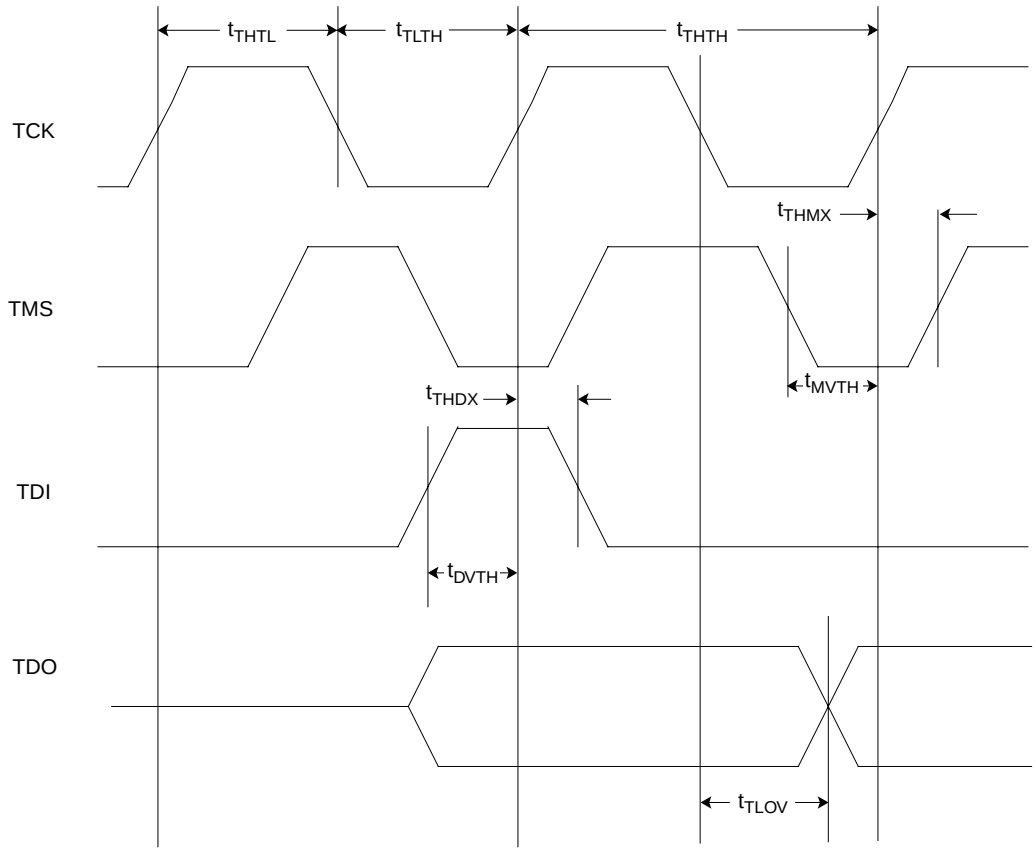
Parameter	Symbol	Conditions	Units
Input Pulse High Level	V_{IH1}	3.0	V
Input Pulse Low Level	V_{IL1}	0.0	V
Input Rise Time	T_{R1}	2.0	ns
Input Fall Time	T_{F1}	2.0	ns
Input and Output Timing Reference Level		1.5	V

JTAG AC Characteristics (T_A = 0 to +85°C, V_{DD} = 2.5V -5%, +10%)

Parameter	Symbol	Min.	Max.	Units	Notes
TCK Cycle Time	t_{THTH}	20	—	ns	
TCK High Pulse Width	t_{THTL}	7	—	ns	
TCK Low Pulse Width	t_{TLTH}	7	—	ns	
TMS Setup	t_{MVTH}	4	—	ns	
TMS Hold	t_{THMX}	4	—	ns	
TDI Setup	t_{DVTH}	4	—	ns	
TDI Hold	t_{THDX}	4	—	ns	
TCK Low to Valid Data	t_{TLOV}	—	7	ns	1

1. See the AC Test Loading figure on page 12.

JTAG Timing Diagram



Scan Register Definition

Register Name	Bit Size x18	Bit Size x36
Instruction	3	3
Bypass	1	1
ID	32	32
Boundary Scan *	49	68

* The Boundary Scan chain consists of the following bits:

- 36 or 18 bits for Data Inputs Depending on x18 or x36 Configuration
- 18 bits for SA0 - SA17 for x36, 19 bits for SA0 - SA18 for x18
- 4 bits for EC, $\overline{EC}$, EC, $\overline{EC}$ x36, 2 bits for EC, $\overline{EC}$ in x18
- 8 bits for CK, $\overline{CK}$, ZQ, $\overline{G}$, $\overline{LBO}$, B1, B2, B3
- 2 bits for Place Holders

* CK and $\overline{CK}$ clocks connect to a differential receiver that generates a single-ended clock signal. This signal and its inverted value are used for Boundary Scan sampling.

ID Register Definition

Part	Field Bit Number and Description				
	Revision Number (31:28)	Device Density and Configuration (27:18)	Vendor Definition (17:12)	Manufacturer JEDEC Code (11:1)	Start Bit(0)
128K x36	xxxx	011 010 1100	xxxxxx	000 101 001 00	1
256K x 18	xxxx	011 100 1011	xxxxxx	000 101 001 00	1
512K x 18	xxxx	101 111 0011	xxxxxx	000 101 001 00	1
256K x 36	xxxx	101 101 0100	xxxxxx	000 101 001 00	1

Instruction Set

Code	Instruction	Notes
000	SAMPLE-Z	1
001	IDCODE	
010	SAMPLE-Z	1
011	PRIVATE	5
100	SAMPLE	4
101	PRIVATE	5
110	PRIVATE	5
111	BYPASS	2, 3

1. Places DQs in High-Z in order to sample all input data regardless of other SRAM inputs.
2. TDI is sampled as an input to the first ID register to allow for the serial shift of the external TDI data.
3. BYPASS register is initiated to V_{SS} when BYPASS instruction is invoked. The BYPASS register also holds the last serially loaded TDI when exiting the Shift DR state.
4. SAMPLE instruction does not place DQs in High-Z.
5. This instruction is reserved for the exclusive use of IBM. Invoking this instruction will cause improper SRAM functionality.

List of IEEE 1149.1 Standard Violations:

- 7.2.1.b, e
- 7.7.1.a-f
- 10.1.1.b, e
- 10.7.1.a-d
- 6.1.1.d

Boundary Scan Order (x36)

Exit Order	Signal	Bump #	Exit Order	Signal	Bump #	Exit Order	Signal	Bump #
1	SA1	5R	24	CQ	8F	47	CQ	2F
2	SA0	5T	25	DQ	9D	48	DQ	1F
3	SA	6R	26	DQ	7F	49	DQ	3H
4	SA	7T	27	DQ	8D	50	DQ	2H
5	SA	7P	28	DQ	9B	51	DQ	1H
6	DQ	8T	29	DQ	8B	52	ZQ	5A
7	DQ	9T	30	SA(8Mb)[2]	7D	53	B1	5B
8	DQ	8P	31	SA	7C	54	B2	5K
9	DQ	7M	32	SA	7B	55	B3	5L
10	DQ	9P	33	SA	7A	56	$\overline{\text{LBO}}$	4L
11	$\overline{\text{CQ}}$	8M	34	SA	6C	57	DQ	1K
12	DQ	9M	35	SA	6A	58	DQ	2K
13	DQ	7K	36	SA	4A	59	DQ	3K
14	DQ	8K	37	SA	4C	60	DQ	1M
15	DQ	9K	38	SA	3A	61	$\overline{\text{CQ}}$	2M
16	PH[1,4]	6L	39	SA	3B	62	DQ	1P
17	$\overline{\text{CK}}$	5H	40	SA	3C	63	DQ	3M
18	CK	5G	41	PH[1](16Mb)[3]	3D	64	DQ	2P
19	$\overline{\text{G}}$	5C	42	DQ	2B	65	DQ	1T
20	DQ	9H	43	DQ	1B	66	DQ	2T
21	DQ	8H	44	DQ	2D	67	SA	3T
22	DQ	7H	45	DQ	3F	68	SA	4R
23	DQ	9F	46	DQ	1D			

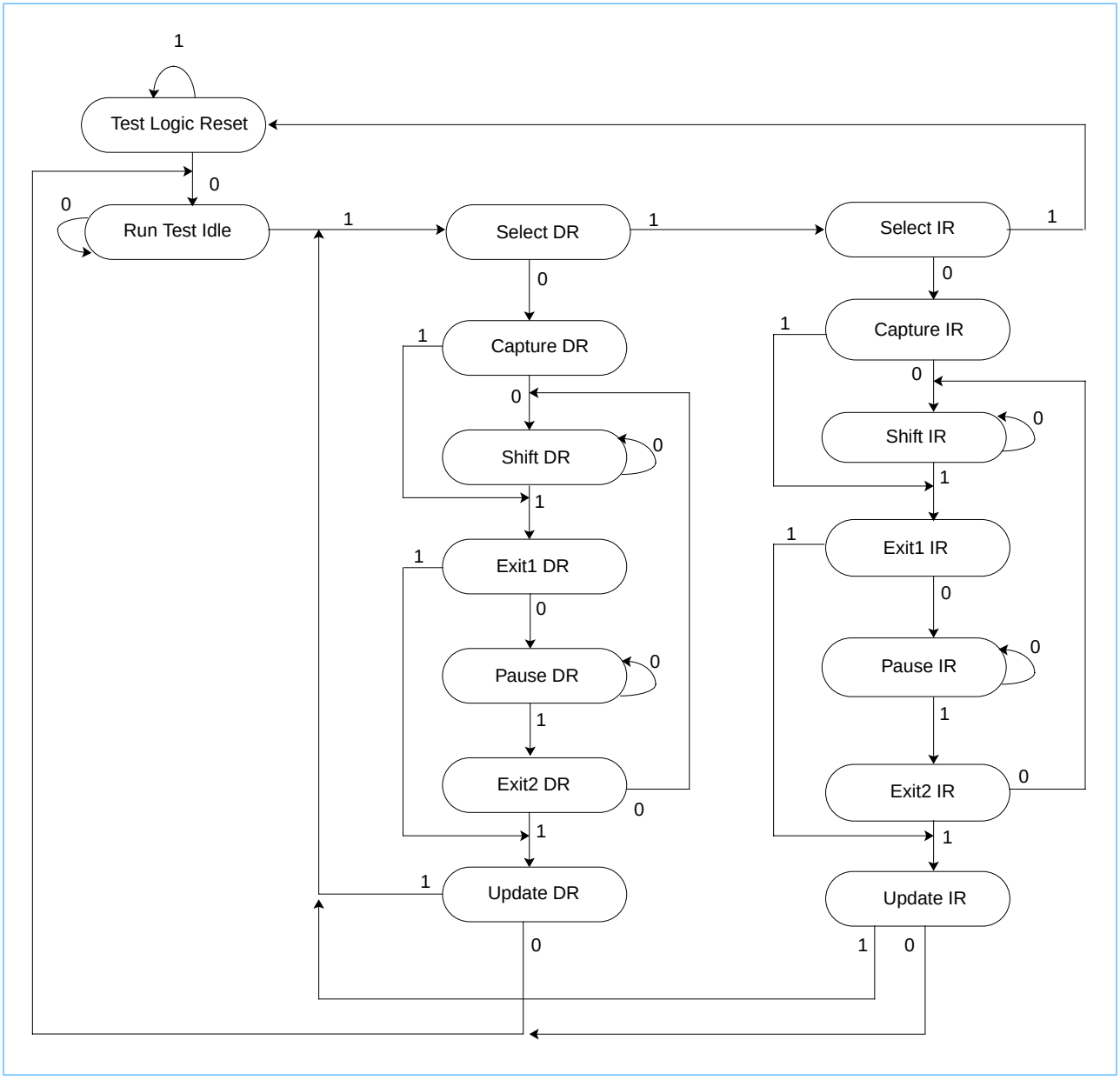
1. PH pins are place holders. BGA bump is a NC (no connect). PH pins are forced to V_{SS}.
2. For 4Mb density, SA(8Mb) becomes a Place Holder (PH).
3. Reserved address bit for 16 Mb density.
4. Reserved for Mode pin.

Boundary Scan Order (x18)

Exit Order	Signal	Bump #	Exit Order	Signal	Bump #
1	SA1	5R	26	SA	4A
2	SA0	5T	27	SA	4C
3	SA	6R	28	SA	3A
4	SA	7T	29	SA	3B
5	SA	7P	30	SA	3C
6	DQ	8T	31	PH[1](16Mb)[3]	3D
7	DQ	9P	32	DQ	2B
8	$\overline{CQ}$	8M	33	DQ	1D
9	DQ	7K	34	CQ	2F
10	DQ	9K	35	DQ	3H
11	PH[1,4]	6L	36	DQ	1H
12	$\overline{CK}$	5H	37	ZQ	5A
13	CK	5G	38	B1	5B
14	$\overline{G}$	5C	39	B2	5K
15	DQ	8H	40	B3	5L
16	DQ	9F	41	$\overline{LBO}$	4L
17	DQ	7F	42	DQ	2K
18	DQ	8D	43	DQ	1M
19	DQ	9B	44	DQ	3M
20	SA (8Mb)[2]	7D	45	DQ	2P
21	SA	7C	46	DQ	1T
22	SA	7B	47	SA	3P
23	SA	7A	48	SA	3T
24	SA	6C	49	SA	4R
25	SA	6A			

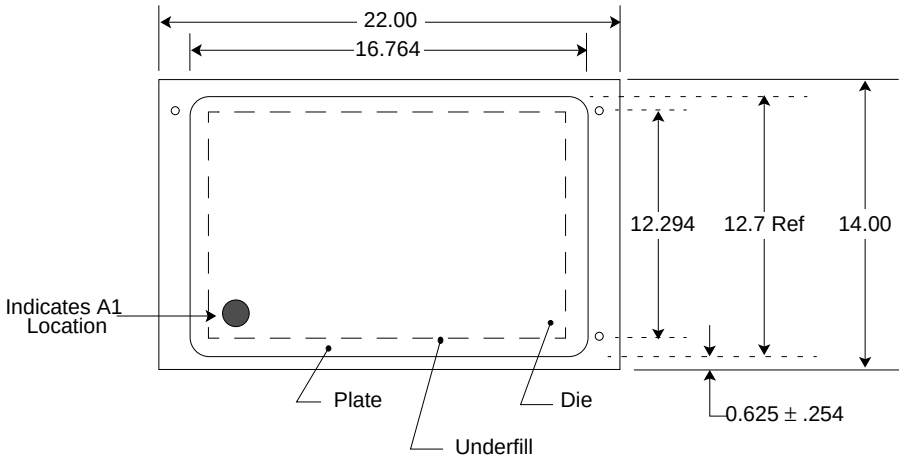
1. PH pins are place holders. BGA bump is a NC (no connect). PH pins are forced to V_{SS}.
2. For 4Mb density, SA(8Mb) becomes a Place Holder (PH).
3. Reserved address bit for 16 Mb density.
4. Reserved for Mode pin.

TAP Controller State Machine

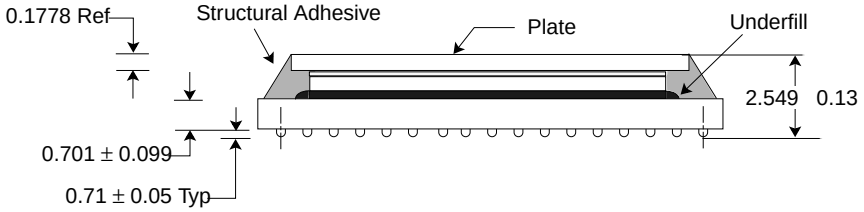


9 x17 BGA Dimensions

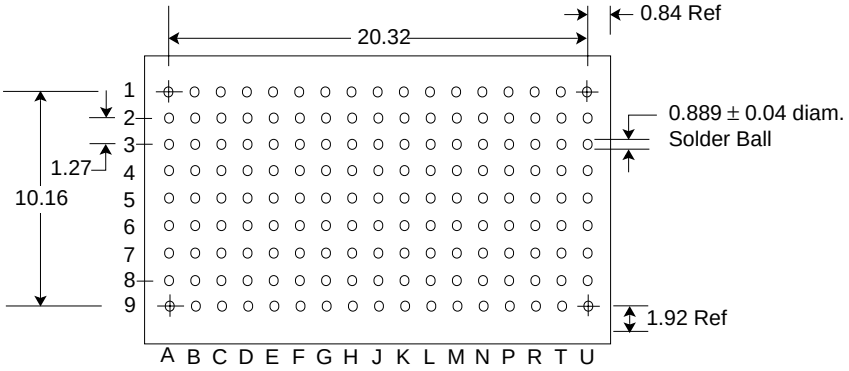
Top View



Side View



Bottom View



Note: All dimensions are in millimeters

References

The following document gives recommendations, restrictions, and limitations for 2nd level attach process:

Double Sided 4Mb SRAM Coupled Cap PBGA Card Assembly Guide

Qualification information, including the scope of application conditions qualified, is available from your marketing representative.

Note: This document contains information on products in the sampling and/or initial production phases of development. This information is subject to change without notice. Verify with your IBM field applications engineer that you have the latest version of this document before finalizing a design.

Revision Log

Date	Contents of Modification
9/98	Initial release.
10/98	Draft to be published.
08/99	General updates.
8/99	Prepare for web publication
11/99	Package drawing update. JTAG ID update. Change clasiffication from Advance to Preliminary
04/05/00	See Recommended DC Operating Conditions on page 9: -Foonote 2 chaged to: V_{IH}(Max)DC = V_{DD} + 0.3 V, V_{IH}(Max)AC = V_{DD}+ 0.85 V (pulse width ≤ 4.0ns)
04/13/00	See AC Characteristics on page 13: Following changes were made to -3P speed sort. -t_{KHKL} = 1.4ns (changed from 1.5ns) -t_{KLKH}= 1.4ns (changed from 1.5ns) -t_{KHBX}= 0.3ns (changed from 0.4ns) -t_{KHDX}= 0.3ns (changed from 0.4ns)
12/05/00	Rev. 07. See AC Characteristics on page 13: -Footnote 5 added, specifying that parameters above are guaranteed by design for -3P and -3 speed sorts. Various minor editorial changes and format refinements made.

Printed in the United States of America December 2000

IBM Microelectronics Division
1580 Route 52, Bldg. 504
Hopewell Junction, NY 12533-6351

The IBM home page can be found at
http://www.ibm.com

The IBM Microelectronics Division home page
can be found at http://www.chips.ibm.com

cddrh251620.07
12/00