IS61C3216B

32K x 16 HIGH-SPEED CMOS STATIC RAM

DECEMBER 2000

FEATURES

- High-speed access time: 10, 12, 15, and 20 ns
- CMOS low power operation
  - — 450 mW (typical) operating
  - — 250 µW (typical) standby
- TTL compatible interface levels
- Single 5V ± 10% power supply
- I/O compatible with 3.3V device
- Fully static operation: no clock or refresh required
- Three state outputs
- Industrial temperature available
- Available in 44-pin 400-mil SOJ package and 44-pin TSOP (Type II)

DESCRIPTION

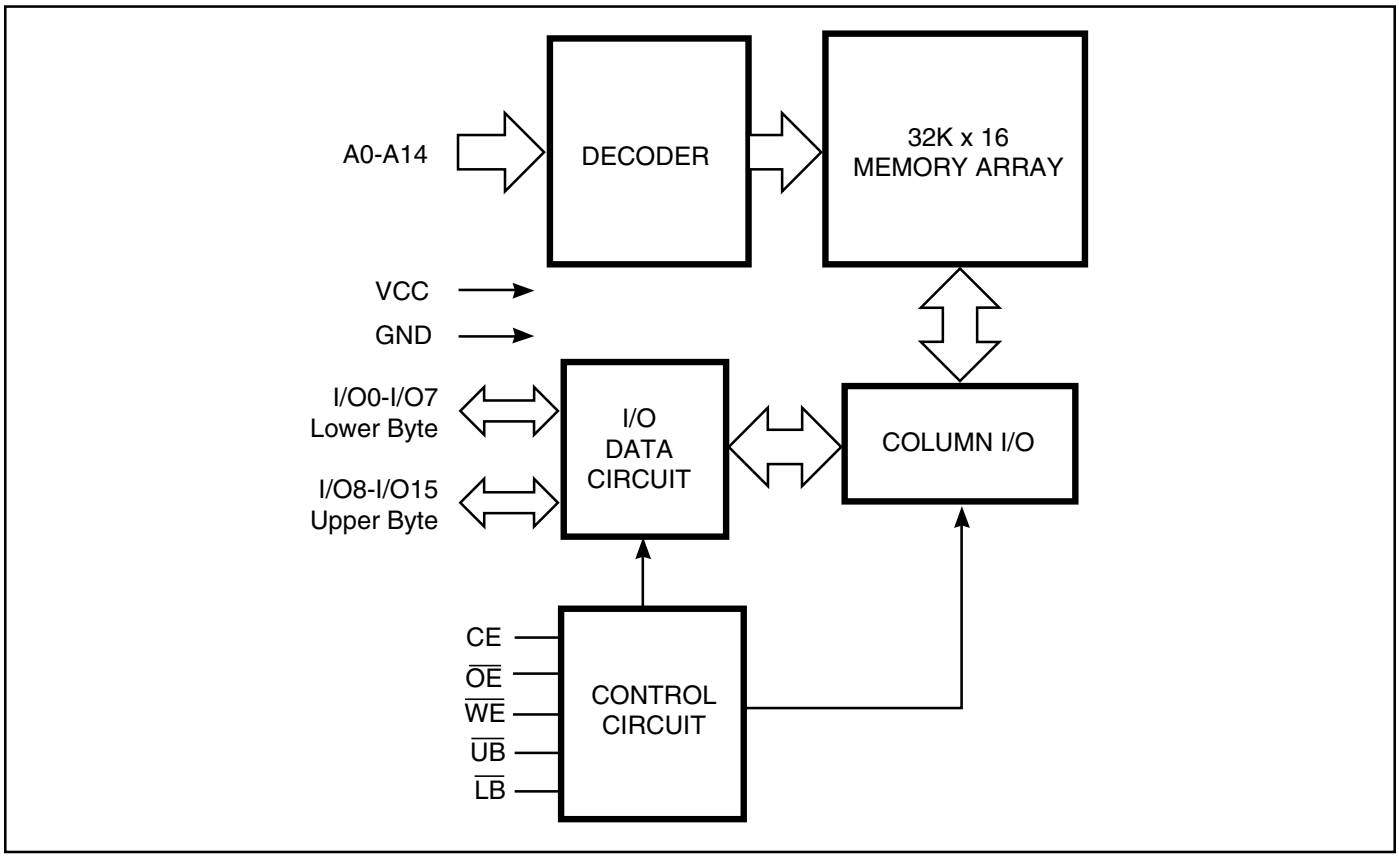
The *ISSI* IS61C3216B is a high-speed, 512K static RAM organized as 32,768 words by 16 bits. It is fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields fast access times with low power consumption.

The device is active when CE is HIGH. When CE is LOW (deselected), the device assumes a standby mode at which the power dissipation can be reduced down to 250 µW (typical) with CMOS input levels.

Easy memory expansion is provided by using Chip Enable and Output Enable inputs, CE and $\overline{OE}$. The active LOW Write Enable ($\overline{WE}$) controls both writing and reading of the memory.A data byte allows Upper Byte ($\overline{UB}$) and Lower Byte ($\overline{LB}$) access.

The IS61C3216B is packaged in the JEDEC standard 44-pin 400-mil SOJ and 44-pin TSOP (Type II).

FUNCTIONAL BLOCK DIAGRAM



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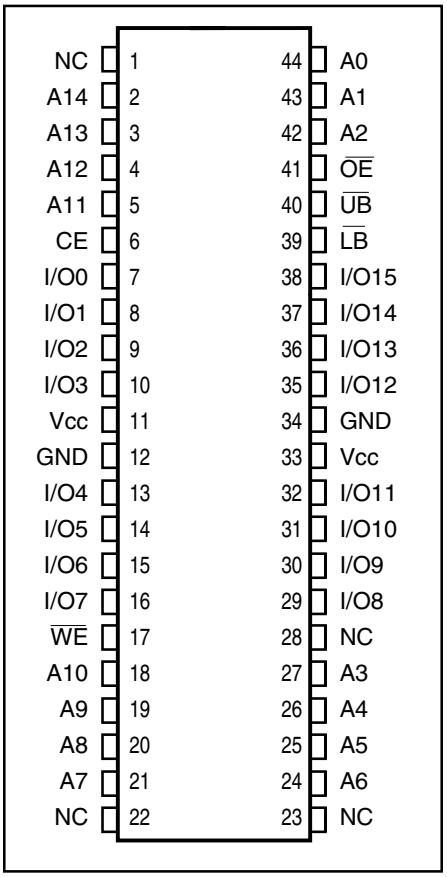
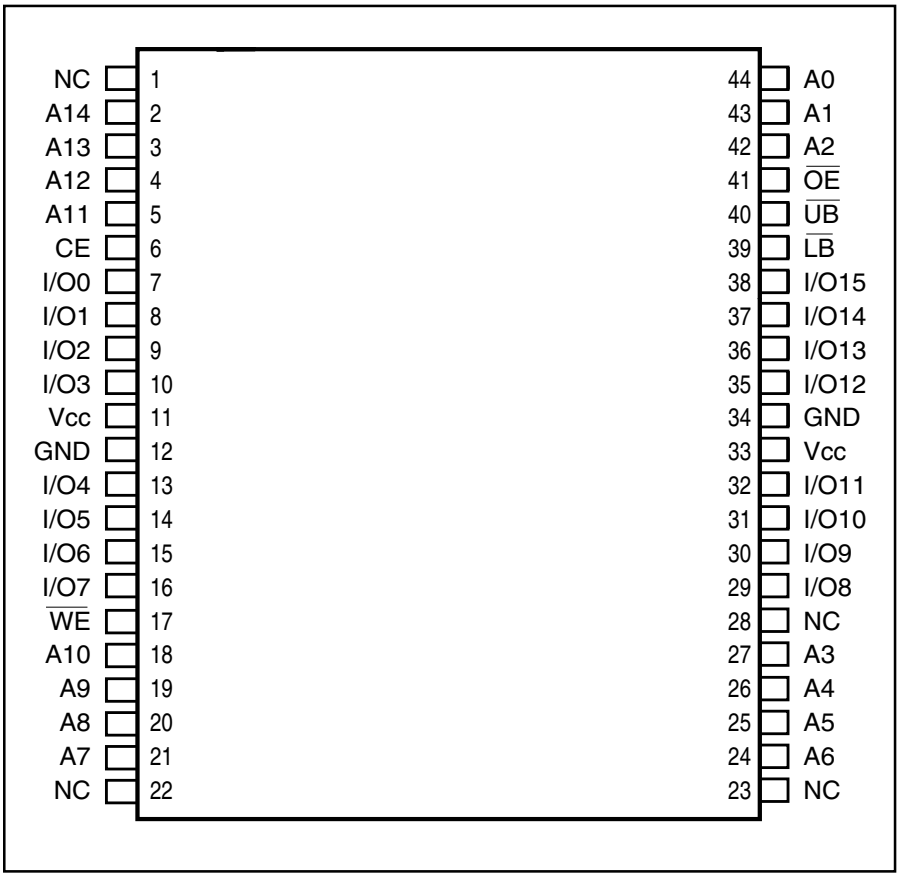
PIN CONFIGURATIONS

44-Pin SOJ



44-Pin TSOP (Type II)



PIN DESCRIPTIONS

A0-A14	Address Inputs
I/O0-I/O15	Data Inputs/Outputs
CE	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input

$\overline{LB}$	Lower-byte Control (I/O0-I/O7)
$\overline{UB}$	Upper-byte Control (I/O8-I/O15)
NC	No Connection
Vcc	Power
GND	Ground

TRUTH TABLE

Mode	$\overline{WE}$	CE	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	I/O0-I/O7	I/O8-I/O15	Vcc Current
Not Selected	X	L	X	X	X	High-Z	High-Z	I_{SB1}, I_{SB2}
Output Disabled	H	H	H	X	X	High-Z	High-Z	I_{CC}
	X	H	X	H	H	High-Z	High-Z	
Read	H	H	L	L	H	D_{OUT}	High-Z	I_{CC}
	H	H	L	H	L	High-Z	D_{OUT}	
	H	H	L	L	L	D_{OUT}	D_{OUT}	
Write	L	H	X	L	H	D_{IN}	High-Z	I_{CC}
	L	H	X	H	L	High-Z	D_{IN}	
	L	H	X	L	L	D_{IN}	D_{IN}	

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage with Respect to GND	–0.5 to +7.0	V
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_{STG}	Storage Temperature	–65 to +150	°C
P_T	Power Dissipation	1.5	W
I_{OUT}	DC Output Current (LOW)	20	mA

Note:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE

Range	Ambient Temperature	Speed	Vcc
Commercial	0°C to +70°C	-10, -12	5V ± 5%
		-15, -20	5V ± 10%
Industrial	–40°C to +85°C	-12	5V ± 5%
		-15, -20	5V ± 10%

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4.0 mA	2.4	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA	—	0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC} + 0.5	V
V_{IL}	Input LOW Voltage[1]		–0.5	0.8	V
I_{LI}	Input Leakage	GND - V_{IN} - V_{CC}	–2	2	µA
I_{LO}	Output Leakage	GND - V_{OUT} - V_{CC}, Outputs Disabled	–2	2	µA

Notes:
1. V_{IL} (min.) = –3.0V for pulse width less than 10 ns.

POWER SUPPLY CHARACTERISTICS[1] (Over Operating Range)

				-10 ns		-12 ns		-15 ns		-20 ns		
Symbol	Parameter	Test Conditions		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
I_{CC}	Vcc Dynamic Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX}	Com.	—	300	—	270	—	250	—	230	mA
			Ind.	—	—	—	290	—	270	—	250	
I_{SB1}	TTL Standby Current (TTL Inputs)	V_{CC} = Max., V_{IN} = V_{IH} or V_{IL} CE • V_{IH}, f = 0	Com.	—	40	—	40	—	40	—	40	mA
			Ind.	—	—	—	45	—	45	—	45	
I_{SB2}	CMOS Standby Current (CMOS Inputs)	V_{CC} = Max., CE • V_{CC} – 0.2V, V_{IN} • V_{CC} – 0.2V, or V_{IN} - 0.2V, f = 0	Com.	—	5	—	5	—	5	—	5	mA
			Ind.	—	—	—	10	—	10	—	10	

Note:
1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

CAPACITANCE[1]

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Input/Output Capacitance	V_{OUT} = 0V	8	pF

Note:
1. Tested initially and after any design or process changes that may affect these parameters.

READ CYCLE SWITCHING CHARACTERISTICS[1] (Over Operating Range)

		-10		-12		-15		-20		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
t_{RC}	Read Cycle Time	10	—	12	—	15	—	20	—	ns
t_{AA}	Address Access Time	—	10	—	12	—	15	—	20	ns
t_{OHA}	Output Hold Time	3	—	3	—	3	—	3	—	ns
t_{ACE}	CE Access Time	—	10	—	12	—	15	—	20	ns
t_{DOE}	$\overline{OE}$ Access Time	—	5	—	5	—	7	—	8	ns
t_{HZOE}[2]	$\overline{OE}$ to High-Z Output	0	5	0	6	0	7	—	8	ns
t_{LZOE}[2]	$\overline{OE}$ to Low-Z Output	0	—	0	—	0	—	0	—	ns
t_{HZCE}[2	CE to High-Z Output	0	5	0	6	0	7	0	8	ns
t_{LZCE}[2]	CE to Low-Z Output	4	—	4	—	4	—	4	—	ns
t_{BA}	$\overline{LB}$, $\overline{UB}$ Access Time	—	5	—	6	—	7	—	8	ns
t_{HZB}	$\overline{LB}$, $\overline{UB}$ to High-Z Output	0	5	0	6	0	7	—	8	ns
t_{LZB}	$\overline{LB}$, $\overline{UB}$ to Low-Z Output	5	—	5	—	5	—	5	—	ns

Notes:
1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1a.
2. Tested with the load in Figure 1b. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. Not 100% tested.

AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	3 ns
Input and Output Timing and Reference Level	1.5V
Output Load	See Figures 1a and 1b

AC TEST LOADS

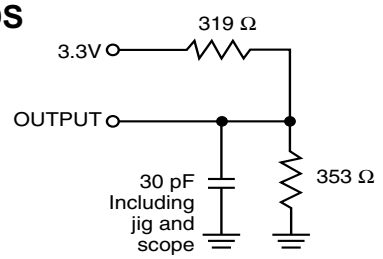


Figure 1a.

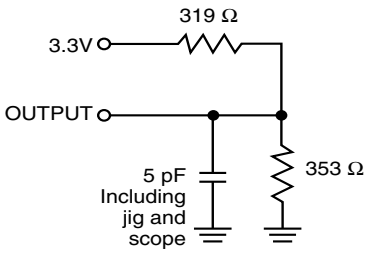
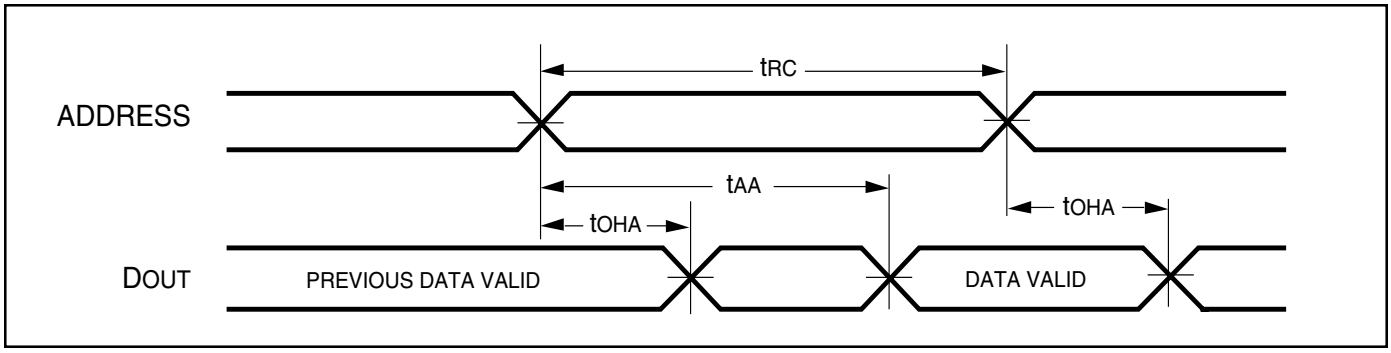


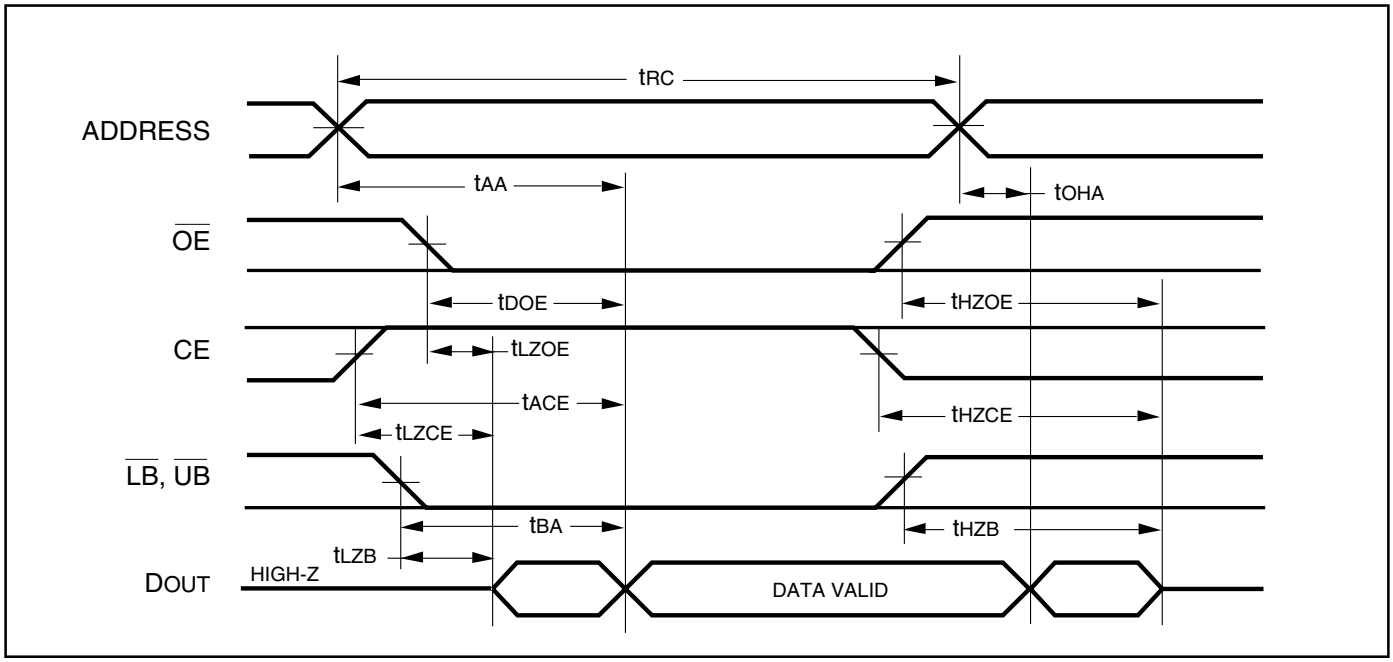
Figure 1b.

AC WAVEFORMS

READ CYCLE NO. 1[1,2] (Address Controlled) (CE = V_{IH}, $\overline{OE}$ = V_{IL}, $\overline{UB}$ or $\overline{LB}$ = V_{IL})



READ CYCLE NO. 2[1,3]



Notes:
1. $\overline{WE}$ is HIGH for a Read Cycle.
2. The device is continuously selected. CE = V_{IH}, $\overline{OE}$, $\overline{UB}$, or $\overline{LB}$ = V_{IL}.
3. Address is valid prior to or coincident with CE HIGH transition.

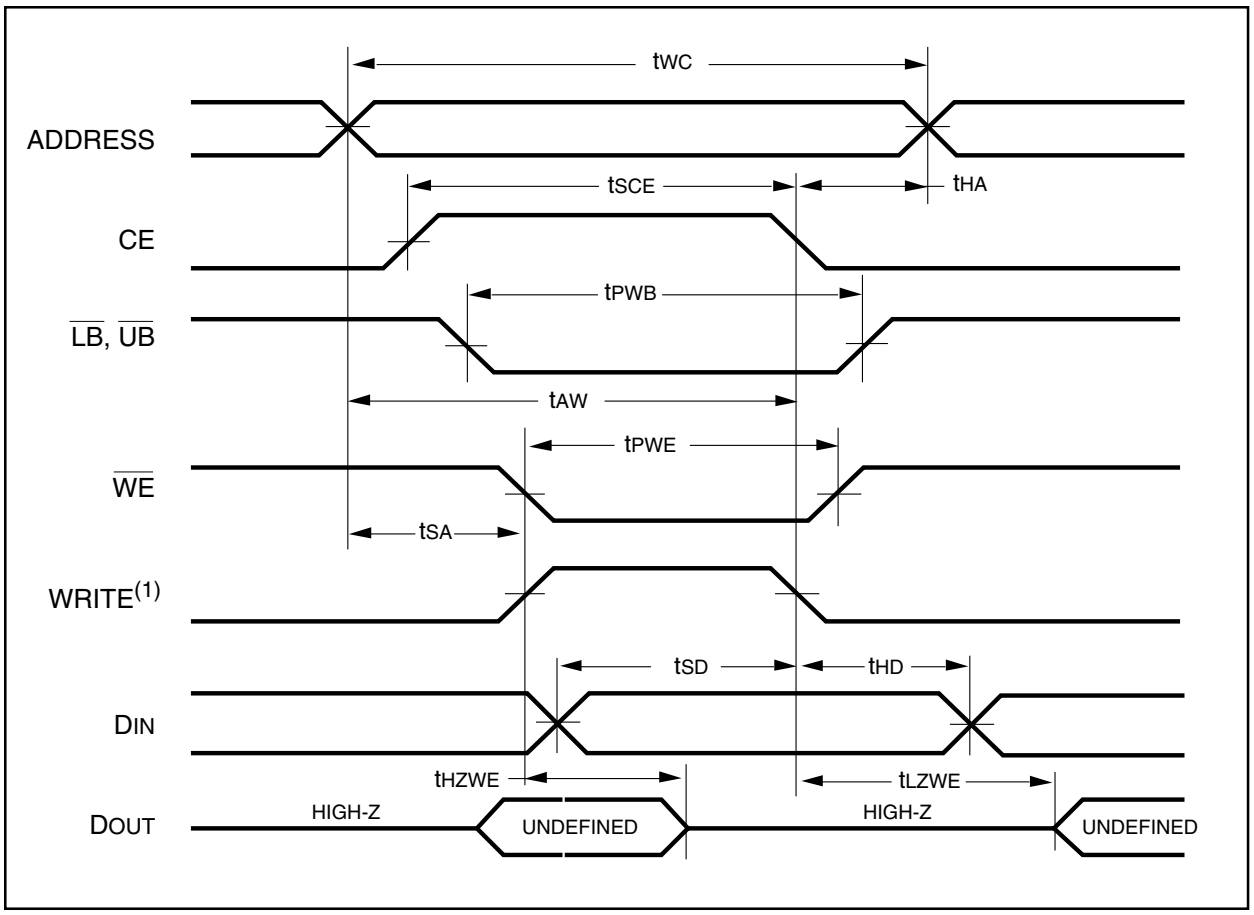
WRITE CYCLE SWITCHING CHARACTERISTICS[1,3] (Over Operating Range)

Symbol	Parameter	-10 Min.	-10 Max.	-12 Min.	-12 Max.	-15 Min.	-15 Max.	-20 Min.	-20 Max.	Unit
t_{WC}	Write Cycle Time	10	—	12	—	15	—	20	—	ns
t_{SCE}	CE to Write End	9	—	10	—	11	—	12	—	ns
t_{AW}	Address Setup Time to Write End	9	—	10	—	11	—	12	—	ns
t_{HA}	Address Hold from Write End	1	—	1	—	1	—	1	—	ns
t_{SA}	Address Setup Time	0	—	0	—	0	—	0	—	ns
t_{PWB}	$\overline{LB}$, $\overline{UB}$ Valid to End of Write	9	—	10	—	11	—	12	—	ns
t_{PWE}	$\overline{WE}$ Pulse Width	7	—	8	—	10	—	11	—	ns
t_{SD}	Data Setup to Write End	5	—	6	—	7	—	8	—	ns
t_{HD}	Data Hold from Write End	0	—	0	—	0	—	0	—	ns
t_{HZWE}[2]	$\overline{WE}$ LOW to High-Z Output	—	5	—	6	—	7	—	8	ns
t_{LZWE}[2]	$\overline{WE}$ HIGH to Low-Z Output	1	—	1	—	1	—	1	—	ns

Notes:
1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1a.
2. Tested with the load in Figure 1b. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of CE HIGH and $\overline{UB}$ or $\overline{LB}$, and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.

AC WAVEFORMS

WRITE CYCLE NO. 1 ($\overline{WE}$ Controlled)[1]



Notes:
1. WRITE is an internally generated signal asserted during an overlap of the LOW states on $\overline{WE}$ and a HIGH state on CE inputs and at least one of the $\overline{LB}$ and $\overline{UB}$ inputs being in the LOW state.

ORDERING INFORMATION

Commercial Range: 0°C to +70°C

Speed (ns)	Order Part No.	Package
10	IS61C3216B-10T	Plastic TSOP (Type II)
	IS61C3216B-10K	400-mil Plastic SOJ
12	IS61C3216B-12T	Plastic TSOP (Type II)
	IS61C3216B-12K	400-mil Plastic SOJ
15	IS61C3216B-15T	Plastic TSOP (Type II)
	IS61C3216B-15K	400-mil Plastic SOJ
20	IS61C3216B-20T	Plastic TSOP (Type II)
	IS61C3216B-20K	400-mil Plastic SOJ

Industrial Range: –40°C to +85°C

Speed (ns)	Order Part No.	Package
12	IS61C3216B-12TI	Plastic TSOP (Type II)
	IS61C3216B-12KI	400-mil Plastic SOJ
15	IS61C3216B-15TI	Plastic TSOP (Type II)
	IS61C3216B-15KI	400-mil Plastic SOJ
20	IS61C3216B-20TI	Plastic TSOP (Type II)
	IS61C3216B-20KI	400-mil Plastic SOJ

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