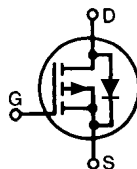


Standard Power MOSFET

P-Channel Enhancement Mode
Avalanche Rated

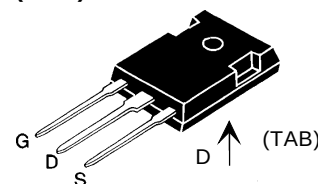
IXTH/IXTT 10P50
IXTH/IXTT 11P50



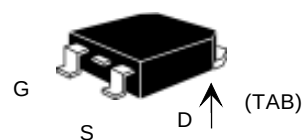
V_{DSS}	I_{D25}	$R_{DS(on)}$
-500 V	-10 A	0.90 Ω
-500 V	-11 A	0.75 Ω

Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	$T_J = 25^\circ\text{C}$ to 150°C	-500	V
V_{DGR}	$T_J = 25^\circ\text{C}$ to 150°C ; $R_{GS} = 1\text{ M}\Omega$	-500	V
V_{GS}	Continuous	± 20	V
V_{GSM}	Transient	± 30	V
I_{D25}	$T_C = 25^\circ\text{C}$	10P50 -10	A
		11P50 -11	A
I_{DM}	$T_C = 25^\circ\text{C}$, pulse width limited by T_J	10P50 -40	A
		11P50 -44	A
I_{AR}	$T_C = 25^\circ\text{C}$	10P50 -10	A
		11P50 -11	A
E_{AR}	$T_C = 25^\circ\text{C}$	30	mJ
P_D	$T_C = 25^\circ\text{C}$	300	W
T_J		-55 ... +150	$^\circ\text{C}$
T_{JM}		150	$^\circ\text{C}$
T_{stg}		-55 ... +150	$^\circ\text{C}$
T_L	Maximum lead temperature for soldering 1.6 mm (0.062 in.) from case for 10 s	300	$^\circ\text{C}$
M_d	Mounting torque (TO-247)	1.13/10	Nm/lb.in.
Weight	TO-247 AD	6	g
	TO-268	4	g

TO-247 AD (IXTH)



TO-268 (IXTT) Case Style



G = Gate
S = Source

D = Drain
TAB = Drain

Symbol	Test Conditions	Characteristic Values ($T_J = 25^\circ\text{C}$, unless otherwise specified)		
		min.	typ.	max.
V_{DSS}	$V_{GS} = 0\text{ V}$, $I_D = -250\text{ }\mu\text{A}$ BV_{DSS} Temperature Coefficient	-500	0.054	V %/K
$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = -250\text{ }\mu\text{A}$ $V_{GS(th)}$ Temperature Coefficient	-3.0	-0.122	V %/K
I_{GSS}	$V_{GS} = \pm 20\text{ V}_{DC}$, $V_{DS} = 0$			± 100 nA
I_{DSS}	$V_{DS} = 0.8 \cdot V_{DSS}$ $V_{GS} = 0\text{ V}$	$T_J = 25^\circ\text{C}$ $T_J = 125^\circ\text{C}$		-200 μA -1 mA
$R_{DS(on)}$	$V_{GS} = -10\text{ V}$, $I_D = 0.5 \cdot I_{D25}$ $R_{DS(on)}$ Temperature Coefficient	10P50 11P50		0.90 Ω 0.75 Ω 0.6 %/K

Features

- International standard packages
- Low $R_{DS(on)}$ HDMOS™ process
- Rugged polysilicon gate cell structure
- Unclamped Inductive Switching (UIS) rated
- Low package inductance
- easy to drive and to protect

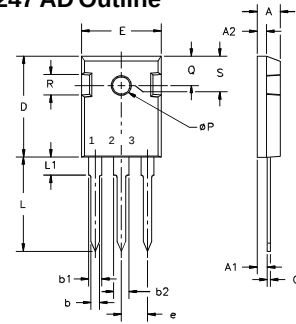
Advantages

- Easy to mount
- Space savings
- High power density

Symbol	Test Conditions	Characteristic Values ($T_J = 25^\circ\text{C}$, unless otherwise specified)		
		min.	typ.	max.
g_{fs}	$V_{DS} = -10\text{ V}$; $I_D = I_{D25}$, pulse test	5	9	S
C_{iss}	$V_{GS} = 0\text{ V}$, $V_{DS} = -25\text{ V}$, $f = 1\text{ MHz}$		4700	pF
C_{oss}			430	pF
C_{rss}			135	pF
$t_{d(on)}$	$V_{GS} = -10\text{ V}$, $V_{DS} = 0.5 V_{DSS}$, $I_D = 0.5 I_{D25}$ $R_G = 4.7\ \Omega$ (External)		33	ns
t_r			27	ns
$t_{d(off)}$			35	ns
t_f			35	ns
$Q_{G(on)}$	$V_{GS} = -10\text{ V}$, $V_{DS} = 0.5 V_{DSS}$, $I_D = 0.5 I_{D25}$		130	nC
Q_{GS}			46	nC
Q_{GD}			92	nC
R_{thJC}	(TO-247)		0.25	0.42 K/W
R_{thCS}				K/W

Source-Drain Diode		Characteristic Values ($T_J = 25^\circ\text{C}$, unless otherwise specified)		
Symbol	Test Conditions	min.	typ.	max.
I_S	$V_{GS} = 0$	10P50 11P50		-10 A -11 A
I_{SM}	Repetitive; pulse width limited by T_{JM}	10P50 11P50		-40 A -44 A
V_{SD}	$I_F = I_S$, $V_{GS} = 0\text{ V}$, Pulse test, $t \leq 300\ \mu\text{s}$, duty cycle $d \leq 2\%$			-3 V
t_{rr}	$I_F = I_S$, $di/dt = 100\text{ A}/\mu\text{s}$		500	ns

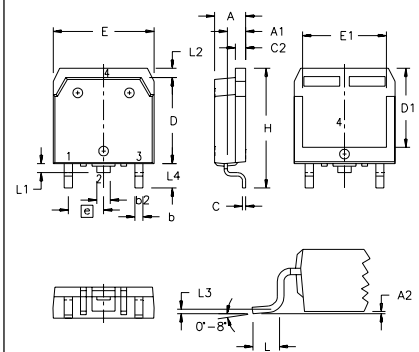
TO-247 AD Outline



Terminals: 1 - Gate 2 - Drain
3 - Source Tab - Drain

Dim.	Millimeter Min.	Max.	Inches Min.	Max.
A	4.7	5.3	.185	.209
A ₁	2.2	2.54	.087	.102
A ₂	2.2	2.6	.059	.098
b	1.0	1.4	.040	.055
b ₁	1.65	2.13	.065	.084
b ₂	2.87	3.12	.113	.123
C	.4	.8	.016	.031
D	20.80	21.46	.819	.845
E	15.75	16.26	.610	.640
e	5.20	5.72	0.205	0.225
L	19.81	20.32	.780	.800
L ₁		4.50		.177
ØP	3.55	3.65	.140	.144
Q	5.89	6.40	0.232	0.252
R	4.32	5.49	.170	.216
S	6.15	BSC	.242	BSC

TO-268 Outline



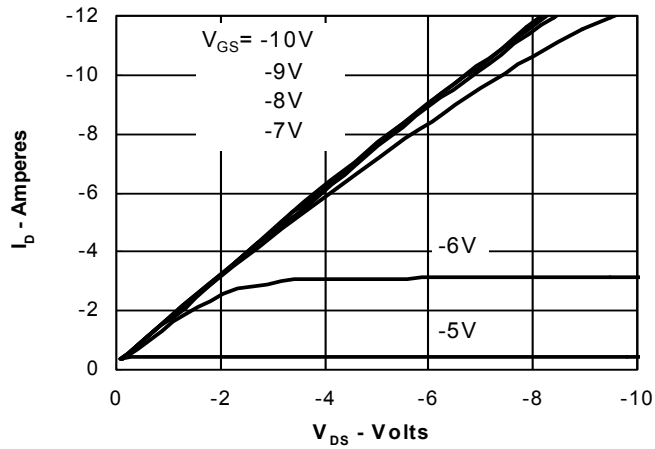
Terminals: 1 - Gate 2 - Drain
3 - Source Tab - Drain

SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.193	.201	4.90	5.10
A ₁	.106	.114	2.70	2.90
A ₂	.001	.010	0.02	0.25
b	.045	.057	1.15	1.45
b ₂	.075	.083	1.90	2.10
C	.016	.026	0.40	0.65
C ₂	.057	.063	1.45	1.60
D	.543	.551	13.80	14.00
D ₁	.488	.500	12.40	12.70
E	.624	.632	15.85	16.05
E ₁	.524	.535	13.30	13.60
e	.215	BSC	5.45	BSC
H	.736	.752	18.70	19.10
L	.094	.106	2.40	2.70
L ₁	.047	.055	1.20	1.40
L ₂	.039	.045	1.00	1.15
L ₃	.010	BSC	0.25	BSC
L ₄	.150	.161	3.80	4.10

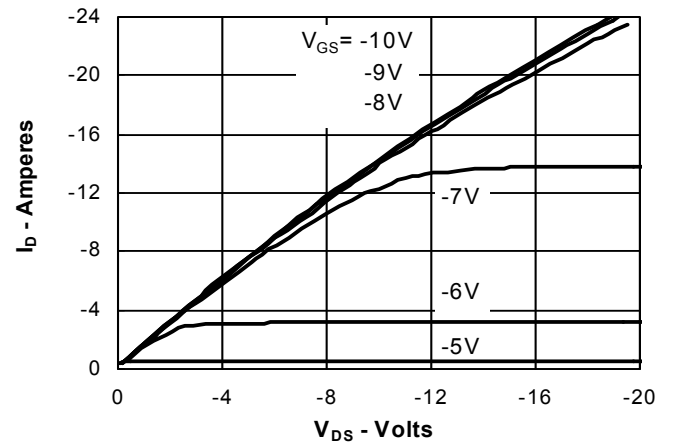
IXYS reserves the right to change limits, test conditions, and dimensions.

IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents:	4,835,592	4,881,106	5,017,508	5,049,961	5,187,117	5,486,715	6,306,728B1
	4,850,072	4,931,844	5,034,796	5,063,307	5,237,481	5,381,025	

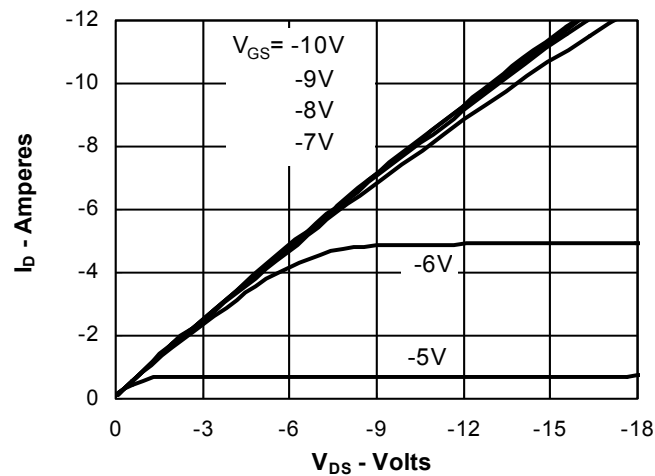
**Fig. 1. Output Characteristics
@ 25 Deg. C**



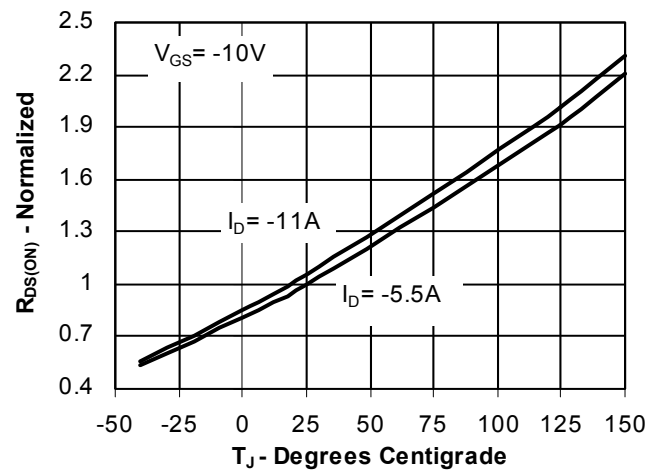
**Fig. 2. Extended Output Characteristics
@ 25 Deg. C**



**Fig. 3. Output Characteristics
@ 125 Deg. C**



**Fig. 4. $R_{DS(ON)}$ Normalized to I_{D25} Value
vs. Junction Temperature**



**Fig. 5. $R_{DS(ON)}$ Normalized to I_{D25}
Value vs. I_D**

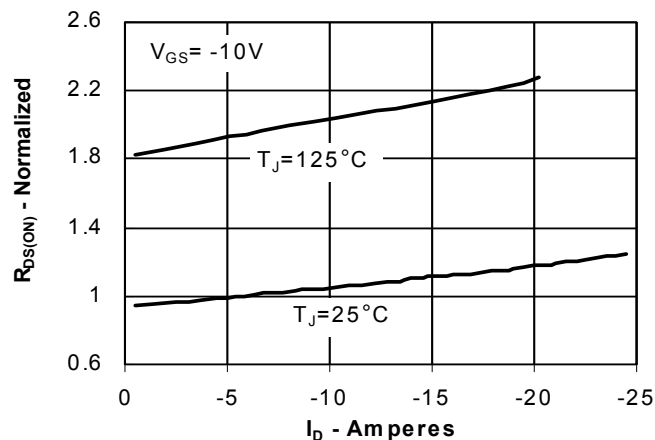


Fig. 6. Input Admittance

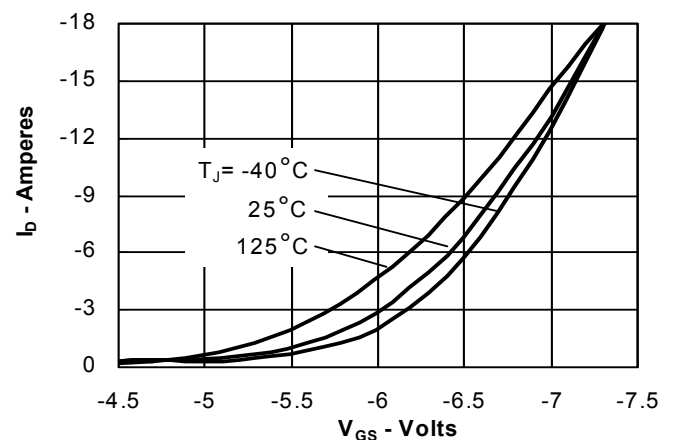


Fig. 7. Transconductance

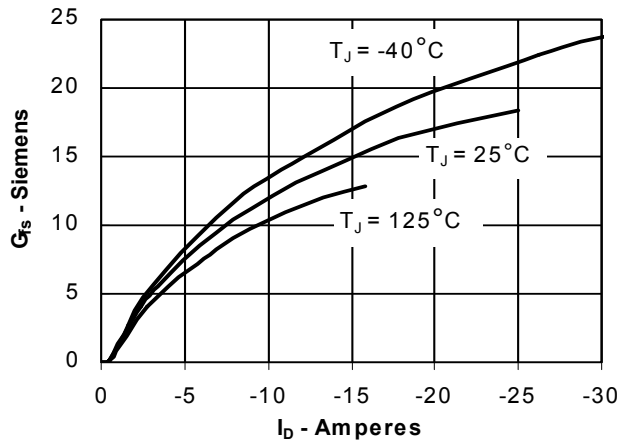


Fig. 8. Source Current vs. Source-To-Drain Voltage

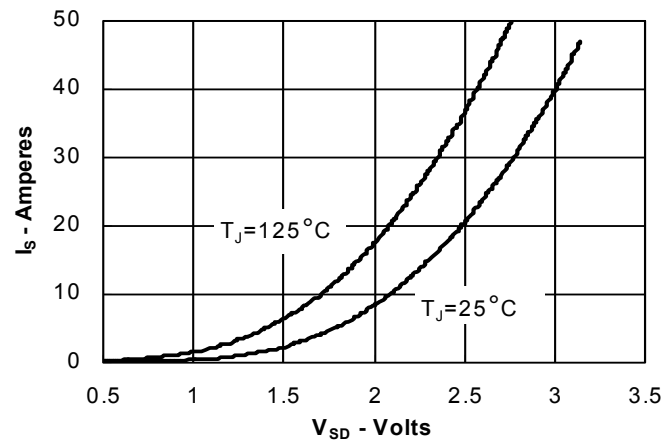


Fig. 9. Gate Charge

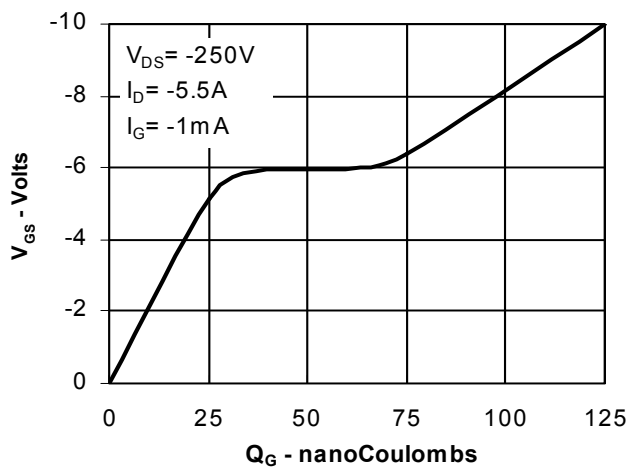


Fig. 10. Capacitance

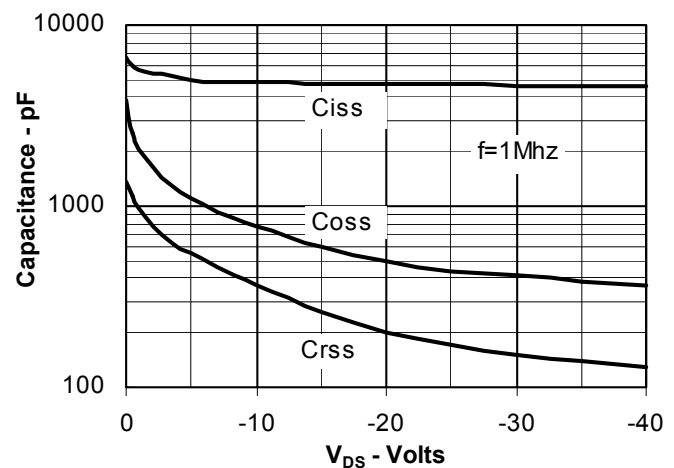
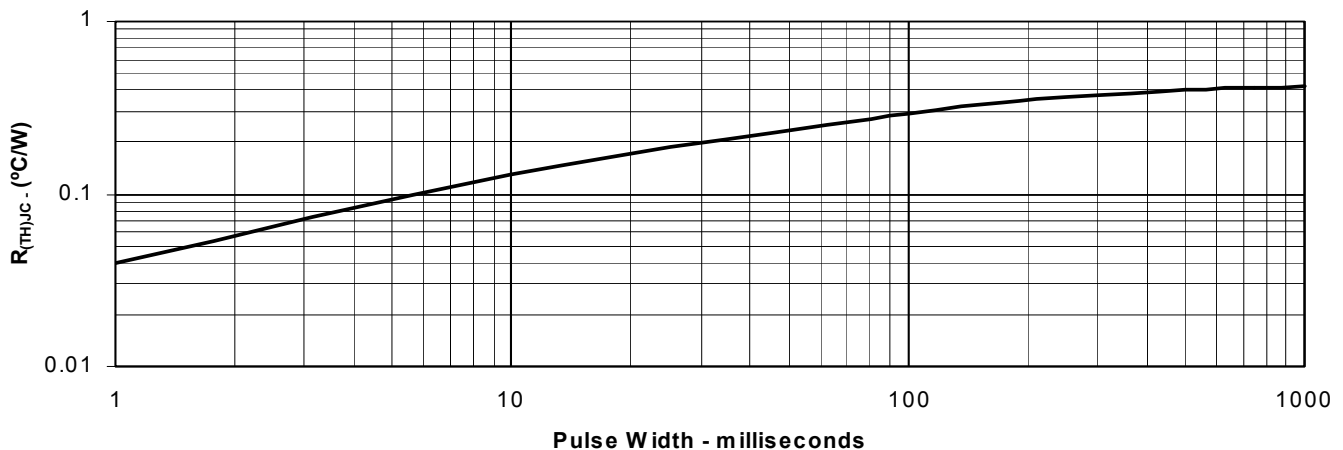


Fig. 14. Maximum Transient Thermal Resistance



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